

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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HUTCHINSON TECHNOLOGY INC.,  
HUTCHINSON TECHNOLOGY OPERATIONS (Thailand) CO., LTD.,  
Petitioners,

v.

NITTO DENKO CORPORATION,  
Patent Owner.

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Case IPR2017-01499  
Patent 7,923,644

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Before THOMAS L. GIANNETTI, CHRISTA P. ZADO, and  
MELISSA A. HAAPALA, *Administrative Patent Judges*.

HAAPALA, *Administrative Patent Judge*.

DECISION  
Denying Institution of *Inter Partes* Review  
37 C.F.R. § 42.108

Hutchinson Technology Incorporated and Hutchinson Technology Operations (Thailand) Co., Ltd. (collectively, “Petitioner”) filed a Petition pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1–4 and 6 of U.S. Patent No. 7,923,644 B2 (“the ’644 patent”). Paper 2 (“Pet.”). Nitto Denko Corporation (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). Applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we deny Petitioner’s request and do not institute an *inter partes* review of the ’644 patent.

## I. BACKGROUND

### A. *The ’644 Patent (Ex. 1001)*

The ’644 patent describes a particular type of printed circuit board (suspension board) for aligning the magnetic head of a hard disk drive with a desired track of a magnetic disk. *See* Ex. 1001, 1:7–9, 1:13–15. The printed circuit board has reduced characteristic impedances of wiring patterns. *Id.* at 1:49–56. Figure 1 is depicted below:

FIG. 1

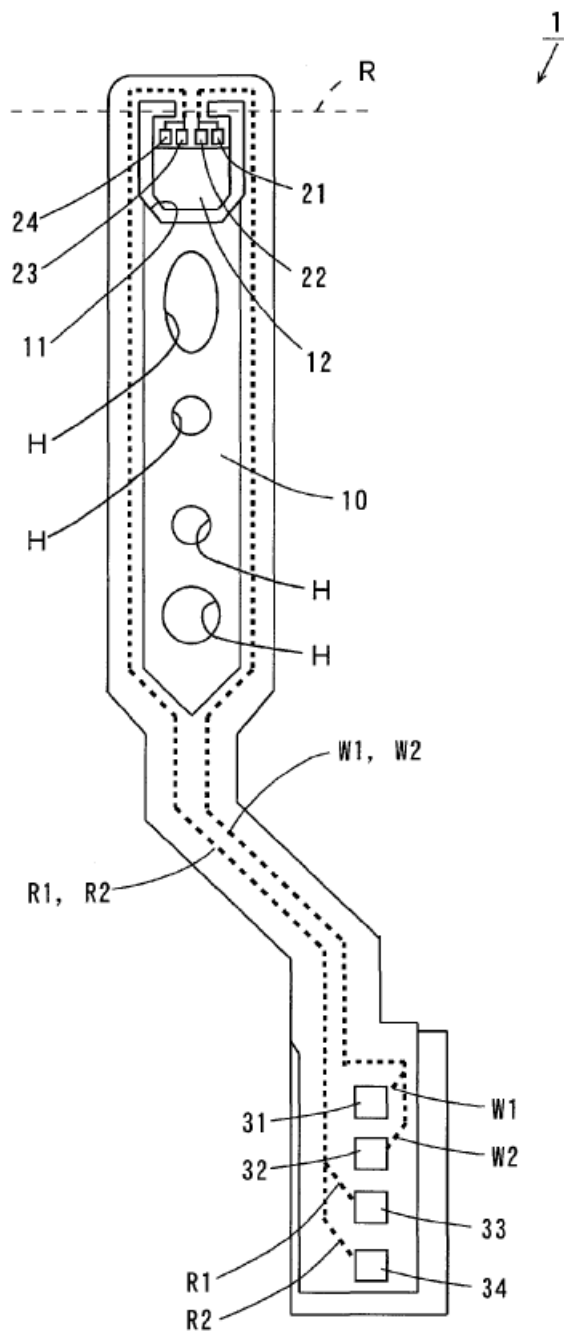


Figure 1 is a plan view of a suspension board. *Id.* at 5:58–59. Suspension board 1 includes suspension body 10 formed of a long-sized metal substrate. *Id.* at 6:34–36. Write wiring patterns W1, W2 and read wiring patterns R1, R2 are formed on suspension body 10. *Id.* at 6:36–38. Electrode pads 21, 22, 23, 24 are formed on one end of the suspension body and electrode pads

31, 32, 33, 34 are formed on the other end. *Id.* at 6:46–49. Electrode pads 21 to 24 and electrode pads 31 to 34 are electrically connected to one another through wiring patterns W1, W2 and read wiring patterns R1, R2, respectively. *Id.* at 6:49–53.

Figure 2 of the '644 patent, as annotated in the Preliminary Response (at p. 4), is depicted below:

FIG. 2

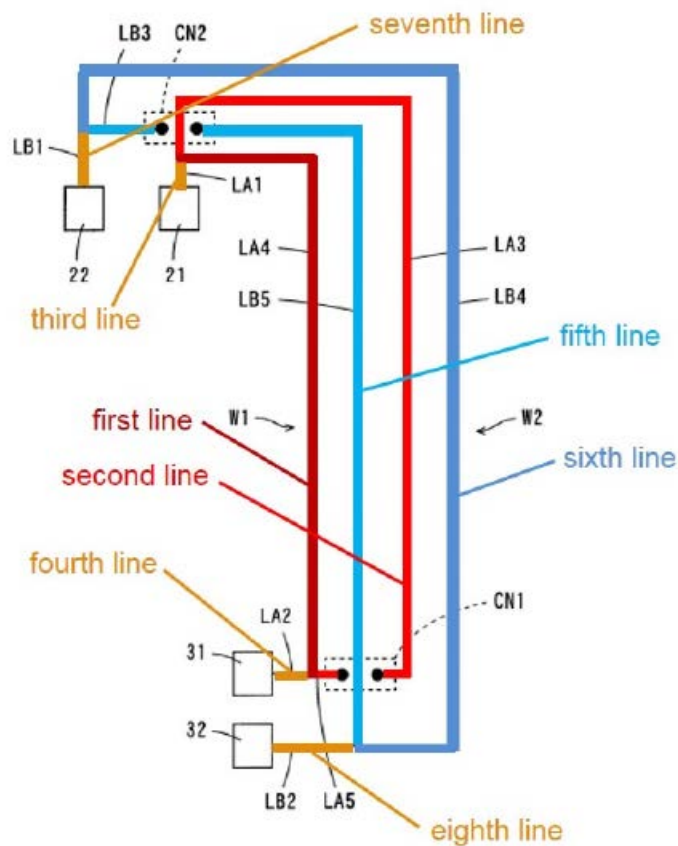


Figure 2 is an annotated schematic diagram showing the configurations of write wiring patterns W1, W2. Ex. 1001, 6:65–67. Write wiring pattern 1 (depicted in red and yellow) is constituted by lines LA4 (first line), LA3/LA5 (divided second line), LA1 (third line), and LA2 (fourth line). *Id.* at 7:1–2. LA1 is connected to electrode pad 21 and LA2 is connected to

electrode pad 31. *Id.* at 7:2–4. One end of lines LA3, LA4 are integrated with line LA1, and the other end of line LA3 and end of line LA5 are electrically connected to each other in intersection region CN1. *Id.* at 7:5–8.

Write wiring pattern 2 (depicted in blue and yellow) is constituted by lines LB3/LB5 (divided fifth line), LB4 (sixth line), LB1 (seventh line), and LB2 (eighth line). *Id.* at 7:11–12. LB1 is connected to electrode pad 22 and LB2 is connected to electrode pad 32. *Id.* at 7:12–13. One ends of lines LB3, LB4 are integrated with line LB1, and the other end of line LB3 and end of line LB5 are electrically connected to each other in intersection region CN2. *Id.* at 7:14–17.

Lines LA3, LA4, LB4, and LB5 are in parallel with one another and arranged so that LA3 is located between lines LB4, LB5 and LB5 is located between lines LA3, LA4. *Id.* at 7:20–25. LA3 of write wiring pattern W1 extends to pass through a portion in between the ends of lines LB3, LB5 in intersection region CN2, and LB5 of write wiring pattern W2 extends to pass through a portion in between the ends of lines LA3, LA5 in intersection region CN1. *Id.* at 7:25–31.

*B. Illustrative Claim*

Claims 1 and 6 are independent claims. Claim 1 is illustrative of the subject matter of the claims at issue:

1. A printed circuit board comprising:
  - an insulating layer;
  - first and second wiring patterns that are formed on one surface of said insulating layer and constitute a signal line pair;
  - first and second electrode pads that are formed on one surface of said insulating layer and are connected to said first wiring pattern;

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