Trials@uspto.gov
571.272.7822

Paper No. 8
Filed: January 31, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORP., UMC GROUP (USA), SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORP., SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORP., SEMICONDUCTOR MANUFACTURING INTERNATIONAL (BEIJINIG) CORP., and SMIC, AMERICAS
Petitioner,
v.
LONE STAR SILICON INNOVATIONS LLC
Patent Owner.

Case IPR2017-01513
Patent 5,973,372

Before GRACE KARAFFA OBERMANN, JENNIFER MEYER CHAGNON, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

OBERMANN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Petitioner filed a Petition seeking *inter partes* review of claims 1 and 4–6 of U.S. Patent No. 5,973,372. Ex. 1001 ("the '372 patent"). Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 7 ("Prelim. Resp.").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). An *inter partes* review may be instituted only upon a showing that "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Taking account of the information presented in the Petition and Preliminary Response, we determine that the Petition fails to make out that threshold showing for review. Accordingly, we deny the Petition and decline to institute a trial.

I. BACKGROUND

A. Related Proceedings

The parties identify the following district court infringement lawsuits as involving the '372 patent. These lawsuits were originally filed in the Eastern District of Texas in November 2016 and subsequently transferred to the Northern District of California:

Lone Star Silicon Innovations, LLC v. United Microelectronics Corp., No. 3:17-cv-04033 (N.D. Cal.); and

Lone Star Silicon Innovations, LLC v. Semiconductor Mfg. Int'l Corp., No. 3:17-cv-03980 (N.D. Cal.).

Pet. viii; Prelim. Resp. 2–3.

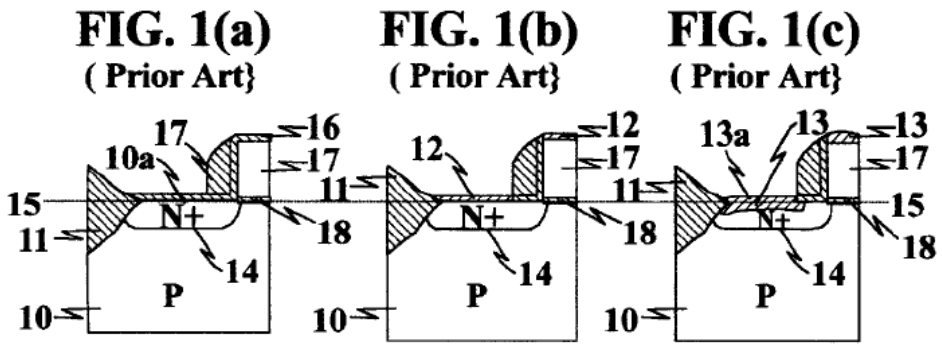
Patent Owner identifies additional lawsuits and *inter partes* reviews that do not involve the '372 patent. *See* Prelim. Resp. 3–5.

B. The '372 Patent (Ex. 1001)

The '372 patent is titled "Silicided Shallow Junction Transistor Formation and Structure with High and Low Breakdown Voltages." Ex. 1001, [54]. The '372 patent specification discloses a method for fabricating integrated circuits and, more specifically, "fabricating silicided shallow junctions and the resultant structure." *Id.* at 1:7–10. The challenged claims are directed to an integrated circuit structure. *Id.* at 7:42–8:8, 8:13–19 (claims 1, 4–6); *see id.* at 4:67–5:1 (describing "the device structure of the present invention").

By way of background, the '372 patent states that advanced submicron integrated circuits require scaling down of the vertical and lateral dimensions, including the junction depth. *Id.* at 1:33–40. Very shallow junctions result in parasitic resistances, which the art has addressed by the use of metal silicides at the shallow junctions. *Id.* at 1:40–50. The '372 patent identifies and addresses a problem that arises in the fabrication of silicided shallow junctions, namely: "a major portion (~one-half) of the originally implanted shallow junction in the silicon substrate is consumed by the silicidation in the conventional silicidation process and such consumption of the silicon substrate during silicidation degrades the integrity of the shallow junctions and sets a lower limit for the junction depth." *Id.* at 1:50–56.

That prior art problem of silicide encroachment into the shallow junctions is depicted in Figure 1(c) of the '372 patent, in which "the major growth of the [metal] silicide is into the silicon substrate"—"as evidenced by the dashed line 15." *Id.* at 4:11–14. Figure 1(c), together with Figures 1(a) and 1(b), is reproduced below:



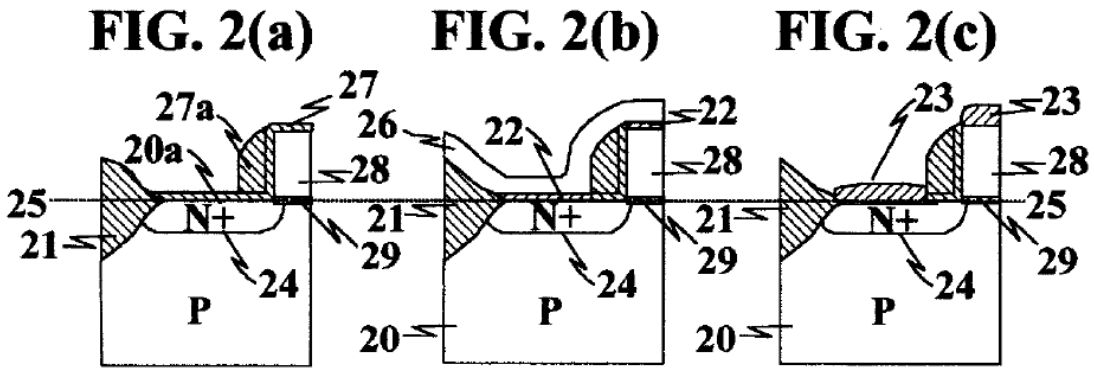
Figures 1(a), 1(b), and 1(c) are cross-sectional views of a prior art method of forming a refractory metal silicide at the surface of an active region of a transistor. *Id.* at 2:53–55.

According to the disclosure of the ’372 patent, in the prior art device depicted in Figure 1, “the major growth of the titanium silicide is *into* the silicon substrate,” and “the greatest growth is at the edges where the N+ impurities are in lower concentration than in the center of the active region.” *Id.* at 4:12–16 (emphasis added); *see id.* at Fig. 1(c) (depicting the encroachment of metal silicide 13 into the shallow junction). The ’372 patent specification discloses that this encroachment of the metal silicide results in shallow junctions that “become[] ever more shallow and the result is degrading of the integrity of the shallow junctions.” *Id.* at 4:17–18.

To address that problem, the ’372 patent proposes a method of forming metal silicide over a shallow junction, whereby the metal reacts preferentially with a layer of silicon deposited on the metal layer, rather than with the silicon substrate beneath the metal layer. Ex. 1001, 2:16–25; *see also id.* at 1:13–32 (describing conventional silicidation process). Using this method, “only a small amount of the silicon of the silicon substrate is consumed during the silicide reaction.” *Id.* at 2:31–32. The ’372 patent also describes a structure that results from this process, namely, an integrated circuit having a silicon substrate, a shallow junction

in the substrate, a metal silicide layer at the shallow junction, and a silicon epitaxy layer between the silicon substrate and the metal silicide. *Id.* at 2:39–46.

The '372 patent explains: "With a thick amorphous silicon layer 26, which is sufficiently thick so as to not be totally consumed by the silicidation, silicon atoms from the amorphous silicon layer migrate through the [metal] silicide 23 and to the single crystal silicon substrate." *Id.* at 4:62–67. "In accordance with the device structure of the present invention,"[1] that migration results in "a solid phase epitaxy layer as shown in the vicinity of" silicide 43 "and the N+ boundary." *Id.* at 4:62–5:3. Figure 2(c) depicts that epitaxy layer as a dark line in the region of dashed line 25, denoting the upper surface region of original silicon substrate 20*a*, which is shown in Figure 2(a). Figures 2(a), 2(b), and 2(c) are reproduced below:



Figures 2(a), 2(b), and 2(c) are cross-sectional views of a method of forming a refractory metal silicide at the surface of an active region of a transistor. *Id.* at 2:56–58.

As explained in the next section, the '372 patent specification (including the illustration provided in Figure 2(c)) describes an "epitaxial silicon layer" that, in

[1] Although the '372 patent elsewhere describes "the present invention" as a fabrication "method" (Ex. 1001, 2:63–64), the claimed invention is directed to an integrated circuit. *Id.* at 7:42–8:8, 8:13–19 (claims 1 and 4–6).

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.