

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.,  
Petitioner,

v.

LONE STAR SILICON INNOVATIONS LLC,  
Patent Owner.

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Case IPR2017-01560  
Patent 5,912,188

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Before GRACE KARAFFA OBERMANN,  
JENNIFER MEYER CHAGNON, and ELIZABETH M. ROESEL,  
*Administrative Patent Judges.*

ROESEL, *Administrative Patent Judge.*

DECISION  
Institution of *Inter Partes* Review  
*37 C.F.R. § 42.108*

This case concerns U.S. Patent No. 5,912,188. Ex. 1001 (“the ’188 patent”). Petitioner, Micron Technology, Inc., filed a Petition seeking *inter partes* review of claims 1–5, 7–13, 15–23, and 25–29 of the ’188 patent. Paper 1 (“Pet.”). Patent Owner, Lone Star Silicon Innovations LLC, filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). An *inter partes* review may not be instituted “unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Applying that standard, we institute an *inter partes* review of claims 1–5, 8–13, 15, and 18–20 of the ’188 patent for the reasons and on the ground set forth below.

The following findings of fact and conclusions of law are not final, but are made for the sole purpose of determining whether Petitioner meets the threshold for initiating review. Any final decision shall be based on the full trial record, including any response timely filed by Patent Owner.

## I. BACKGROUND

### A. *Related Matters*

Pursuant to 37 C.F.R. § 42.8(b)(2), the parties identify the following patent infringement lawsuits involving the ’188 patent:

*Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*,  
No. 2:16-cv-01116 (E.D. Tex. filed Oct. 7, 2016); and

*Lone Star Silicon Innovations, LLC v. Toshiba Corp.*, No. 2:16-  
cv-01170 (E.D. Tex. filed Oct. 14, 2016).

Pet. 2–3; Paper 4, 2 (Patent Owner Mandatory Notices).

In addition, Patent Owner identifies IPR2017-01561 involving the '188 patent. Paper 4, 1. Patent Owner identifies additional *inter partes* review proceedings involving Micron Technology as Petitioner and Lone Star Silicon Innovations LLC and states that the patents involved in the additional proceedings are not related to the '188 patent. *Id.*

*B. Asserted Grounds of Unpatentability*

Petitioner asserts the following grounds of unpatentability under 35 U.S.C. § 103(a):

Reference(s)	Claim(s)
Hashimoto <sup>1</sup>	1–5, 8–13, 15, 18, and 19
Hashimoto and Sung <sup>2</sup>	20
Hashimoto and Kawai <sup>3</sup>	7, 16, 17, 21–23, and 25–27
Hashimoto, Sung, and Kawai	28 and 29

Pet. 4. Petitioner supports its challenge with a Declaration of Richard Fair, Ph.D. Ex. 1003. Patent Owner supports its Preliminary Response with a Declaration of W. R. Bottoms, Ph.D. Ex. 2001.

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<sup>1</sup> Hashimoto et al., Japanese Patent Publication No. JP H9-64297, published March 7, 1997, with certified English translation, Ex. 1005 (“Hashimoto”). Hashimoto is asserted as prior art under 35 U.S.C. § 102(b). Pet. 18 n.3.

<sup>2</sup> Sung, US 5,550,078, filed June 28, 1995 and issued August 27, 1996, Ex. 1006 (“Sung”). Sung is asserted as prior art under 35 U.S.C. § 102(a) and (e). Pet. 24 n.4.

<sup>3</sup> Kawai et al., Japanese Patent Publication No. JP H8-46173, published February 16, 1996, with certified English translation, Ex. 1007 (“Kawai”). Kawai is asserted as prior art under 35 U.S.C. § 102(b). Pet. 26 n.5.

*C. The '188 Patent (Ex. 1001)*

The '188 patent was issued June 15, 1999 from Application No. 08/905,686, filed August 4, 1997. Ex. 1001, [45], [21], [22].

The '188 patent relates to integrated circuit manufacturing, and more specifically, to a method of forming a contact hole in an interlevel dielectric layer using dual etch stops. *Id.* at [54], [57], 1:7–10.

The '188 patent addresses the problem of overetching and gouging of underlying materials when forming contact holes. *Id.* at 2:29–50, 2:65–67, 3:2–4. According to the '188 patent, one known solution is an interlevel dielectric layer with a thick silicon dioxide layer on a thin silicon nitride layer and a two-step etching process, whereby the first etch is highly selective of silicon dioxide with respect to silicon nitride. *Id.* at 2:51–56. The '188 patent states that this approach has a drawback in that the second etch is highly selective of both silicon nitride and silicon and may cause substantial damage to an underlying silicon surface. *Id.* at 2:58–63.

The solution proposed by the '188 patent is an interlevel dielectric with first, second, and third dielectric layers and a three-step etching process, whereby the first dielectric layer is etched using the second dielectric layer as an etch stop, and the second dielectric layer is etched using the third dielectric layer as an etch stop. *Id.* at 3:4–10.

Figures 1A–1J of the '188 patent illustrate process steps for forming a contact hole in an interlevel dielectric. *Id.* at 4:17–20. Figures 1D through 1G are reproduced below:

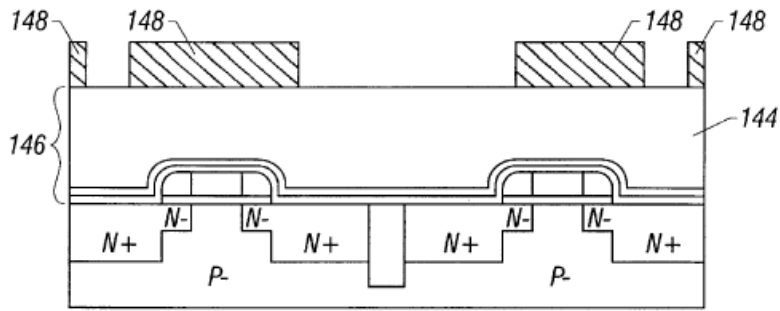


FIG. 1D

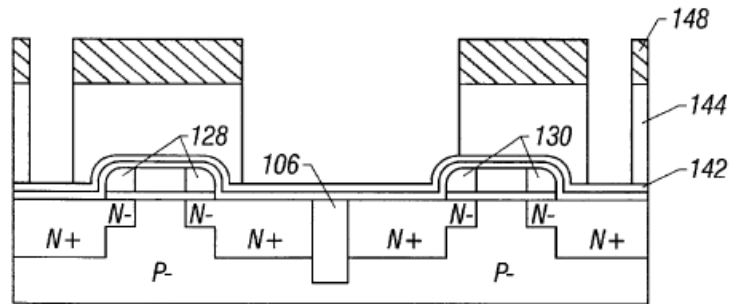


FIG. 1E

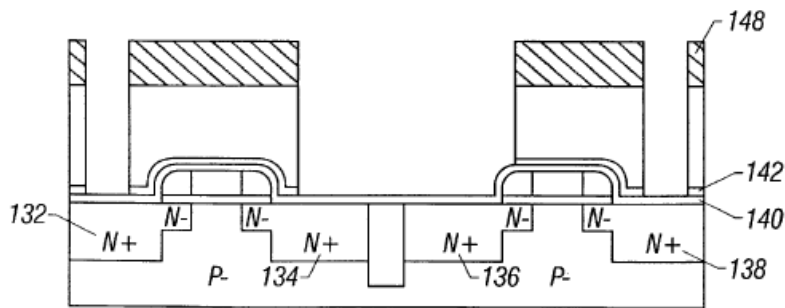


FIG. 1F

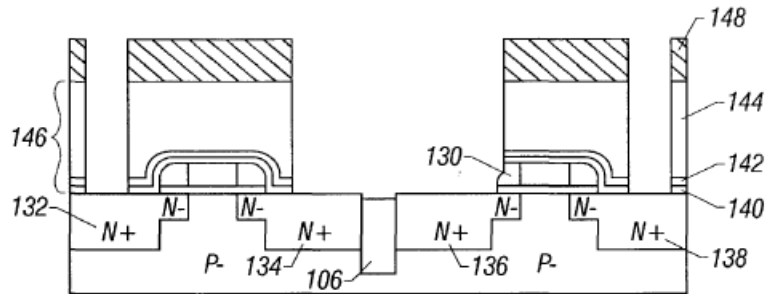


FIG. 1G

Figures 1D through 1G of the '188 patent illustrate process steps for forming a contact hole in an interlevel dielectric. Ex. 1001, 4:17-20. Figure 1D

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