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Paper 9
Entered: December 21, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION, TOSHIBA MEMORY CORPORATION, and TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.,
Petitioners,

v.

MACRONIX INTERNATIONAL CO., LTD.,
Patent Owner.

Case IPR2017-01632
Patent 8,035,417 B1

Before KEN B. BARRETT, JENNIFER S. BISK, and JASON M. REPKO, *Administrative Patent Judges.*

REPKO, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background and Summary

Toshiba Corporation, Toshiba Memory Corporation, and Toshiba America Electronic Components, Inc. (collectively, "Petitioners") filed a petition (Paper 1, "Pet.")[1] to institute an *inter partes* review of claims 1–7, 11–16, and 18 of U.S. Patent No. 8,035,417 B1 (Ex. 1001, the "'417 patent"). 35 U.S.C. § 311. Macronix International Co., Ltd. ("Patent Owner") filed a Preliminary Response. Paper 8 ("Prelim. Resp.").

For the reasons that follow, we institute an *inter partes* review for all the challenged claims.

B. Related Matters

According to Petitioners, the '417 patent is involved in matters before the United States International Trade Commission (Inv. No. 337-TA-1046) and the United States District Court for the Southern District of California (Case No. 17-cv-0462). Pet. 1–2.

C. The '417 Patent

The '417 patent describes an output buffer circuit with a variable output drive strength. Ex. 1001, Abstract. An output buffer drives a load by setting a voltage on an output line. *Id.* at 5:61–62. The driver capability, however, should be suitable for its application. *See id.* at 5:61–67. An

[1] In an email message to the Board on August 21, 2017, Petitioners requested authorization to file a corrected version of the petition. In response, the Board requested that the parties meet and confer regarding this request and update the Board. However, no update has been received. We have entered these emails as Exhibit 3001.

unsuitable driver capability may slow performance or create power noise. *See id.* To reduce power noise and meet speed and loading requirements, the '417 patent describes combining multiple output buffer circuits to vary the drive strength. *Id.* at 8:49–55. For example, Figure 6 of the '417 patent, reproduced below, illustrates a block diagram of multiple output buffer circuits sharing output DQ.

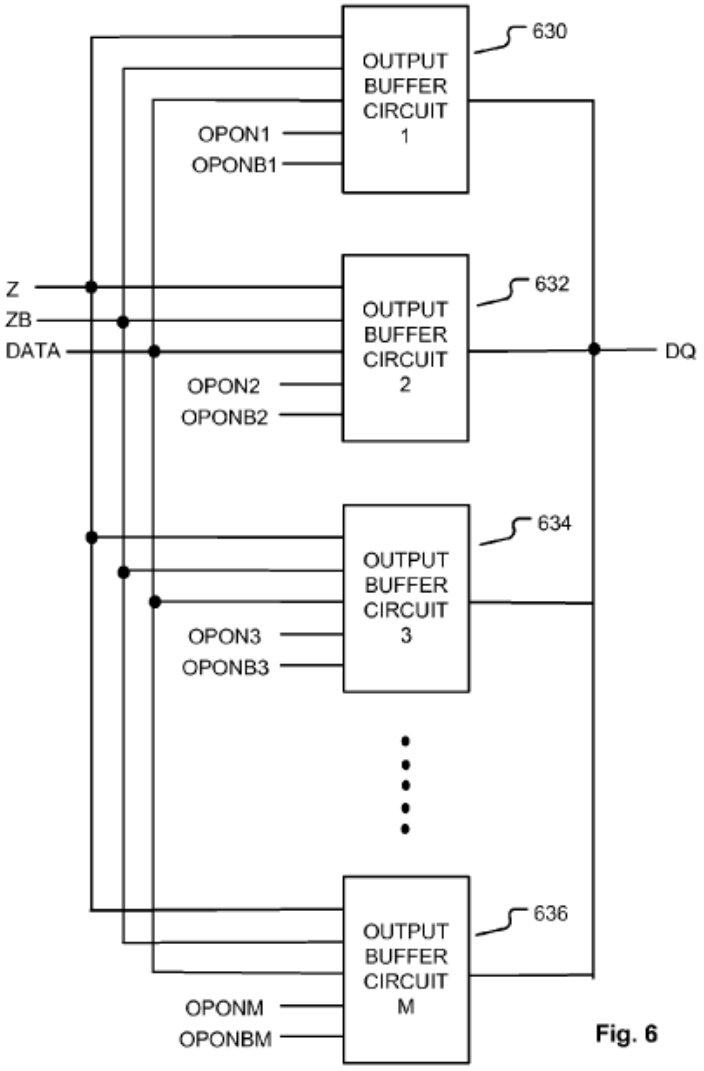

Fig. 6

As shown in Figure 6 above, the output buffers receive control-input signals (OPON1–OPONM and OPONB1–OPONBM). *Id.* at 8:35–38. These control-input signals can enable some output buffer circuits and disable

others. *Id.* at 8:39–48. The combined drive strength equals the sum of the drive strengths of the enabled output buffers. *Id.* at 8:49–53. Accordingly, the '417 patent discloses varying the combined drive strength by selectively enabling and disabling the buffers. *Id.* at 8:42–55.

D. Illustrative Claim

Of the challenged claims, claims 1, 11, and 18 are independent. Claims 2–7 and 12–16 depend directly or indirectly from claims 1 or 11. Claim 1 is illustrative:

> 1. An apparatus, comprising:
> a plurality of output buffer circuits coupled in parallel to provide a combined output drive strength, each output buffer circuit of the plurality of output buffer circuits including:
> a buffer data input receiving a data input signal shared across the plurality of output buffer circuits;
> a first buffer enable input receiving a first buffer enable signal shared across the plurality of output buffer circuits;
> a second buffer enable input receiving a second buffer enable signal customized across the plurality of output buffer circuits;
> a buffer data output providing a data output signal having a drive strength,
> wherein the data output signal is combined across the plurality of output buffer circuits to provide a combined data output signal having the combined output drive strength, and the combined output drive strength is tuned by the second buffer enable signals customized across the plurality of output buffer circuits,
> wherein buffer enable signals are received together with complements of the buffer enable signals, and the buffer enable signals and the complements of the buffer enable signals control pairs of transistors having opposite conductivity types, and the buffer enable signals include the first buffer enable signal and the second buffer enable signal.

Id. at 9:35–62.

E. Applied References

Petitioners rely upon the references listed below. Pet. 4.

Reference	Exhibit
U.S. Patent No. 7,307,836 B2 to Yen et al.	1003
U.S. Patent Application No. 2007/0247194 A1 to Jain	1004

F. Asserted Grounds of Unpatentability

Petitioners assert the following grounds of unpatentability. Pet. 4.

References	Basis	Claims challenged
Yen et al.	Pre-AIA[2] 35 U.S.C. § 102(a) and (b)	1–7, 11–16, and 18
Yen et al. and Jain	Pre-AIA 35 U.S.C. § 103	1–7, 11–16, and 18

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable interpretation standard, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary

[2] Because the claims at issue have a filing date prior to March 16, 2013, the effective date of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), the pre-AIA version of 35 U.S.C. §§ 102 and 103 applies here.

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