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Paper 49
Entered: November 20, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

Case IPR2017-01781
Patent 8,161,344 B2

Before MINN CHUNG, DANIEL J. GALLIGAN, and JOHN A. HUDALLA, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, NVIDIA Corporation ("Petitioner") challenges the patentability of claims 1–5, 8–12, 14, 16–23, 26–31, 43–45, and 48–51 of U.S. Patent No. 8,161,344 B2 ("the '344 patent," Ex. 1001), which is assigned to Polaris Innovations Limited ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has not proven by a preponderance of the evidence that claims 1–5, 8–12, 14, 16–23, 26–31, 43–45, and 48–51 of the '344 patent are unpatentable in this proceeding. *See* 35 U.S.C. § 316(e) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

On July 25, 2017, Petitioner requested *inter partes* review of claims 1–5, 8–12, 14, 16–23, 26–31, 43–45, and 48–51 of the '344 patent. Paper 2 ("Pet."). Patent Owner filed a Preliminary Response. Paper 7 ("Prelim. Resp."). We instituted trial on all grounds of unpatentability, which are as follows:

1. Whether claims 1, 8–12, 14, 16, 19, 26–31, 43, and 48–51 are unpatentable under 35 U.S.C. § 102(e) over Yoon;[1]

2. Whether claims 16 and 18 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Yoon and Wickeraad;[2]

[1] US 2008/0082900 A1, filed Dec. 28, 2006, issued Apr. 3, 2008 (Ex. 1020).
[2] US 2007/0234182 A1, filed Mar. 31, 2006, issued Oct. 4, 2007 (Ex. 1022).

3. Whether claims 2, 20, and 44 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Yoon and LaBerge;[3]

4. Whether claims 4, 5, 22, 23, and 45 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Yoon and Hancock;[4]

5. Whether claims 1–3, 8–10, 12, 16–21, 26–28, 30, 43, 44, 48, 49, and 51 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Raz[5] and Wickeraad; and

6. Whether claims 4, 5, 11, 22, 23, 29, 45, and 50 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Raz, Wickeraad, and Hancock.

Paper 9 ("Dec. on Inst."), 37.

During the trial, Patent Owner filed a Request for Rehearing (Paper 11), which we denied (Paper 15). Patent Owner also filed a Response (Paper 18, "PO Resp."), and Petitioner filed a Reply (Paper 26, "Pet. Reply").[6] With our authorization (Paper 31), Patent Owner filed a sur-reply addressing prior conception and diligent reduction to practice (Paper 37), and Petitioner filed a responsive brief (Paper 41). Each party also filed a Motion to Exclude evidence. Papers 32, 34.

An oral hearing was held on August 17, 2018, a transcript of which appears in the record. Paper 45 ("Tr."). Following the hearing, with our authorization (Paper 46), the parties filed additional briefing addressing the

[3] US 2003/0158981 A1, issued Aug. 21, 2003 (Ex. 1024).
[4] US 4,277,844, issued July 7, 1981 (Ex. 1023).
[5] US 2005/0066110 A1, issued Mar. 24, 2005 (Ex. 1021).
[6] Paper 26 is a redacted version of Paper 25. For this Final Written Decision, we do not rely on any material that was filed under seal, and, therefore, we refer to the public, redacted version of Petitioner's Reply.

broadest reasonable interpretation of "data arrangement alteration." Papers 47, 48.

B. Real Parties in Interest

Patent Owner identifies itself, Wi-LAN Inc., and Quarterhill Inc. as real parties-in-interest. Paper 6, 2.

C. Related Matters

Petitioner and Patent Owner cite the following judicial matter involving the '505 patent: *Polaris Innovations Ltd. v. Dell Inc. & NVIDIA Corp.*, Case No. 4:16-cv-07005 (N.D. Cal.). Pet. 93; Paper 4, 2–3. The '344 patent is also at issue in IPR2017-01346, in which we are issuing a final written decision concurrently with this Decision.

D. The '344 Patent and Illustrative Claim

The '344 patent generally relates to circuits for error coding. Ex. 1001, Abstract, 1:11–12. Figure 1A, reproduced below, illustrates an embodiment of such a circuit.

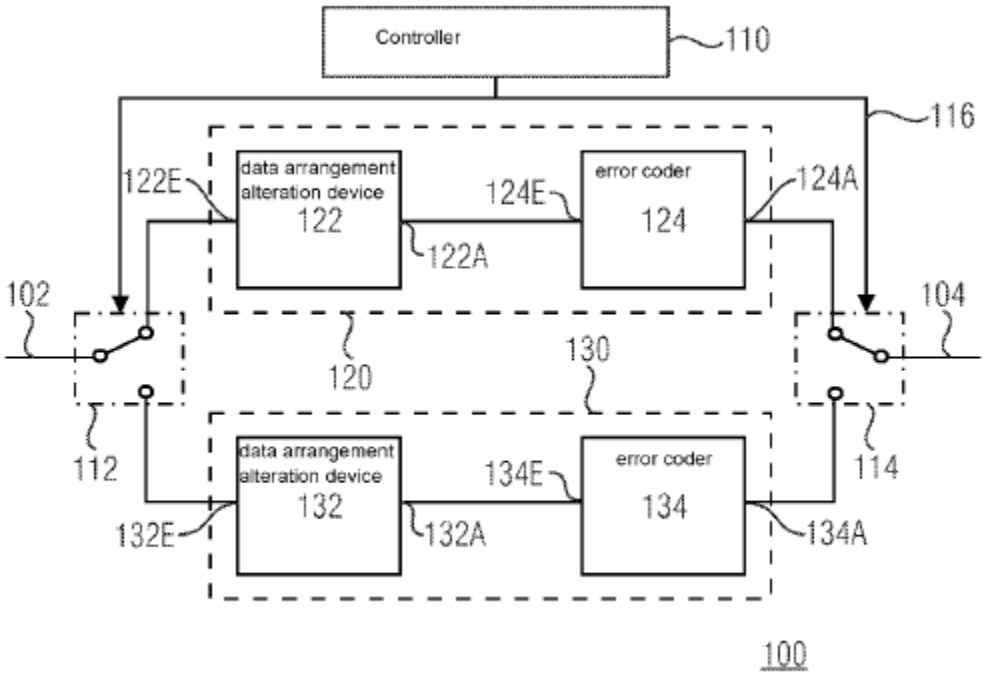

FIG 1A

Figure 1A illustrates an error coding circuit having controller 110, input 102, first error coding path 120, second error coding path 130, and output 104. Ex. 1001, 3:27–30. As illustrated in Figure 1A, each of error coding paths 120 and 130 has a data arrangement alteration device and an error coder. Ex. 1001, 3:30–34. The '344 patent explains that control indicator 116 is used to select between the first and second error coding paths. Ex. 1001, 4:41–47.

Of the claims at issue in the present proceeding, claims 1, 16, 19, and 43 are independent claims. Claim 1 is illustrative and is reproduced below.

> 1. A circuit for creating an error coding data block for a first data block, the circuit comprising:
>
> a first error coding path adapted to selectively create a first error coding data block in accordance with a first error coding; and

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