

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS AMERICA, INC. and
ASUS COMPUTER INTERNATIONAL, INC.,
Petitioner,

v.

JAMES B. GOODMAN,
Patent Owner

Case IPR2017-02021¹
Patent 6,243,315 B1

Before BRIAN J. McNAMARA, PATRICK M. BOUCHER, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Case IPR2018-00047, filed by ASUS Computer International, Inc. (“ASUS”), has been joined with this proceeding.

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Samsung Electronics America, Inc. and ASUS Computer International, Inc. (collectively “Petitioner”) challenge the patentability of claims 1–20 (“the challenged claims”) of U.S. Patent No. 6,243,315 B1 (Ex. 1001, “the ’315 patent”²), owned by James B. Goodman (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during trial. For the reasons discussed below, we determine that Petitioner has shown by a preponderance of the evidence that claims 1, 5, 10, and 16 of the ’315 patent are unpatentable but has not shown by a preponderance of the evidence that claims 2–4, 6–9, 11–15, and 17–20 are unpatentable.

A. Procedural History

On August 29, 2017, Samsung Electronics America, Inc. filed a Petition requesting an *inter partes* review of claims 1–20 of the ’315 patent. Paper 2 (“Pet.”). The Petition is supported by the declaration testimony of Dr. Andrew Wolfe. Ex. 1002. Patent Owner filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

On October 12, 2017, ASUS Computer International, Inc. (“ASUS”) filed a Petition requesting *inter partes* review of claims 1–20 of the ’315 patent on the same grounds and arguments presented in Case IPR2017-02021 and requested joinder with Case IPR2017-02021. *See* Case IPR2018-00047, Papers 2, 3. Patent Owner filed a Preliminary Response. Case IPR2018-00047, Paper 7.

² Citations are to IPR2017-02021 unless otherwise indicated.

IPR2017-02021
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On March 9, 2018, we instituted an *inter partes* review of the challenged claims in IPR2017-02021. Paper 7 (“Decision on Institution” or “Dec. on Inst.”). On March 20, 2018, we granted ASUS’s request for *inter partes* review and for joinder of the IPR2018-00047 proceeding with IPR2017-02021. IPR2018-00047, Paper 9. On June 1, 2018, Patent Owner filed a Patent Owner Response. Paper 10. On August 24, 2018, Petitioner filed a Reply. Paper 11 (“Reply”).

A hearing was held on November 16, 2018. A transcript of the hearing has been entered into the record. Paper 18 (“Tr.”).

B. Related Proceedings

Petitioner identifies the following litigations as related proceedings: *Goodman v. Samsung Electronics America, Inc.*, Case No. 1:17-cv-05539 (S.D.N.Y.); *Goodman v. Hewlett-Packard Co.*, Case No. 4:16-cv-03195 (S.D. Tex.); *Goodman v. ASUS Computer Int’l, Inc.*, Case No. 4:16-cv-03232 (S.D. Tex.). Pet. 2.

Patent Owner further identifies the following litigations as related proceedings: *Goodman v. ASUS Computer Int’l*, Case No. 17-cv-05542 (N.D. Cal.) (transferred from the S.D. Tex.); *Goodman v. Lenovo (United States) Inc.*, Case No. 17-cv-06782; and *Goodman v. Acer American Corp.*, Case No. 17-cv-07297. See Prelim. Resp. 2; IPR2018-00047, Prelim. Resp. 3.

We also note that the ’315 patent was the subject of a Final Written Decision in *HP Inc. v. Goodman* (Case IPR2017-01994) in which we determined claims 1 and 5 were not shown to be unpatentable but that claims 10 and 16 were shown to be unpatentable. IPR2017-01994, Paper 16. The ’315 patent was also the subject of a petition for *inter partes* review in

SMART Modular Technologies, Inc. v. Goodman, Case IPR2015-01675, in which the Board instituted *inter partes* review and subsequently granted the parties' joint motion to terminate. See IPR2015-01675, Paper 20.

C. The '315 patent

The '315 patent is directed to memory systems having volatile solid state memory devices that retain information when an electrical power source is applied but lose their memory contents when power is removed. Ex. 1001, 2:54–58, 3:46–52. To reduce energy consumption and preserve memory contents, volatile memory devices are placed in low power “self-refresh mode” when the memory system is not receiving requests for access. See *id.* at 3:46–54 (stating the “low power mode utilizes significantly less electrical current than when the memory device is in the operating mode or powered up mode”), 3:25–30 (stating “placing the memory devices into a power down self-refresh mode . . . will maintain the data using a minimum of electrical power”). The memory system of the '315 patent has a control device interposed electrically between the memory devices and a central processing unit (“CPU”). *Id.* at 3:54–56. The control device senses CPU access of the memory devices and conditions the memory devices to an operating mode condition prior to allowing access to the information contained therein. *Id.* at 3:56–59. The control device also places the solid state memory devices into a low power standby mode when it “senses the termination of a memory cycle.” *Id.* at 3:59–62.

Figure 1 of the '315 patent, reproduced below, illustrates a preferred embodiment in which address and control busses are electrically isolated from the memory devices when the memory devices are in a power down self refresh mode. *Id.* at 5:60–63.

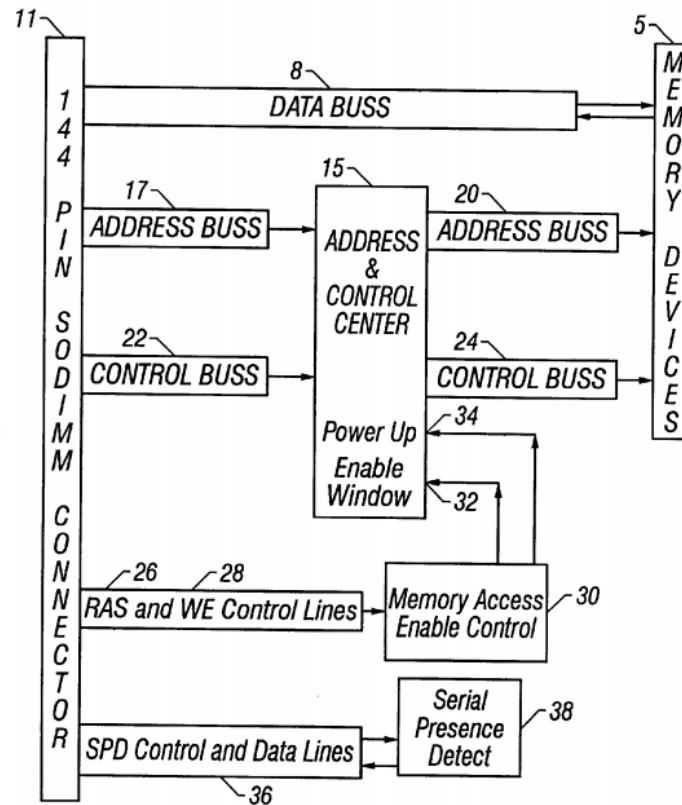


FIG. 1

As shown in Figure 1 of the '315 patent above, control device 15 is interdisposed between address buss 17 and address buss 20 (*id.* at 5:50–52) as well as in between control buss 22 and control buss 24 (*id.* at 5:54–56). Control devices 15 isolates address buss 17 and control buss 22 from memory devices 5 when the memory devices are in a power down self refresh mode. *Id.* at 5:60–63. By isolating the memory devices from control buss 22 and address buss 17, control device 15 prevents errant signals from erroneously changing or affecting the data being retained by memory devices 5. *Id.* at 5:63–67.

Figure 1 also shows row address select (“RAS”) control lines 26 and write enable (“WE”) control lines 28, which are connected to memory access enable control device 30. *Id.* at 6:1–3. Memory access enable control device 30 receives signals from the CPU indicating that a memory

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