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Paper 18
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner,

v.

VLSI TECHNOLOGY LLC,

Patent Owner.

Case IPR2018-01038
Patent 8,566,836 B2

Before BART A. GERSTENBLITH, MINN CHUNG, and KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314(a)

I. INTRODUCTION

Intel Corporation ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1–11, 13, 14, 18, 20, and 21 ("the challenged claims") of U.S. Patent No. 8,566,836 B2 (Ex. 1001, "the '836 patent"). Paper 2 ("Pet."). On September 6, 2018, VLSI Technology LLC ("Patent Owner") filed a Patent Owner Preliminary Response (Paper 9) and a Corrected Patent Owner Preliminary Response (Paper 10, "Prelim. Resp."). Following authorization, Petitioner filed a Reply (Paper 14, "Reply") and Patent Owner filed a Sur-Reply to Petitioner's Reply (Paper 15, "Sur-Reply"). We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a).

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Upon consideration of the Petition, the Preliminary Response, Reply, the Sur-Reply, and the evidence therein, we conclude the information presented does not show that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of the challenged claims of the '836 patent. Accordingly, we do not institute *inter partes* review of the '836 patent.

A. Related Proceedings

Petitioner states Patent Owner has asserted claims 1, 4, 7, 9–11, 13, 14, 17, 20, and 21 of the '836 patent in *VLSI Technology LLC v. Intel Corporation*, No. 5:17-cv-05671 (N.D. Cal. Oct. 2, 2017). Pet. 2.

B. The '836 Patent

The '836 patent is directed to a "multi-core system on a chip" in which a speed information for each core, such as the maximum operation speed (Fmax), is extracted and stored in a storage device, such as a device control registry. Ex. 1001 [57]. The information may be "accessed and used by the operating system when allocating workload among the cores by selecting the fast[est] core . . . to run any applications or tasks that [cannot] be executed on a plurality of cores." *Id.*

C. Illustrative Claims

Claims 1, 10, and 20, which are the only challenged independent claims in this proceeding, are illustrative and reproduced below.[1]

1. A method for operating a multi-core processing device, comprising:

   [a] measuring a processing speed parameter for each of a plurality of cores;

   [b] storing each measured processing speed parameter for each of the plurality of cores in a storage device;

   [c] and upon identifying a processing task that can not be run across the plurality of cores, selecting a core from the plurality of cores having a fastest measured processing speed parameter at a given voltage to run the processing task.

10. A multi-core system on chip (SOC), comprising:

   [a] a plurality of cores, each core comprising a performance measurement circuit for measuring a performance parameter value for said core; and

[1] Bracketed material and formatting added for clarity and for consistency with usage by the parties.

[b] at least a first storage device for storing the performance parameter values for the plurality of cores

[c] for use in selecting a core having maximized or minimized performance parameter value at a specified voltage to run a processing task that can not be run across the plurality of cores.

20. In a multi-core processor comprising multiple cores which are controlled by system logic, a method for executing single core applications and multi-core applications comprising:

[a] measuring a maximum processing speed value for each of the multiple cores for at least a first operating voltage value;

[b] storing each measured maximum processing speed value for each of the multiple cores;

[c] running a multi-core application on a plurality of the multiple cores by controlling each of the plurality of the multiple cores to run at a speed which is identified from the stored maximum processing speed values to be the slowest maximum processing speed of the plurality of the multiple cores; and

[d] running a single core application on a single core which is identified from the stored maximum processing speed values for the multiple cores as being the fastest core upon identifying a processing task that cannot be run across the plurality of the multiple cores.

D. Asserted Grounds of Unpatentability

Relying upon the declaration testimony of David August, Ph.D., (Ex. 1002), Petitioner challenges claims 1–11, 13, 14, 17, 18, 20, and 21 of

the '836 patent based on the asserted grounds of unpatentability ("grounds") set forth in the table below.

References	Basis	Challenged Claim(s)
Jacobowitz,[2] Finkelstein,[3] and Bowman [4]	§ 103	1–11, 13, 14, 18, 20, and 21
Jacobowitz, Finkelstein, and Bowman, and Herbert [5]	§ 103	17

II. DISCUSSION

A. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in

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[2] U.S. Patent No. 7,917,758 B2, filed May 11, 2007, issued Mar. 29, 2011 (Ex. 1003, "Jacobowitz")
[3] U.S. Patent Application Publication No. 2010/0169609 A1, filed Dec. 30, 2008, published July 1, 2010 (Ex. 1004, "Finkelstein")
[4] Bowman et al., *Impact of Die-to-Die and Within-Die Parameter Variations on the Throughput Distribution of Multi-Core Processors*, ISLPED '07 Proceedings of the 2007 International Symposium on Low Power Electronics and Design, Aug. 27–29, 2007, pp. 50–55 (Ex. 1005, "Bowman").
[5] Herbert et al., *Analysis of Dynamic Voltage/Frequency Scaling in Chip-Multiprocessors*, ISLPED '07 Proceedings of the 2007 International Symposium on Low Power Electronics and Design, Aug. 27–29, 2007, pp. 38–43 (Ex. 1007, "Herbert").

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