UNITED STATES PATENT AND TRADEMARK OFFICE
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BEFORE THE PATENT TRIAL AND APPEAL BOARD
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MEDIATEK INC. and MEDIATEK USA INC., and
ARM LTD. and ARM, INC.,
Petitioners,

v.

ADVANCED MICRO DEVICES, INC. and ATI TECHNOLOGIES ULC,
Patent Owner.
_____

Case IPR2018-00102
Case IPR2018-01149[1]
Patent 7,633,506 B1

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Before JONI Y. CHANG, BRIAN J. McNAMARA, and
PAUL J. KORNICZKY, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and
37 C.F.R. § 42.73

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[1] IPR2018-00102 and IPR2018-01149 have been joined. All references in
this Decision are to Papers and Exhibits in IPR2018-00102, unless otherwise
noted.

BACKGROUND

On December 12, 2018, IPR2018-01149 was joined to this IPR2018-00102 in which a trial already had been instituted. *See ARM Ltd. and ARM Inc. v. Advanced Micro Devices, Inc. and ATI Techs., Inc.*, Case IPR2018-01140, slip op. (PTAB Dec. 12, 2018) (Paper 16, Decision to Institute and Grant of Motion For Joinder). "Petitioner" refers to MediaTek Inc., MediaTek USA Inc., ARM Ltd., and ARM, Inc., collectively. "Patent Owner" refers to Advanced Micro Devices, Inc. and ATI Technologies ULC collectively.

Inter Partes Review: On October 20, 2018, Petitioner filed a Petition ("Pet.") for *inter* partes review of claims 1–9 of U. S. Patent No. 7,633,506 B1 ("the '506 patent"). On April 27, 2018, in IPR2018-00102, we instituted an *inter partes* review of claims 1–9 of the '506 patent on all grounds asserted in the Petition. Paper 14 ("Dec. to Inst."). Patent Owner filed a Patent Owner Response. Paper 17 ("PO Resp."). Petitioner filed a Petitioner Reply. Paper 28 ("Pet. Reply"). Patent Owner filed a Sur-Reply. Paper 35 ("PO Sur-reply").

Motion to Amend: Patent Owner filed a Contingent Motion to Amend. Paper 18 ("Mot. To Amend"). Petitioner filed an Opposition to Patent Owner's Motion to Amend. Paper 29 ("Opp. To Mot. To Amend"). Patent Owner filed a Reply to Petitioner's Opposition to its Motion to Amend. Paper 34 ("Reply to Opp. To Mot. To Amend"). Petitioner filed a Sur-reply. Paper 41 ("Pet. Sur-Reply to Mot. To Amend").

Motion to Exclude Evidence: Patent Owner filed a Motion to Exclude Evidence. Paper 40 ("Mot. To Exclude"). Petitioner filed a Response. Paper 42 ("Resp. To Mot. To Exclude").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). A transcript of an oral hearing held on January 22, 2019, (Paper 47, "H'rg. Tr.") has been entered into the record.

Having reviewed the arguments of the parties and the supporting evidence, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims are unpatentable. We also deny Patent Owner's Motion to Amend.

THE '506 PATENT (EXHIBIT 1001)

According to the '506 patent, a three dimensional (3D) image typically is displayed on a two dimensional array of pixels using a plurality of graphical objects, such as points, lines, and polygons, known as primitives that are the basis of most rendering instructions. Ex. 1001, 1:45–50. Visible primitives that are part of a scene are drawn individually by determining those pixels falling within the edges of the primitives and obtaining attributes that correspond to each of the pixels to determine the displayed color value of the applicable pixels. *Id.* at 1:52–60. The final displayed color of an individual pixel may be a blend of colors from multiple surfaces or layers. *Id.* at 1:65–67. A blending function based on an opacity value associated with each pixel of each primitive can be used to blend colors of overlapping surfaces or layers when the top surface is not completely opaque. *Id*. at 1:61–65. 3D image data represents attributes such as color, opacity, texture, depth, and perspective information. *Id*. at 2:5–6. Graphics processing is the execution of draw commands that may include X and Y coordinates for the vertices of the primitive, as well as attribute parameters

for the primitive (color and depth or "Z" data) to generate a display image. *Id.* at 2:6–11.

According to the '506 patent, a graphics chip designed to carry out instruction processing to render graphics on a screen typically has a front-end and a back-end. Ex. 1001, 2:19–20. The front-end receives graphics instructions and generates geometry defining primitives or combinations of primitives that are processed by the back-end, where they might be textured, shaded, colored, or otherwise prepared for final output. *Id.* at 2:20–26. When back-end processing of primitives is complete, each pixel in the screen has a specific number value that defines a unique color attribute the pixel will have when drawn. *Id.* at 2:26–29. That final value is kept in a frame buffer for use at an appropriate time. *Id.* at 2:29–31. Systems have become more complex to accommodate three-dimensional (3D) data, requiring a 256-bit system that processes 512 bits in a single logic cycle. *Id.* at 2:32–40. The use of data words with a 256-bit frame buffer is a challenge for the input/output (I/O) system used by the graphics processing back-end because granularity may be too coarse. *Id.* at 2:40–45.

In the '506 patent, geometry representative data presented to the back-end of the graphics chip is divided into data words and provided to one or more parallel pipelines. *Id.* at 2:55–60. The display screen is divided into tiles and a portion of the display screen defined by one or more tiles is serviced by a pipeline. *Id.* at 2:60–64, Fig. 3. Work is allocated to pipelines based on a repeating square pixel tile pattern. *Id.* 5:23–25. The tiling pattern is based on the number of active pipelines. *Id.* at 5:50–51. As shown in Figure 5, logic 520 in set-up unit 515 intersects graphics primitives with the repeating tile pattern, such that a primitive is sent to a pipeline only

if it is likely to result in generation of covered pixels. *Id.* at 5:25–28. Set-up unit 515 creates a bounding box based on X, Y coordinates for each vertex of a polygon and the bounding box is compared to the tile pattern and mapped to one or more pipelines. *Id.* at 5:51–67.

Each parallel pipeline comprises a raster back-end having (i) a scan converter to step through the geometric patterns passed to the back end, (ii) a "hierarchical-Z" component to define the borders of the geometry more precisely, (iii) a "Z-buffer" for performing three dimensional operations of the data, (iv) a rasterizer for computing texture addresses and color components for a pixel, (v) a unified shader for combining multiple characteristics for a pixel and outputting a single value, and (vi) a color buffer logic unit for taking the incoming shader color and blending it into the frame buffer using the current frame buffer blend operations. *Id*. at 2:65–3:8, Fig. 5.

ILLUSTRATIVE CLAIM

Claim 1, with claim element designations used in the Petition shown in brackets, is reproduced below:

> 1. [preamble] A graphics chip comprising:
>> [a] a front-end in the graphics chip configured to receive one or more graphics instructions and to output a geometry;
>> [b] a back-end in the graphics chip configured to receive said geometry and to process said geometry into one or more final pixels to be placed in a frame buffer;
>> [c] wherein said back-end in the graphics chip comprises multiple parallel pipelines;
>> [d] wherein said geometry is determined to locate in a portion of an output screen defined by a tile; and
>> [e] wherein each of said parallel pipelines further comprises a unified shader that is programmable to perform both color shading and texture shading.

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