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Paper 27
Entered: January 6, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

IPR2018-01249
Patent 7,693,002 B2

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and SCOTT B. HOWARD, *Administrative Patent Judges.*

GALLIGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
Granting Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, Apple Inc. ("Petitioner") challenges the patentability of claims 1–28 and 31–37 of U.S. Patent No. 7,693,002 B2 ("the '002 patent," Ex. 1001), which is assigned to Qualcomm Incorporated ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 1–28 and 31–37 of the '002 patent are unpatentable. *See* 35 U.S.C. § 316(e) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

On June 18, 2018, Petitioner requested *inter partes* review of claims 1–28 and 31–37 of the '002 patent on the following grounds:

Claims Challenged	35 U.S.C. §[1]	Reference(s)
1–28, 31–37	103(a)	Sato[2]
1–17, 20–28, 31–36	103(a)	Asano,[3] Itoh[4]

[1] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. §§ 103 and 112 that became effective after the filing of the application for the '002 patent. Therefore, we apply the pre-AIA versions of these sections.
[2] US 4,951,259, issued Aug. 21, 1990 (Ex. 1005).
[3] US 2006/0098520 A1, published May 11, 2006 (Ex. 1006).
[4] Kiyoo Itoh, *VLSI Memory Chip Design*, (2001) (Ex. 1007).

Paper 2 ("Pet."). Patent Owner did not file a Preliminary Response. We instituted trial on all grounds of unpatentability. Paper 6 ("Dec. on Inst."), 18.

During the trial, Patent Owner filed a Response (Paper 11, "PO Resp."), Petitioner filed a Reply (Paper 15, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 17, "PO Sur-reply").

Petitioner filed a Motion to Exclude Exhibit 2004 (Paper 19), to which Patent Owner filed an Opposition (Paper 21), and in support of which Petitioner filed a Reply (Paper 23).

An oral hearing was held on October 10, 2019, a transcript of which appears in the record. Paper 26 ("Tr.").

B. The '002 Patent and Illustrative Claim

The '002 patent generally relates to wordline drivers and decoders for memory arrays. Ex. 1001, code (57), 1:7–9. Figure 1 of the '002 patent is reproduced below.

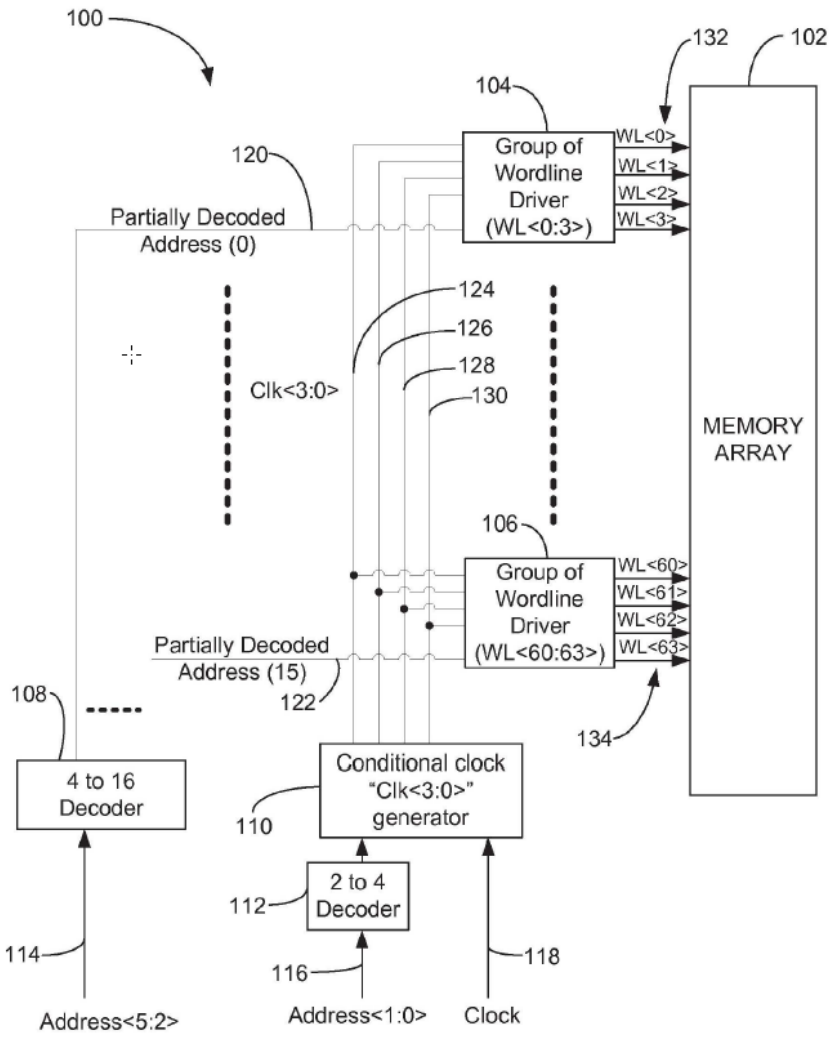

FIG. 1

Figure 1 is a block diagram of an embodiment of a wordline driver system 100. Ex. 1001, 2:31–34. Figure 1 shows groups of wordline drivers 104 and 106 that control particular wordlines in memory array 102. *Id.* at 2:53–3:8. Group of wordline drivers 104 drives wordlines WL<0> through WL<3>, and group of wordline drivers 106 drives wordlines WL<60> through WL<63>. *Id.* Additional wordline drivers that are not shown control the wordlines between WL<3> and WL<60>. *Id.* at 3:4–8.

In operation, two-to-four bit decoder 112 decodes the first portion (such as bits 0 and 1) of a six-bit memory address, and four-to-sixteen bit decoder decodes the remaining portion of the address (bits 2 through 5). Ex. 1001, 3:9–25. Based on the decoded first portion of the address received from decoder 112, conditional clock generator 110 "selectively applies the clock signal to a selected one of the clock outputs 124, 126, 128 and 130," each of which is coupled to a particular wordline driver in each group of wordline drivers. *Id.* at 3:26–34. "The four-to-sixteen bit memory address decoder 108 decodes the remainder of the six-bit memory address (e.g. bits two to five) and applies a partial address input to the wordlines that are related to the decoded memory address." *Id.* at 3:37–40. For example, if the partially-decoded address indicates that the first group of wordlines is addressed (WL<0> through WL<3>), decoder 108 applies a signal to address line 120, which, as shown in Figure 1, connects to group of wordline drivers 104. Ex. 1001, 3:41–67. The '002 patent explains that "the decoded output of the two-to-four decoder 112 with clock generator 110 and the decoded output of the four-to-sixteen bit memory address decoder 108 may be utilized via a logical AND operation to selectively activate a wordline driver of the group of wordline drivers 104." *Id.* at 4:3–8.

Of the challenged claims, claims 1, 7, 11, 17, 21, and 23–27 are independent. Claim 1, reproduced below, is illustrative.

> 1. A circuit device comprising:
>
> first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

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