UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD
SAMSUNG ELECTRONICS CO., LTD. AND SAMSUNG ELECTRONICS AMERICA, INC. Petitioner
v.
INVENSAS CORPORATION Patent Owner
U.S. Patent No. 6,054,336

PETITION FOR INTER PARTES REVIEW **OF U.S. PATENT NO. 6,054,336** 



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1002	Declaration of Dr. Miltiadis Hatalis
1003	Curriculum Vitae for Dr. Miltiadis Hatalis
1004	Prosecution File History of U.S. Patent No. 6,054,336
1005	U.S. Patent No. 5,847,460 ("Liou")
1006	U.S. Patent No. 5,428,231 ("Tanaka")
1007	Nakamura et al., "A Single-Layer Metal-Electrode CCD Image
	Sensor," Digest of technical papers of the 1995 IEEE
	International Solid-State Circuits Conference, pp. 222-223.
1008	Ben G. Streetman, Solid State Electronic Devices (Prentice Hall
	1995)
1009	Ted Kamins, Polycrystalline Silicon for Integrated Circuit
	Applications (Springer 1988)
1010	W. Maly, Atlas of IC technologies: An Introduction to VLSI
	Processes (Benjamin/Cummings 1987)
1011	Sorab K. Ghandhi, VLSI Fabrication Principles (Wiley 1983)



#### I. INTRODUCTION

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively "Samsung") request *inter partes* review ("IPR") of Claims 1-3 of U.S. Patent No. 6,054,336 ("the '336 Patent"; Ex-1001), assigned to Invensas Corporation ("Patent Owner").

The '336 Patent claims a semiconductor fabrication process that uses "spacers" to form conductor patterns having dimensions smaller than those that can be formed using lithography and masks. Ex-1001, Claim 1. During prosecution, the applicant argued that Claim 1's combination of steps — including forming spacers by etching "auxiliary windows" in a "first dielectric layer," adding a "second layer," "anisotropic etching of this second layer" to form spacers, and then using the spacers to form "very narrow conductor tracks" — taught over the prior art cited by the Examiner. Ex-1004, 65-72. The Examiner accepted these arguments and allowed the claims. *Id.*, 73-76.

However, the '336 Patent's combination of steps for using spacers to create conductive patterns with small dimensions was known before the '336 Patent's priority date of May 29, 1997. For example, these steps were disclosed in prior art



<sup>&</sup>lt;sup>1</sup> All citations to Ex-1004 are to the repaginated page numbers applied to the File History by Samsung.

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