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Paper 15
Entered: April 11, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

Case IPR2018-01296
Patent 7,675,806 B2

Before ROBERT J. WEINSCHENK, MINN CHUNG, and KIMBERLY McGRAW, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 11, 12, 13, 15, and 17 (the "challenged claims") of U.S. Patent No. 7,675,806 B2 (Ex. 1101, "the '806 patent"). VLSI Technology LLC ("Patent Owner") filed a Preliminary Response (Paper 14, "Prelim. Resp.").

By statute, institution of an *inter partes* review may not be authorized unless "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Upon consideration of the Petition and the Preliminary Response, we conclude that the information presented does not show there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of any challenged claim of the '806 patent. Accordingly, we do not institute an *inter partes* review.

II. BACKGROUND

A. Related Matters

The parties indicate that the '806 patent is the subject of the following district court litigation: *VLSI Technology LLC v. Intel Corporation*, No. 5:17-cv-05671 (N.D. Cal. Oct. 2, 2017). Pet. 2; Paper 6, 2.

The '806 patent is also the subject of petitions for *inter partes* review filed by Petitioner in IPR2018-01034 and IPR2019-00034.[1]

[1] The petition in IPR2018-01034 has been dismissed at the request of Petitioner. IPR2018-01034, Paper 11 (Decision Granting Petitioner's Unopposed Motion to Dismiss).

B. The '806 Patent

The '806 patent describes a low-voltage memory device in an integrated circuit. Ex. 1101, [57]. Figure 1 of the '806 patent is reproduced below.

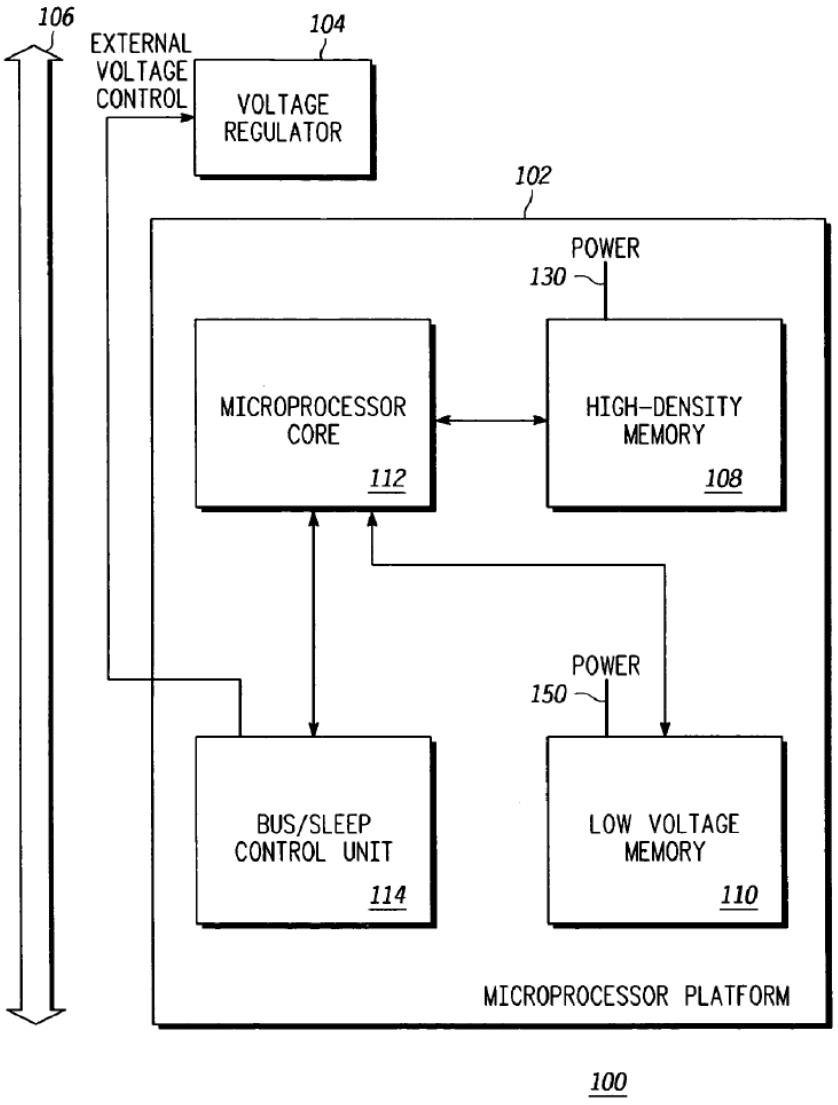

FIG. 1

Figure 1 is a block diagram of an exemplary system including a memory device. *Id.* at 1:40–41. As shown in Figure 1, integrated circuit 102 comprises microprocessor core 112, first memory 108, and

second memory 110. *Id.* at 3:9–10. Integrated circuit 102 also includes bus interface unit and sleep control unit 114. *Id.* at 3:10–11.

As illustrated in Figure 1, integrated circuit 102 is connected to external bus 106. *Id.* at 2:7–8. During operation, integrated circuit 102 can communicate with external devices via external bus 106. *Id.* at 2:15–16. In an embodiment, integrated circuit 102 may be incorporated in a multi-core device or system such that integrated circuit 102 is accessible to external microprocessor cores (not shown) via external bus 106. *Id.* at 2:16–20.

As also depicted in Figure 1, bus interface unit and sleep control unit 114 of integrated circuit 102 is connected to voltage regulator 104 to provide a voltage control signal. *Id.* at 3:14–17. Voltage regulator 104 regulates the voltages supplied to integrated circuit 102, which can operate in an active mode or low-voltage mode of operation. *Id.* at 2:21–23. According to the ’806 patent, integrated circuit 102 operates with less power in the low-voltage mode than in the active mode of operation, albeit with reduced functionality. *Id.* at 2:30–32.

To enter the low-voltage mode of operation, integrated circuit 102 instructs voltage regulator 104 to reduce the voltage supplied to integrated circuit 102 below the minimum operating voltage for certain portions of integrated circuit 102. *Id.* at 2:56–60. In an embodiment, first memory 108 has a minimum operating voltage, which is the lowest voltage at which first memory 108 can reliably respond to read and write operations. *Id.* at 3:44–47. If the voltage supplied to first memory 108 is below its minimum operating voltage, first memory 108 is effectively inaccessible to microprocessor core 112 and other devices. *Id.* at 3:47–50. According to the ’806 patent, first memory 108 also has a retention voltage, which is a

voltage at which the memory can still retain stored data when the voltage is lowered below the minimum operating voltage. *Id.* at 3:50–56. In other words, first memory 108 can retain data stored in the memory when the voltage supplied to first memory 108 is below the minimum operating voltage but above or at the retention voltage. *Id.*

The '806 patent describes that second memory 110 is a low-voltage memory that operates at a lower voltage than first memory 108. *Id.* at 3:57–58. In an embodiment, the minimum operating voltage for second memory 110 is lower than the minimum operating voltage for first memory 108, but higher than the retention voltage for first memory 108. *Id.* at 3:61–64.

According to the '806 patent, in the active mode of operation, the voltage supplied to first memory 108 and second memory 110 is sufficiently high to allow read and write operations on both memories. *Id.* at 4:28–31. In the low-voltage mode of operation, the voltage supplied to first memory 108 is reduced below the first memory's minimum operating voltage, but the voltage supplied to second memory 110 is maintained above the minimum operating voltage for the second memory, such that second memory 110 remains accessible, although first memory 108 is inaccessible. *Id.* at 4:32–40. Thus, devices connected to external bus 106 can continue to access second memory 110 during the low-voltage mode of operation, which can reduce the number of times integrated circuit 102 needs to exit the low-voltage mode of operation, resulting in reduced power consumption. *Id.* at 4:40–45.

The '806 patent describes that first memory 108 has a relatively high-density memory topology compared to second memory 110 and that

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