

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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INTEL CORPORATION,  
Petitioner,

v.

QUALCOMM INCORPORATED,  
Patent Owner.

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IPR2018-01334  
U.S. Patent No. 8,838,949

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**PETITIONER'S OPENING BRIEF ON REMAND<sup>1</sup>**

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<sup>1</sup> IPR2018-01335 and IPR2018-01336 have been consolidated with IPR2018-01334, and Petitioner will file this brief only in IPR2018-01334. All citations are to IPR2018-01334 unless otherwise noted.

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## I. INTRODUCTION

This consolidated *Inter Partes Review* proceeding is before the Board on remand from the Federal Circuit. In its Final Written Decision, the Board found claims 10, 11, 13-15, and 18-23 of U.S. Patent No. 8,838,949 (“the ’949 patent”) obvious but held that Petitioner had not proven by a preponderance of the evidence that claims 1-9, 12, 16, and 17 were unpatentable. The Board found that “hardware buffer” ““should not be read so broadly as to encompass’ the use of a temporary buffer” (FWD (Paper 30) at 17) and claims 1-9 and 12 were not obvious under that negative construction. The Board also declined to determine whether there was structure corresponding to the mean-plus-function terms of claims 16 and 17. Instead, it found that Petitioner failed to carry its burden of providing adequate evidence of the corresponding structure.

On appeal, the Federal Circuit remanded, instructing the Board to properly construe “hardware buffer,” determine whether claims 1-9 and 12 are obvious under that construction, and determine whether the Board can resolve the prior art challenge to the patentability of claims 16 and 17 despite the potential indefiniteness of the means-plus-function terms or whether the terms are indefinite and it is impossible to adjudicate the prior art challenge on its merits. Petitioner asks the Board to (1) adopt its proposed claim construction for “hardware buffer”; (2) hold claims 1-9 and 12 unpatentable under this construction; and (3) find claims 16 and 17

obvious and/or indefinite.

## II. STATEMENT OF FACTS AND PROCEDURAL HISTORY

In July 2018, Petitioner filed these Petitions challenging all claims of the '949 patent as unpatentable under 35 U.S.C. § 103 based on four references, two of which are discussed here: Bauer (Ex. 1009) and Svensson (Ex. 1010).

The '949 patent claims to solve certain inefficiencies in prior art multi-processor systems by allowing data to be loaded to a secondary processor's system memory without copying the entire software image from a buffer. Ex. 1001 ('949 patent) at 9:42-56. However, the system and methods of the '949 patent were routine and well-known in the prior art. Multi-processor systems and the direct transfer of data between processors were disclosed in multiple prior art references, some of which were not before the Patent Office during the original prosecution.

### A. "Hardware Buffer" Limitation

Petitioner did not originally propose a claim construction for the term "hardware buffer," but argued that the "intermediate storage area" ("ISA") in Bauer and Svensson is a "hardware buffer" under the term's plain meaning and the broadest reasonable interpretation standard that applies here. *See* Petition (Paper 3) at 26-27; IPR2018-01335 Petition (Paper 3) at 61-62. In its Institution Decision, the Board agreed that Bauer and Svensson's ISA is a "hardware buffer" because "[t]he intermediate storage area of Bauer and Svensson is a buffer used to store data destined for another

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