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QUALCOMM INCORPORATED 5775 MOREHOUSE DR. SAN DIEGO, CA 92121			ELAMIN, ABDELMONIEM I	
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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-24 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Svensson, International Publication No. WO 2006/077068 A2 (cited by Applicant).

3. Claims 1, 3, 7-8, 19, 21, Svensson teaches a secondary processor [*client processor 104*] comprising system memory [*DSPXRAM 110*] and a hardware buffer [*An intermediate storage area is defined within the memory 108*] for receiving at a least a portion of an executable software image [*this reserved block of memory is used for intermediate storage of information (code and/or data) to be transferred to the slave- private memory, see page 7, lines 5-8. On receipt of the slave's information, the second stage of the host boot loader fills the intermediate storage area with information (code and/or data) to be loaded into the slave's invisible memory (Step 216) page7, lines25-27*], the secondary processor comprising a scatter loader controller for loading the executable software image directly from the hardware buffer to the system memory [*The slave copies the contents of the intermediate storage area to appropriate locations in its slave-private memory (Step 220), thereby implementing its actual loading, see page 7, last line - page 8, line 2*];

a primary processor [*host processor102*] coupled with a memory [*non-volatile memory 106*], the memory storing the executable software image for the secondary processor [*This*

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can be inferred from The first stage resets and holds the slave 104 in the reset state (Step 202) and pushes information (program instructions and/or data) (Step 204) in the usual way from the non-volatile memory 106 into the commonly visible memories 108, see page 5, lines 23-26]; and

an interface communicatively coupling the primary processor and the secondary processor via which the executable software image is received by the secondary processor [*The arrows in FIG. 1 indicate access paths, e.g., busses and DMA paths, between the CPUs and the memories. The ARM host CPU 102 can access the non-volatile memory 106 and the SARAM and DARAM 108 of the DSP, but not the DSP's XRAM 110, and the DSP slave CPU 104 can access all of the RAMs 108, 110, see page 5, lines 8-12].*

4. Claim 2, Svensson teaches the scatter loader controller is configured to load the executable software image directly from the hardware buffer to the system memory of the secondary processor without copying data between system memory locations on the secondary processor [*there is no indication that data is copied between system memory locations on the secondary processor when loading the executable software image from the hardware buffer to the system memory of the secondary processor].*

5. Claims 4-6, Svensson teaches the executable software image comprises an image header and at least one data segment [*Fig. 3, it is clear that the executable software image comprises an image header and at least one segment].*

6. Claim 9, Svensson teaches the portion of the executable software image is loaded into the system memory of the secondm₅ processor without an entire executable software image being stored in the hardware buffer [*This also means that a block should be split if it is larger than the*

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remaining part of the intermediate storage area, and one part transferred to the intermediate storage area with the remaining part transferred in the next block. Moreover, if a block is several times larger than the intermediate storage area, it may have to be split more than once, see page 8, line 27]

7. Claims 10, 20, 22, Svensson teaches the multi-processor system is integrated into a computer [*This invention relates to initialization of electronic systems having multiple programmable processors, see page 1, line 4*].

8. Claims 11, 14-15, 17, 23, Svensson teaches receiving at a secondary processor [*client processor 104*], from a primary processor [*host processor 102*] via an inter- chip communication bus [*The arrows in FIG. 1 indicate access paths, e.g., busses and DMA paths, between the CPUs and the memories. The ARM host CPU 102 can access the non-volatile memory 106 and the SARAM and DARAM 108 of the DSP, but not the DSP's XRAM 110, and the DSP slave CPU 104 can access all of the RAMs 108, 110, see page 5, lines 8-12*], an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment [*A block of code and/or data to be transferred into the intermediate storage area includes a header*];

processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store the at least one data segment [*that indicates the length of the block and where it is to be loaded in the slave memory, i.e., the destination address, see page 8, lines 15-18*];

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