UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Intel Corporation
Petitioner

v.

QUALCOMM INCORPORATED
Patent Owner

Trial No. IPR2018-01334[1]

U.S. Patent No. 8,838,949

PETITIONER'S DEMONSTRATIVE EXHIBITS ON REMAND

[1] IPR2018-01335 and IPR2018-01336 have been consolidated with the instant proceeding.

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United States Patent and Trademark Office
Before the Patent Trial and Appeal Board

Intel Corporation, Petitioner,
v.
Qualcomm Incorporated, Patent Owner

Case No: IPR2018-01334

(Consolidated with IPR2018-01335, -01336)

Petitioner's Demonstrative Exhibits on Remand

***Inter Partes Review* of U.S. Patent No. 8,838,949 on Remand**

August 4, 2022

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

verview

Overview of the ’949 Patent

Overview of the Prior Art

Disputed Issues

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Overview of the '949 Patent

Overview of the Prior Art

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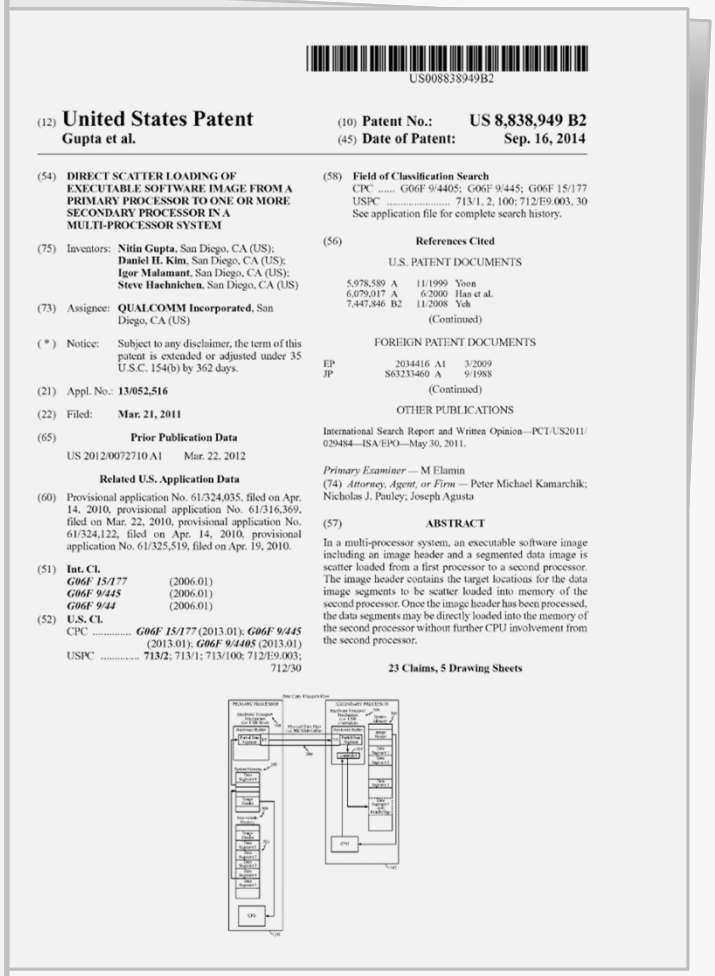
49 Patent



US008838949B2

(12) **United States Patent**
Gupta et al.

(10) **Patent No.: US 8,838,949 B2**
(45) **Date of Patent: Sep. 16, 2014**

(54) **DIRECT SCATTER LOADING OF EXECUTABLE SOFTWARE IMAGE FROM A PRIMARY PROCESSOR TO ONE OR MORE SECONDARY PROCESSOR IN A MULTI-PROCESSOR SYSTEM**

(75) Inventors: **Nitin Gupta**, San Diego, CA (US); **Daniel H. Kim**, San Diego, CA (US); **Igor Malamant**, San Diego, CA (US); **Steve Haehnichen**, San Diego, CA (US)

(73) Assignee: **QUALCOMM Incorporated**, San Diego, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 362 days.

(21) Appl. No.: **13/052,516**

(22) Filed: **Mar. 21, 2011**

(65) **Prior Publication Data**

US 2012/0072710 A1 Mar. 22, 2012

Related U.S. Application Data

(60) Provisional application No. 61/324,035, filed on Apr. 14, 2010, provisional application No. 61/316,369, filed on Mar. 22, 2010, provisional application No. 61/324,122, filed on Apr. 14, 2010, provisional application No. 61/325,519, filed on Apr. 19, 2010.

(51) **Int. Cl.**
G06F 15/177 (2006.01)
G06F 9/445 (2006.01)
G06F 9/44 (2006.01)

(52) **U.S. Cl.**
CPC ***G06F 15/177*** (2013.01); ***G06F 9/445*** (2013.01); ***G06F 9/4405*** (2013.01)
USPC **713/2**; 713/1; 713/100; 712/E9.003; 712/30

(58) **Field of Classification Search**
CPC G06F 9/4405; G06F 9/445; G06F 15/177
USPC 713/1, 2, 100; 712/E9.003, 30
See application file for complete search history.

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(57) **ABSTRACT**

In a multi-processor system, an executable software image including an image header and a segmented data image is scatter loaded from a first processor to a second processor. The image header contains the target locations for the data image segments to be scatter loaded into memory of the second processor. Once the image header has been processed, the data segments may be directly loaded into the memory of the second processor without further CPU involvement from the second processor.

23 Claims, 5 Drawing Sheets

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Accordingly, no extra memory copy operations occur in the secondary processor in the above aspect. Thus, conventional techniques employing a temporary buffer for the entire image, and the packet header handling, etc., are bypassed in favor of a more efficient direct loading process. Thus, the exemplary load process of FIG. **3** does not require the intermediate buffer operations traditionally required for loading a software image from a primary processor to a secondary processor. Instead of scatter loading from a temporary buffer holding the entire image, the exemplary load process of FIG. **3** allows for direct scatter load the image segments to their respective target destinations directly from the hardware to the system memory. Once the image header is processed, the executable image is directly scatter loaded into target memory, bypassing farther CPU involvement.

Op. Br. (Paper 35) at 2; -01334 Pet. at 9-15.

Ex. 1001 ('949 Patent) at cover page, 9:42-56.

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