DOCKET NO.: 0107131.00568US1
Filed on behalf of Intel Corporation
By:
David L. Cavanaugh, Reg. No. 36,476 (David.Cavanaugh@wilmerhale.com)
Thomas E. Anderson, Reg. No. 37,063 (Tom.Anderson@wilmerhale.com)
Joseph H. Haag, Reg. No. 42,612 (Joseph.Haag@wilmerhale.com)
Wilmer Cutler Pickering Hale and Dorr LLP
1875 Pennsylvania Avenue, N.W.
Washington, DC 20006
Tel: (202) 663-6000

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Intel Corporation
Petitioner

v.

QUALCOMM INCORPORATED
Patent Owner

Trial No. IPR2018-01334[1]

U.S. Patent No. 8,838,949

PETITIONER'S DEMONSTRATIVE EXHIBITS

[1] IPR2018-01335 and IPR2018-01336 have been consolidated with the instant proceeding.

United States Patent and Trademark Office
Before the Patent Trial and Appeal Board

Intel Corporation, Petitioner,
v.
Qualcomm Incorporated, Patent Owner

Case No: IPR2018-01334

(Consolidated with IPR2018-01335, -01336)

Petitioner's Demonstrative Exhibits

***Inter Partes Review* of U.S. Patent No. 8,838,949**

December 12, 2019

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

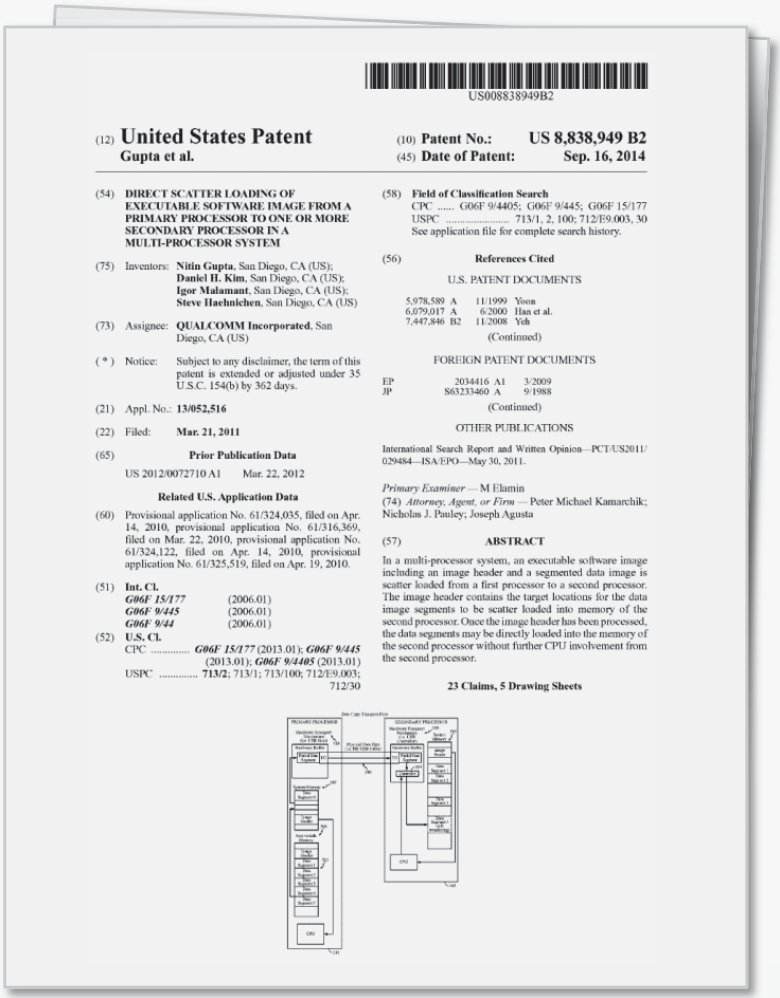
Overview

- Overview of the ’949 Patent
- Overview of the Prior Art
- Obviousness of the Challenged Claims
- Summary of the Proceeding
- Disputed Issues

Overview

- **Overview of the '949 Patent**
- Overview of the Prior Art
- Obviousness of the Challenged Claims
- Summary of the Proceeding
- Disputed Issues

’949 Patent



US008838949B2

(12) **United States Patent**
Gupta et al.

(10) **Patent No.: US 8,838,949 B2**
(45) **Date of Patent: Sep. 16, 2014**

(54) **DIRECT SCATTER LOADING OF EXECUTABLE SOFTWARE IMAGE FROM A PRIMARY PROCESSOR TO ONE OR MORE SECONDARY PROCESSOR IN A MULTI-PROCESSOR SYSTEM**

(75) Inventors: **Nitin Gupta**, San Diego, CA (US); **Daniel H. Kim**, San Diego, CA (US); **Igor Malamant**, San Diego, CA (US); **Steve Haehnichen**, San Diego, CA (US)

(73) Assignee: **QUALCOMM Incorporated**, San Diego, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 362 days.

(21) Appl. No.: **13/052,516**

(22) Filed: **Mar. 21, 2011**

(65) **Prior Publication Data**

US 2012/0072710 A1 Mar. 22, 2012

Related U.S. Application Data

(60) Provisional application No. 61/324,035, filed on Apr. 14, 2010, provisional application No. 61/316,369, filed on Mar. 22, 2010, provisional application No. 61/324,122, filed on Apr. 14, 2010, provisional application No. 61/325,519, filed on Apr. 19, 2010.

(51) **Int. Cl.**
G06F 15/177 (2006.01)
G06F 9/445 (2006.01)
G06F 9/44 (2006.01)

(52) **U.S. Cl.**
CPC ***G06F 15/177*** (2013.01); ***G06F 9/445*** (2013.01); ***G06F 9/4405*** (2013.01)
USPC **713/2**; 713/1; 713/100; 712/E9.003; 712/30

(58) **Field of Classification Search**
CPC G06F 9/4405; G06F 9/445; G06F 15/177
USPC 713/1, 2, 100; 712/E9.003, 30
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,978,589 A 11/1999 Yoon
6,079,017 A 6/2000 Han et al.
7,447,846 B2 11/2008 Yeh
(Continued)

FOREIGN PATENT DOCUMENTS

EP 2034416 A1 3/2009
JP S63233460 A 9/1988
(Continued)

OTHER PUBLICATIONS

International Search Report and Written Opinion—PCT/US2011/029484—ISA/EPO—May 30, 2011.

Primary Examiner — M Elamin
(74) *Attorney, Agent, or Firm* — Peter Michael Kamarchik; Nicholas J. Pauley; Joseph Agusta

(57) **ABSTRACT**

In a multi-processor system, an executable software image including an image header and a segmented data image is scatter loaded from a first processor to a second processor. The image header contains the target locations for the data image segments to be scatter loaded into memory of the second processor. Once the image header has been processed, the data segments may be directly loaded into the memory of the second processor without further CPU involvement from the second processor.

23 Claims, 5 Drawing Sheets

(10) **Patent No.: US 8,838,949 B2**
(45) **Date of Patent: Sep. 16, 2014**

(54) **DIRECT SCATTER LOADING OF EXECUTABLE SOFTWARE IMAGE FROM A PRIMARY PROCESSOR TO ONE OR MORE SECONDARY PROCESSOR IN A MULTI-PROCESSOR SYSTEM**

(57) **ABSTRACT**

In a multi-processor system, an executable software image including an image header and a segmented data image is scatter loaded from a first processor to a second processor. The image header contains the target locations for the data image segments to be scatter loaded into memory of the second processor. Once the image header has been processed, the data segments may be directly loaded into the memory of the second processor without further CPU involvement from the second processor.

Ex. 1001 (’949 Patent); -01334 Pet. at 9-15; Ex. 1002 (Lin Decl.) ¶¶ 53-59.

'949 Patent: Claim 1

Secondary Processor

System Memory & Hardware Buffer

Image header and each data segment received separately

Scatter Loader Controller

Primary Processor with Memory

Interface Between Primary & Secondary Processor

What is claimed is:

1. A multi-processor system comprising:

a secondary processor comprising:

system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image, the image header and each data segment being received separately, and

a scatter loader controller configured:

to load the image header; and

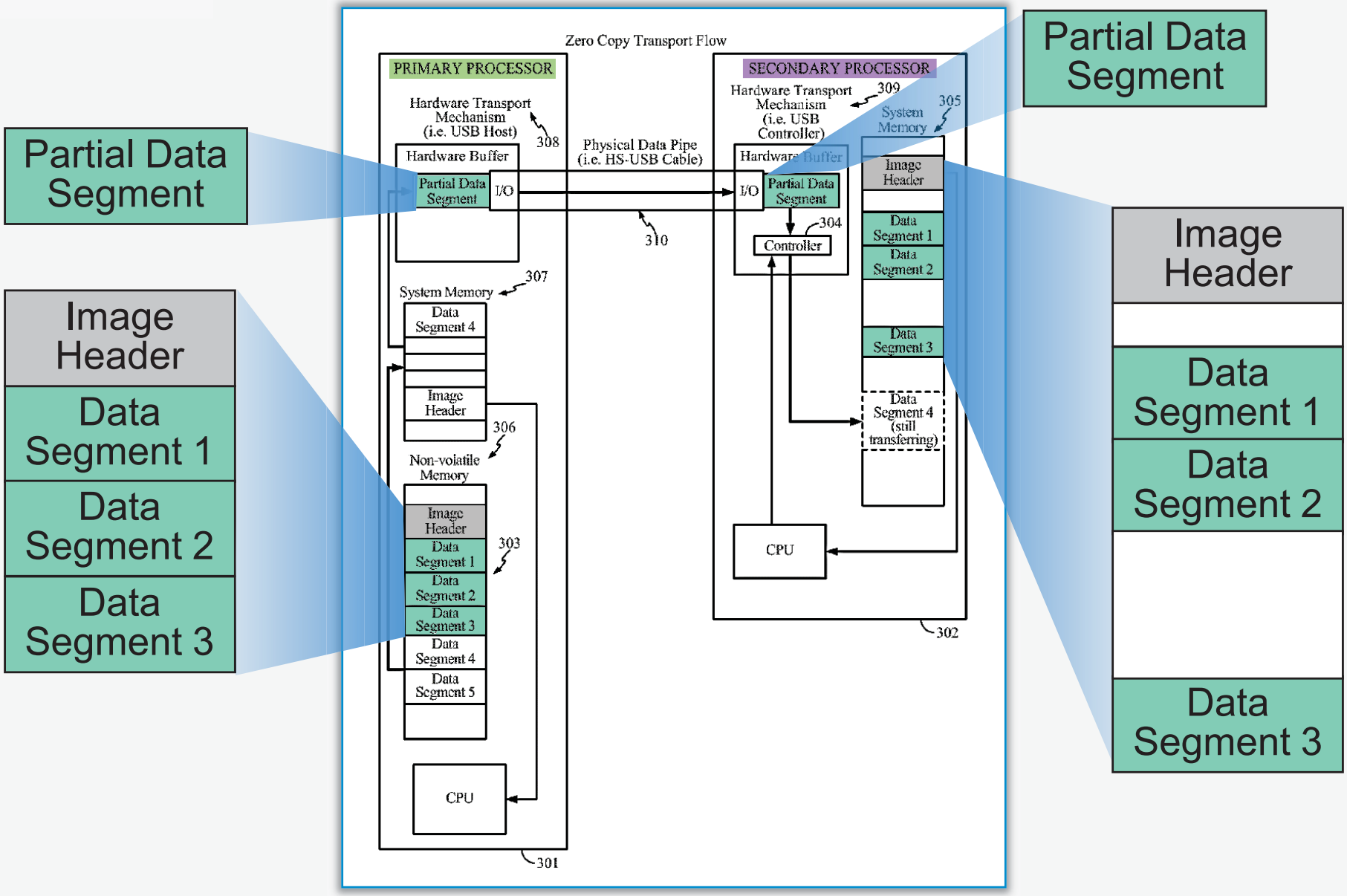
to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory;

a primary processor coupled with a memory, the memory storing the executable software image for the secondary processor; and

an interface communicatively coupling the primary processor and the secondary processor, the executable software image being received by the secondary processor via the interface.

Ex. 1001 ('949 Patent) at Claim 1 (highlighting and annotations added); -01334 Pet. at 25-52; Ex. 1002 (Lin Decl.) ¶¶ 107-155.

'949 Patent Alleged Invention:
Figure 3



-01334 Pet. at 12; Ex. 1002 (Lin Decl.) ¶¶ 59-67; Ex. 1001 ('949 Patent) at Fig. 3 (highlighting and annotations added).

'949 Patent: Challenged Claims

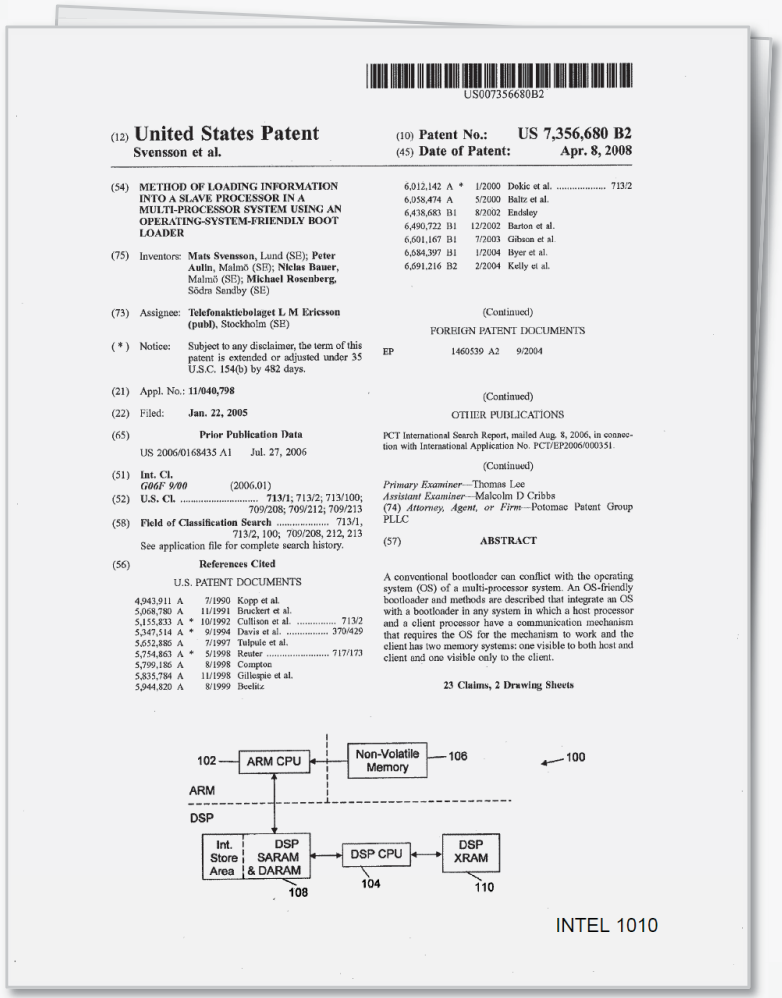
- Independent claims 1, 10, 16, 18, 20, and 22
  - Independent claims include multi-processor system (claims 1, 18, 20), method (claim 10, 22), and apparatus (claim 16)
  - All recite separately receiving an image header and a data segment and scatter loading each received data segment into system memory
  - Claim 16 uses "means for" terms
  - Claims 18 and 20 add well-known features such as a file system and a second non-volatile memory storing configuration parameters, which are not in dispute
- Dependent claims 2-9, 11-15, 17, 19, 21, 23

-01334 Pet.; -01335 Pet.; -01336 Pet.

Overview

- Overview of the '949 Patent
- **Overview of the Prior Art**
- Obviousness of the Challenged Claims
- Summary of the Proceeding
- Disputed Issues

U.S. 7,356,680 ("Svensson")



US007356680B2

(12) **United States Patent**
Svensson et al.

(10) **Patent No.: US 7,356,680 B2**
(45) **Date of Patent: Apr. 8, 2008**

(54) **METHOD OF LOADING INFORMATION INTO A SLAVE PROCESSOR IN A MULTI-PROCESSOR SYSTEM USING AN OPERATING-SYSTEM-FRIENDLY BOOT LOADER**

(75) Inventors: **Mats Svensson**, Lund (SE); **Peter Aulin**, Malmö (SE); **Niclas Bauer**, Malmö (SE); **Michael Rosenberg**, Södra Sandby (SE)

(73) Assignee: **Telefonaktiebolaget L M Ericsson (publ)**, Stockholm (SE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 482 days.

(21) Appl. No.: **11/040,798**

(22) Filed: **Jan. 22, 2005**

(65) **Prior Publication Data**

US 2006/0168435 A1 Jul. 27, 2006

(51) **Int. Cl.**
G06F 9/00 (2006.01)

(52) **U.S. Cl.** **713/1**; 713/2, 713/100; 709/208; 709/212; 709/213

(58) **Field of Classification Search** 713/1, 713/2, 100; 709/208, 212, 213
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,943,911	A	7/1990	Kopp et al.	
5,068,780	A	11/1991	Bruckert et al.	
5,155,833	A *	10/1992	Cullison et al.	713/2
5,347,514	A *	9/1994	Davis et al.	370/429
5,652,885	A	7/1997	Tulpule et al.	
5,754,863	A *	5/1998	Reuter	717/173
5,799,186	A	8/1998	Compton	
5,835,784	A	11/1998	Gillespie et al.	
5,944,820	A	8/1999	Beelitz	
6,012,142	A *	1/2000	Dokic et al.	713/2
6,058,474	A	5/2000	Baltz et al.	
6,438,683	B1	8/2002	Endsley	
6,490,722	B1	12/2002	Barton et al.	
6,501,167	B1	7/2003	Gibson et al.	
6,584,397	B1	1/2004	Byer et al.	
6,591,216	B2	2/2004	Kelly et al.	

(Continued)

FOREIGN PATENT DOCUMENTS

EP	1460539	A2	9/2004

(Continued)

OTHER PUBLICATIONS

PCT International Search Report, mailed Aug. 8, 2006, in connection with International Application No. PCT/EP2006/000351.

(Continued)

Primary Examiner—Thomas Lee
Assistant Examiner—Malcolm D Cribbs
(74) *Attorney, Agent, or Firm*—Potomac Patent Group PLLC

(57) **ABSTRACT**

A conventional bootloader can conflict with the operating system (OS) of a multi-processor system. An OS-friendly bootloader and methods are described that integrate an OS with a bootloader in any system in which a host processor and a client processor have a communication mechanism that requires the OS for the mechanism to work and the client has two memory systems: one visible to both host and client and one visible only to the client.

23 Claims, 2 Drawing Sheets

INTEL 1010

(10) **Patent No.: US 7,356,680 B2**
(45) **Date of Patent: Apr. 8, 2008**

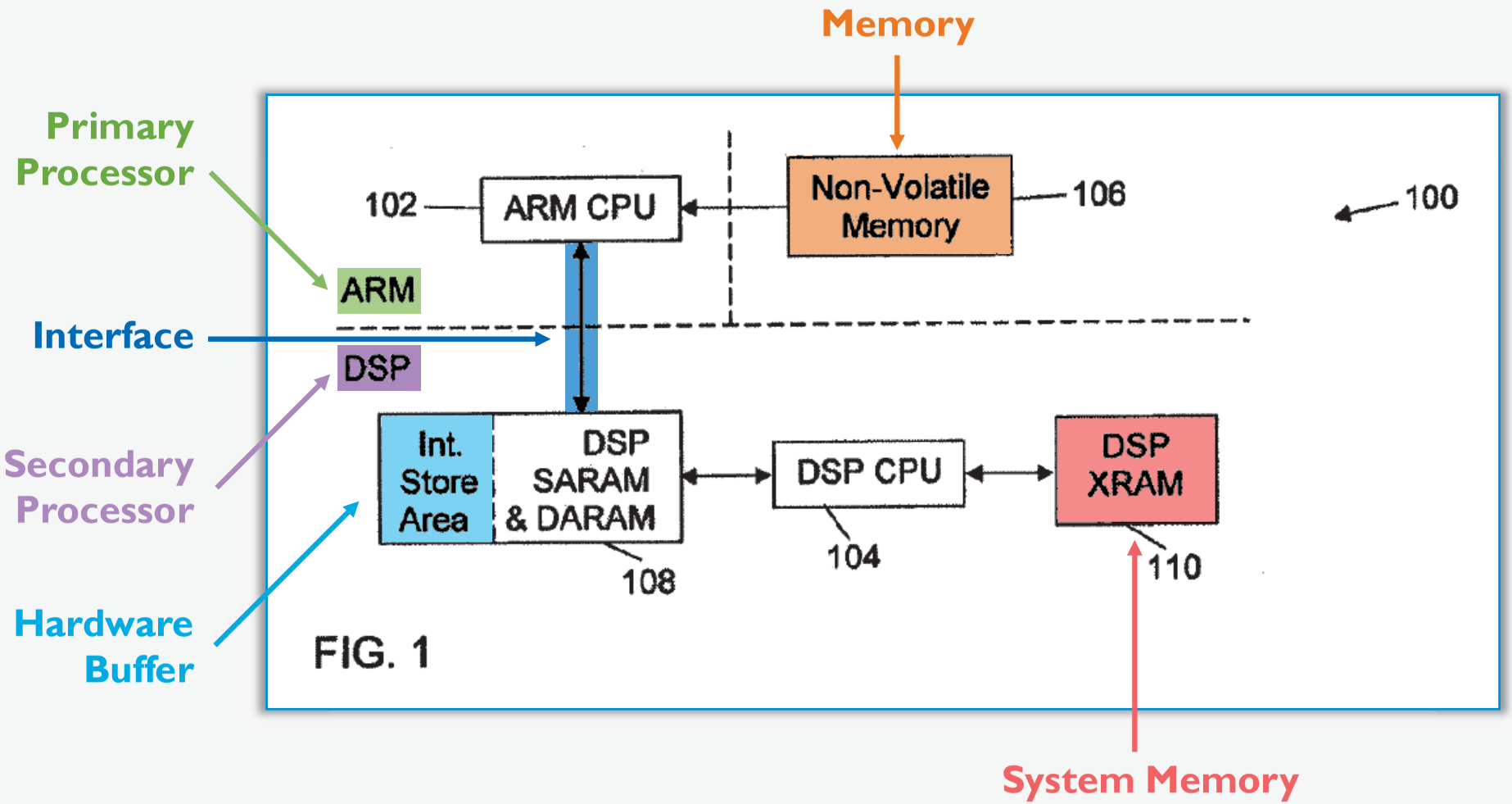
(54) **METHOD OF LOADING INFORMATION INTO A SLAVE PROCESSOR IN A MULTI-PROCESSOR SYSTEM USING AN OPERATING-SYSTEM-FRIENDLY BOOT LOADER**

(57) **ABSTRACT**

A conventional bootloader can conflict with the operating system (OS) of a multi-processor system. An OS-friendly bootloader and methods are described that integrate an OS with a bootloader in any system in which a host processor and a client processor have a communication mechanism that requires the OS for the mechanism to work and the client has two memory systems: one visible to both host and client and one visible only to the client.

Ex. 1010 (Svensson); -01334 Pet. at 17-19.

Svensson: Primary & Secondary Processors, Hardware Buffer & System Memory



Ex. 1010 (Svensson) at Fig. 1 (highlighting and annotations added); -01334 Pet. at 17-19, 25-27, 50-52.

Svensson:
Header with Destination Address

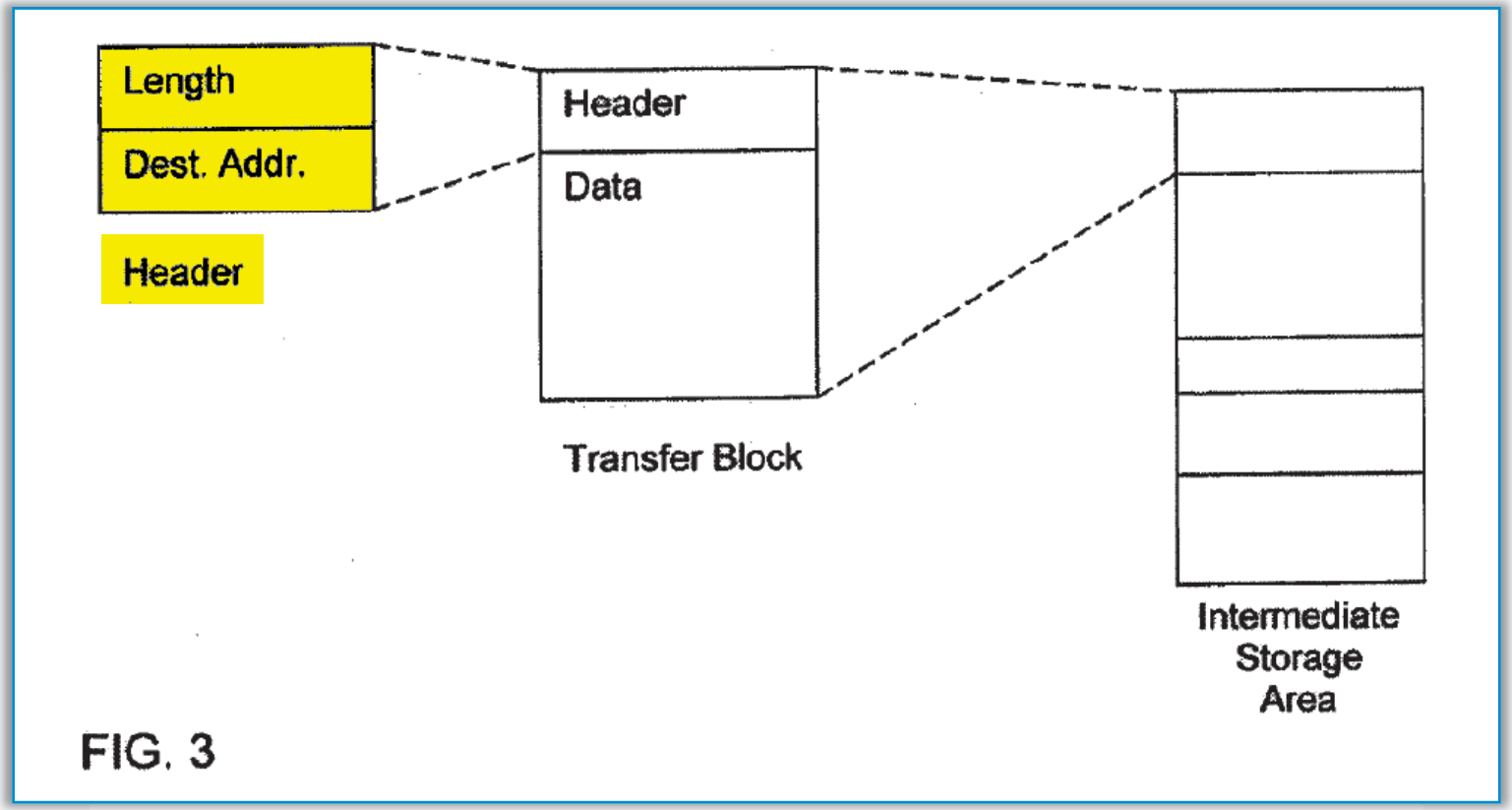
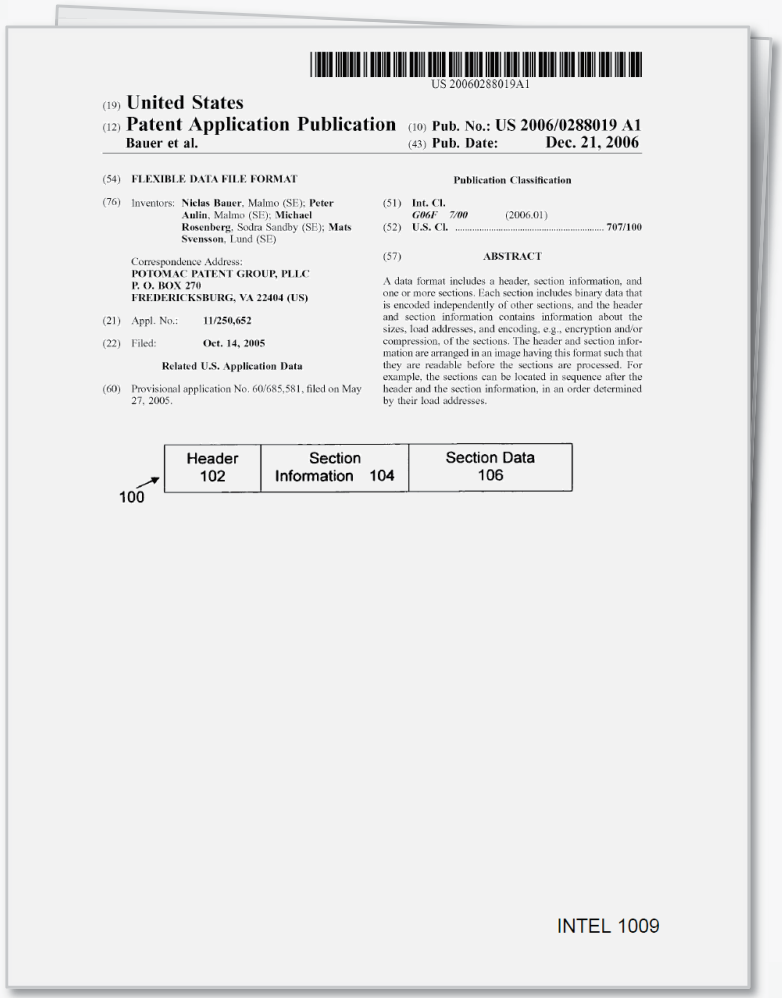


FIG. 3

Ex. 1010 (Svensson) at Fig. 3 (highlighting added); -01334 Pet. at 19.

U.S. 2006/0288019 ("Bauer")



US 20060288019A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0288019 A1**

Bauer et al. (43) **Pub. Date: Dec. 21, 2006**

(54) **FLEXIBLE DATA FILE FORMAT**

(76) Inventors: **Niclas Bauer**, Malmo (SE); **Peter Aulin**, Malmo (SE); **Michael Rosenberg**, Sodra Sandby (SE); **Mats Svensson**, Lund (SE)

Correspondence Address:
POTOMAC PATENT GROUP, PLLC
P. O. BOX 270
FREDERICKSBURG, VA 22404 (US)

(21) Appl. No.: **11/250,652**

(22) Filed: **Oct. 14, 2005**

Related U.S. Application Data

(60) Provisional application No. 60/685,581, filed on May 27, 2005.

Publication Classification

(51) **Int. Cl.**
G06F 7/00 (2006.01)

(52) **U.S. Cl.** **707/100**

(57) **ABSTRACT**

A data format includes a header, section information, and one or more sections. Each section includes binary data that is encoded independently of other sections, and the header and section information contains information about the sizes, load addresses, and encoding, e.g., encryption and/or compression, of the sections. The header and section information are arranged in an image having this format such that they are readable before the sections are processed. For example, the sections can be located in sequence after the header and the section information, in an order determined by their load addresses.

INTEL 1009

(10) **Pub. No.: US 2006/0288019 A1**

(43) **Pub. Date: Dec. 21, 2006**

(54) **FLEXIBLE DATA FILE FORMAT**

(57) **ABSTRACT**

A data format includes a header, section information, and one or more sections. Each section includes binary data that is encoded independently of other sections, and the header and section information contains information about the sizes, load addresses, and encoding, e.g., encryption and/or compression, of the sections. The header and section information are arranged in an image having this format such that they are readable before the sections are processed. For example, the sections can be located in sequence after the header and the section information, in an order determined by their load addresses.

Ex. 1009 (Bauer); -01334 Pet. at 19-21.

Bauer:
Same Multi-Processor System as Svensson

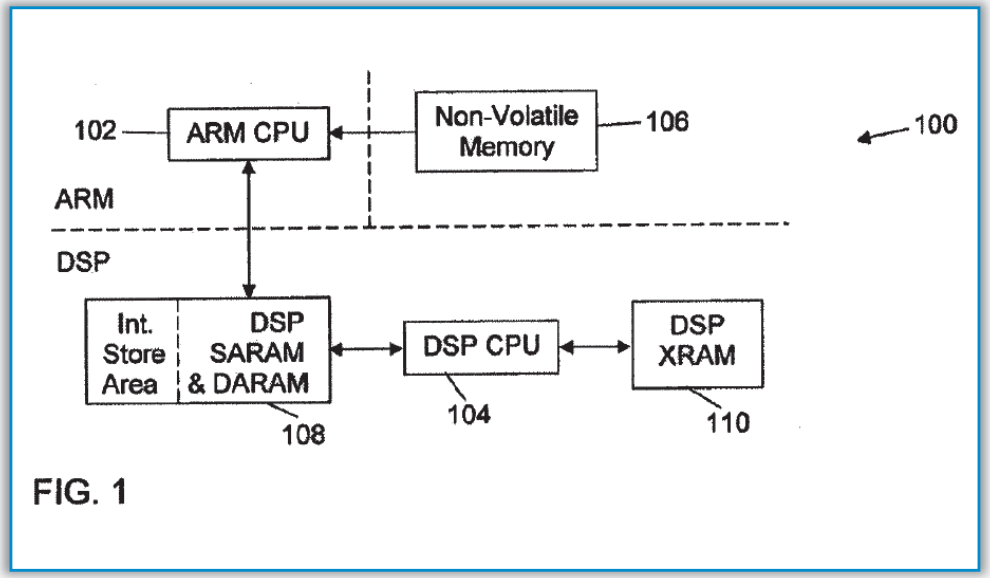


FIG. 1

Ex. 1010 (Svensson) at Fig. 1.

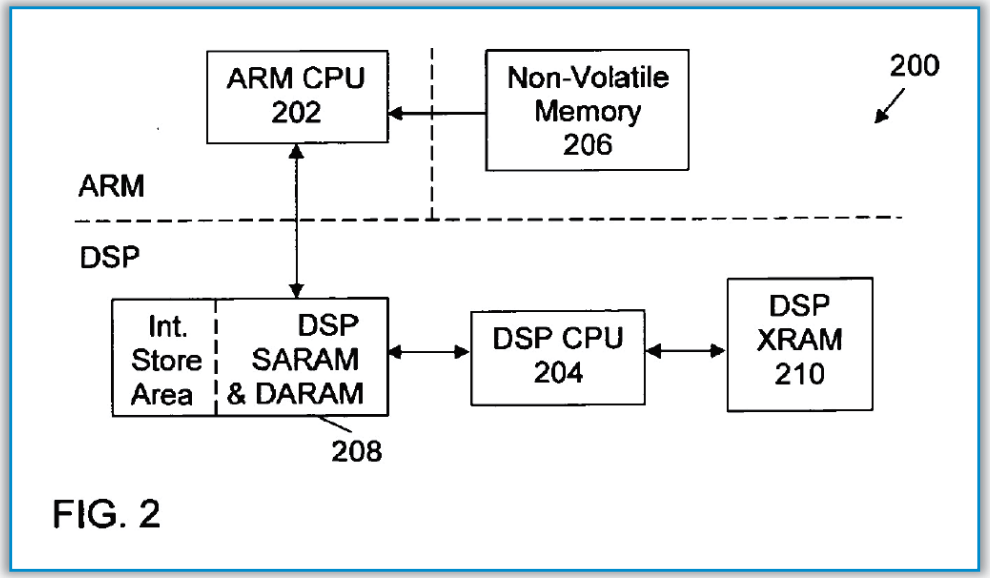
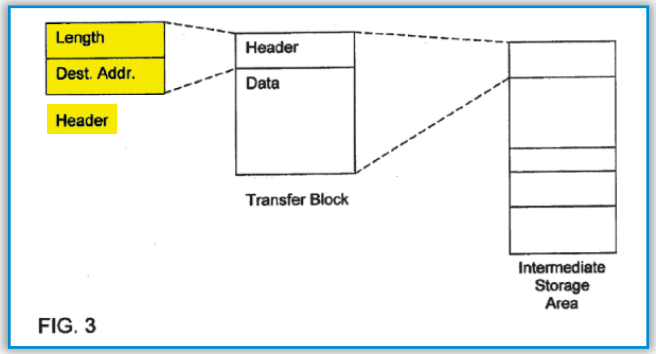


FIG. 2

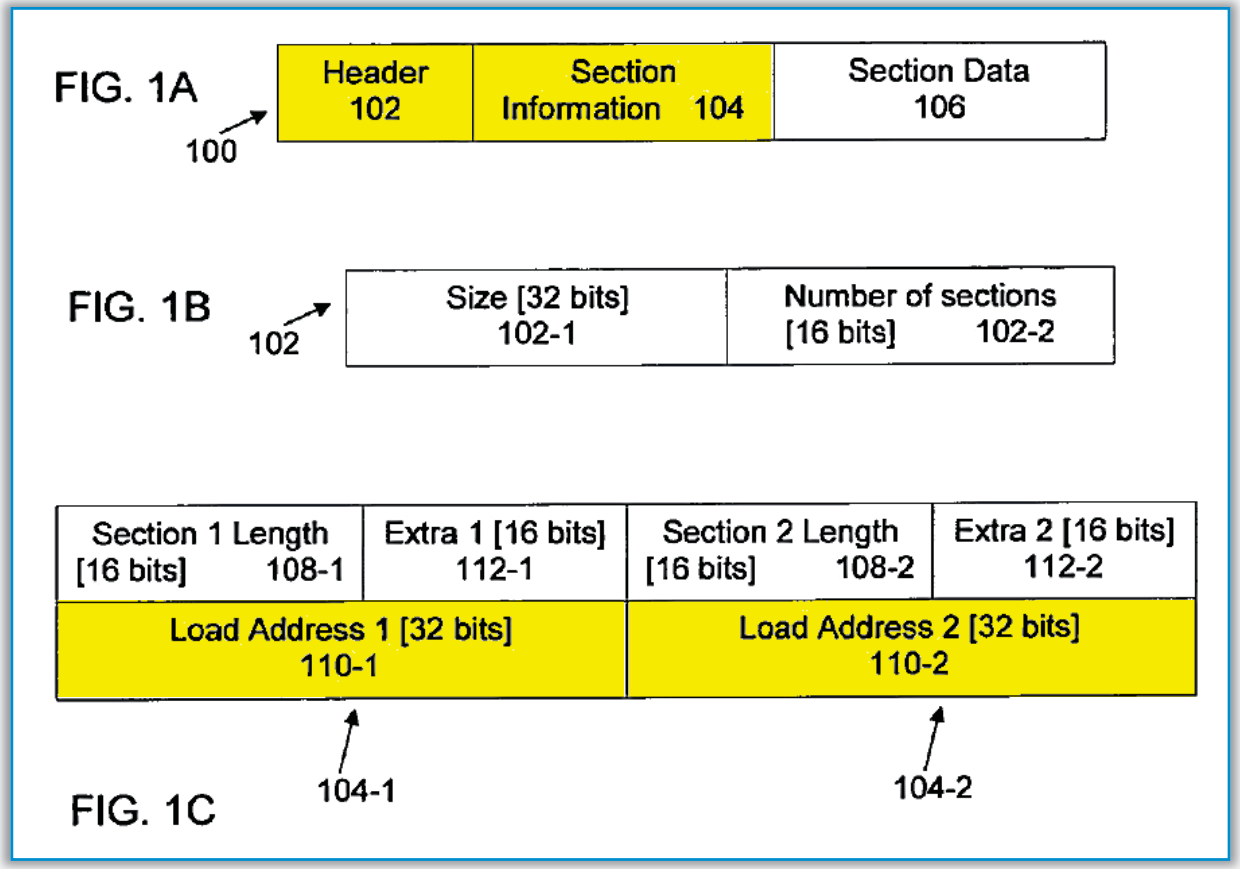
Ex. 1009 (Bauer) at Fig. 2.

Ex. 1010 (Svensson); Ex. 1009 (Bauer); -01334 Pet. at 19-21, 23-24.

Bauer: Improved Header and File Format Over that Used in Svensson



Ex. 1010 (Svensson) at Fig. 3 (highlighting added).



Ex. 1009 (Bauer) at Figs. 1A-1C (highlighting added).

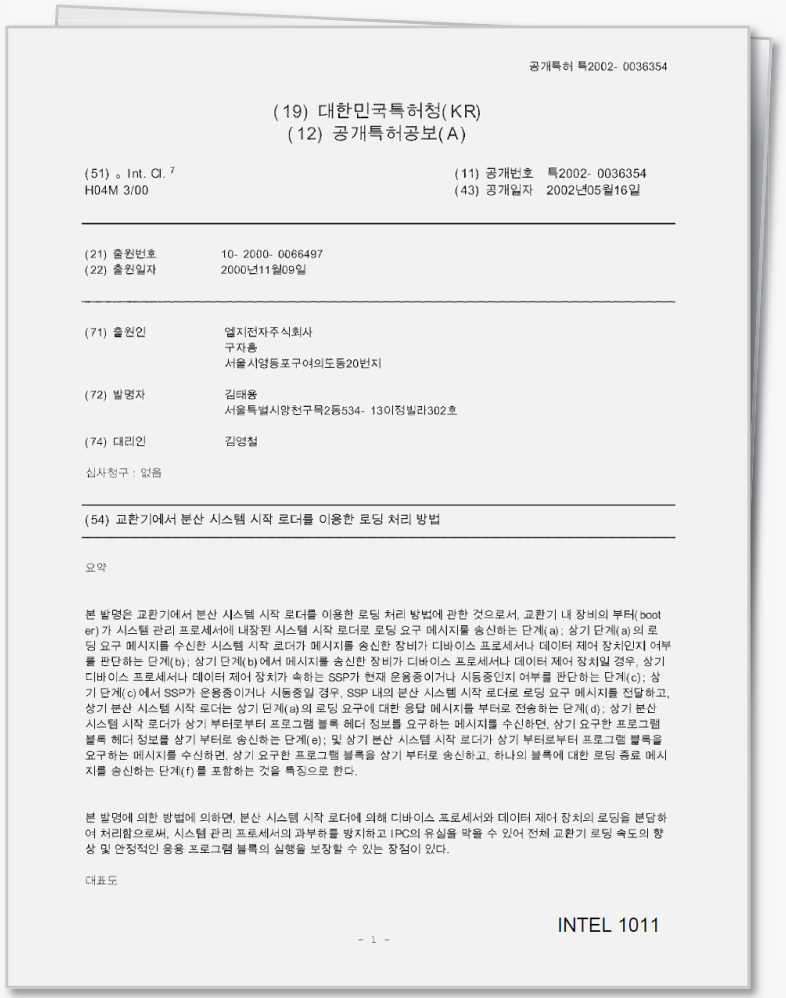
Ex. 1009 (Bauer); -01334 Pet. at 19-21; Ex. 1009 (Lin Decl.) ¶¶ 27-34, 88-90.

Bauer: Cites to Svensson for Example of Program Loader Using Bauer's File Format

[0031] There are many possible applications of this format and its individually coded sections. For example, an operating system memory manager can load and unload sections of memory according to images in this format. It can also be used as a file format in which executable files are stored, and linkers and program loaders can be readily adapted to support (read, write, and interpret) the format. Object code and data can also be stored in this file format, with a program loader reading the stored information and processing stored sections accordingly. One example of such a program loader is described in U.S. patent application Ser. No. 11/040,798 filed on Jan. 22, 2005, by M. Svensson et al. for "Operating-System-Friendly Bootloader".

Ex. 1009 (Bauer) at ¶31 (highlighting added); -01334 Pet. at 20, 24, 32-33.

K.R. 10-2002-0036354 ("Kim")



공개특허 특2002-0036354

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(51) ₀ Int. Cl. [7]
H04M 3/00

(11) 공개번호 특2002-0036354
(43) 공개일자 2002년05월16일

(21) 출원번호 10-2000-0066497
(22) 출원일자 2000년11월09일

(71) 출원인 엘지전자주식회사
구자홍
서울시영등포구여의도동20번지

(72) 발명자 김태용
서울특별시양천구목2동534-13이정빌라302호

(74) 대리인 김영철

심사청구 : 없음

(54) 교환기에서 분산 시스템 시작 로더를 이용한 로딩 처리 방법

요약

본 발명은 교환기에서 분산 시스템 시작 로더를 이용한 로딩 처리 방법에 관한 것으로서, 교환기 내 장비의 부터(booter)가 시스템 관리 프로세서에 내장된 시스템 시작 로더로 로딩 요구 메시지를 송신하는 단계(a); 상기 단계(a)의 로딩 요구 메시지를 수신한 시스템 시작 로더가 메시지를 송신한 장비가 디바이스 프로세서나 데이터 제어 장치인지 여부를 판단하는 단계(b); 상기 단계(b)에서 메시지를 송신한 장비가 디바이스 프로세서나 데이터 제어 장치일 경우, 상기 디바이스 프로세서나 데이터 제어 장치가 속하는 SSP가 현재 운용중이거나 시동중인지 여부를 판단하는 단계(c); 상기 단계(c)에서 SSP가 운용중이거나 시동중일 경우, SSP 내의 분산 시스템 시작 로더로 로딩 요구 메시지를 전달하고, 상기 분산 시스템 시작 로더는 상기 단계(a)의 로딩 요구에 대한 응답 메시지를 부터로 전송하는 단계(d); 상기 분산 시스템 시작 로더가 상기 부터로부터 프로그램 블록 헤더 정보를 요구하는 메시지를 수신하면, 상기 요구한 프로그램 블록 헤더 정보를 상기 부터로 송신하는 단계(e); 및 상기 분산 시스템 시작 로더가 상기 부터로부터 프로그램 블록을 요구하는 메시지를 수신하면, 상기 요구한 프로그램 블록을 상기 부터로 송신하고, 하나의 블록에 대한 로딩 종료 메시지를 송신하는 단계(f)를 포함하는 것을 특징으로 한다.

본 발명에 의한 방법에 의하면, 분산 시스템 시작 로더에 의해 디바이스 프로세서와 데이터 제어 장치의 로딩을 분담하여 처리함으로써, 시스템 관리 프로세서의 과부하를 방지하고 IPC의 유실을 막을 수 있어 전체 교환기 로딩 속도의 향상 및 안정적인 응용 프로그램 블록의 실행을 보장할 수 있는 장점이 있다.

대표도

INTEL 1011

- 1 -

(11) Publication No.: 10-2002-0036354

(43) Publication Date: May 16, 2002

(54) Title (EN): METHOD FOR LOADING USING DISTRIBUTED SYSTEM STARTUPLOADER IN PRIVATE BRANCH EXCHANGE

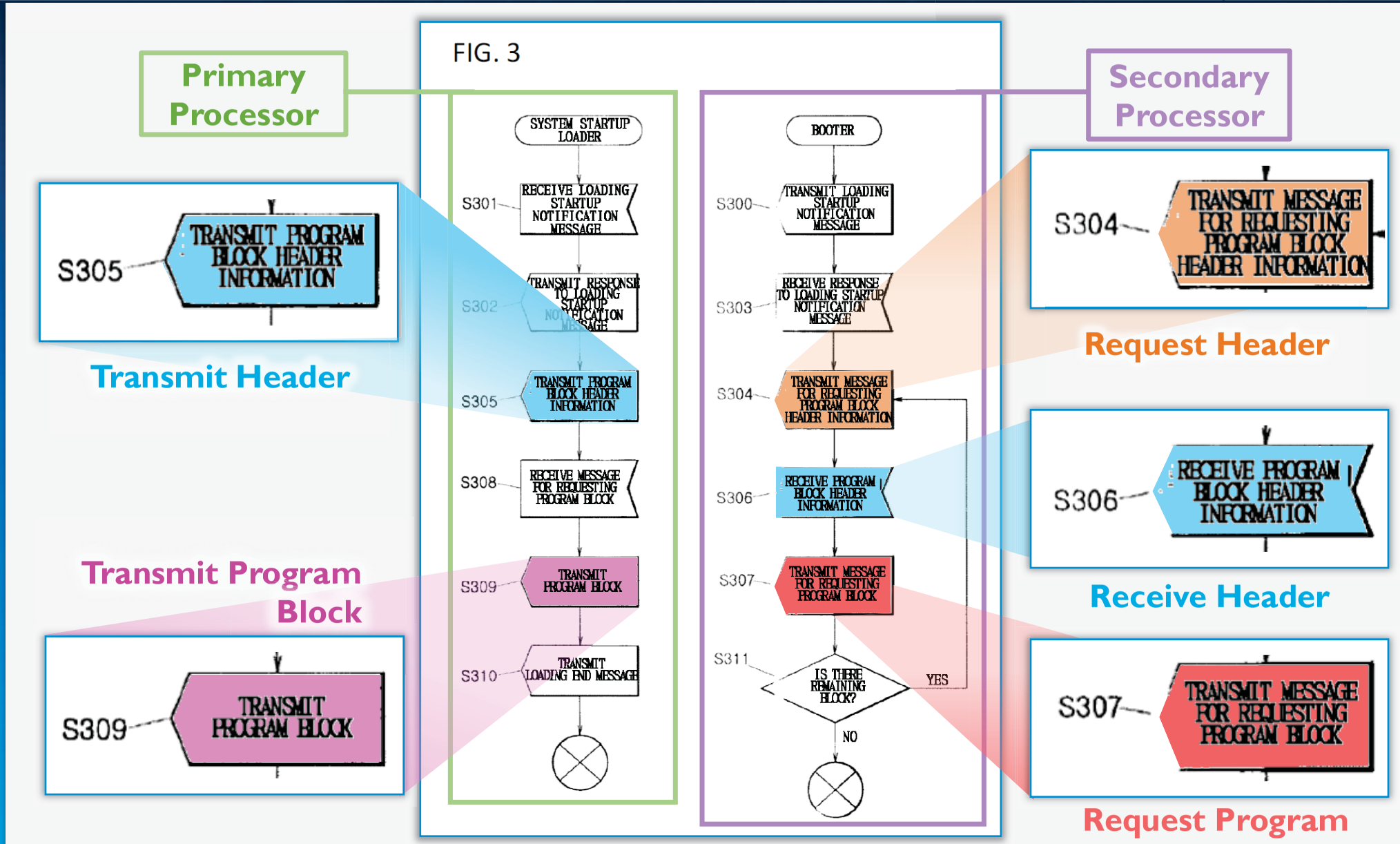
【Abstract】

The present invention relates to a loading processing method using a distributed system startup loader in an exchanger. The loading processing method is characterized by including the steps of: (a) transmitting, by a booter of a device in the exchanger, a loading request message to a system startup loader built in a system management processor; (b) determining, by the system startup loader, whether the device that has transmitted the loading request message is a device processor or a data control device when the loading request message in step (a) is received; (c)

• • • •

Ex. 1011, 1012 (Kim); -01334 Pet. at 21-22; Ex. 1002 (Lin Decl.) ¶¶ 91-93.

Kim: Secondary Processor Receives Header Separately from Program Block



Ex. 1011, 1012 (Kim) at Fig. 3 (highlights and annotations added); -01334 Pet. at 21-22, 40-42.

Overview

- Overview of the ’949 Patent
- Overview of the Prior Art
- **Obviousness of the Challenged Claims**
- Summary of the Proceeding
- Disputed Issues

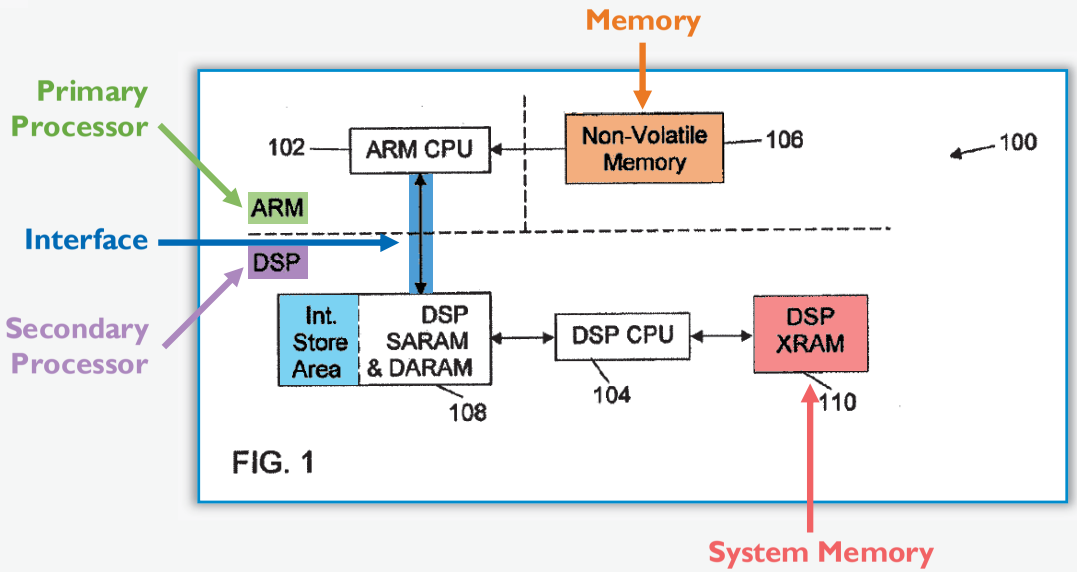
Claim 1 is Obvious Over Bauer and Svensson (and alternatively with Kim)

Claim 1	Discloses?
[1a]. A multi-processor system comprising:	✓ Bauer + Svensson
[1b] a secondary processor comprising: system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image,	✓ Bauer + Svensson
[1c] the image header and each data segment being received separately, and	✓ Bauer + Svensson (and alternatively Kim)
[1d] a scatter loader controller configured: to load the image header; and to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory;	✓ Bauer + Svensson
[1e] a primary processor coupled with a memory, the memory storing the executable software image for the secondary processor; and	✓ Bauer + Svensson
[1f] an interface communicatively coupling the primary processor and the secondary processor, the executable software image being received by the secondary processor via the interface.	✓ Bauer + Svensson

-01334 Pet. at 23-52; Ex. 1002 (Lin Decl.) ¶¶ 101-155.

Claim 1 is Obvious Over Bauer and Svensson (and alternatively with Kim)

- Patent Owner and its expert Dr. Rinard do not dispute that Bauer and Svensson teach the below limitations



Ex. 1010 (Svensson) at Fig. 1 (highlighting and annotations added).

Claim 1	Discloses?
[1a]. A multi-processor system comprising:	✓
[1b] a secondary processor comprising: system memory …	✓
[1e] a primary processor coupled with a memory, the memory storing the executable software image for the secondary processor; and	✓
[1f] an interface communicatively coupling the primary processor and the secondary processor, the executable software image being received by the secondary processor via the interface.	✓

-01334 Pet. at 25-52; Ex. 1002 (Lin Decl.) ¶¶ 151-155; *see generally* POR; Ex. 2007 (Rinard).

Overview

- Overview of the ’949 Patent
- Overview of the Prior Art
- Obviousness of the Challenged Claims
- **Summary of the Proceeding**
- Disputed Issues

Summary of the Proceeding

- The Board instituted trial on all grounds and all claims and consolidated IPR2018-01334, -01335, -01336 into a single proceeding: IPR2018-01334
- Patent Owner contests the challenged claims based on the following:
  - Claim Construction
  - Motivation To Combine Bauer And Svensson -- Obviousness of Transferring an Image in Bauer's File Format to a System Memory of a Secondary Processor Using Svensson's Program Loader
  - Disclosure of "System Memory" and "Hardware Buffer" in Combination of Bauer And Svensson
  - Disclosure of "Scatter Loading" in Combination of Bauer And Svensson
  - Disclosure of Secondary Processor Receiving the Image Header and Each Data Segment Separately in Combination of Bauer and Svensson (and alternatively with Kim)
  - Disclosure of "Scatter Loader Controller" in Combination of Bauer And Svensson
  - Whether Dependent Claims 2 and 12 Are Obvious

-01334 DI; -01335 DI; -01336 DI; *see generally* POR.

Overview

- Overview of the ’949 Patent
- Overview of the Prior Art
- Obviousness of the Challenged Claims
- Summary of the Proceeding
- **Disputed Issues**

Overview:
Issues Raised By Patent Owner

1. **Motivation to Combine Bauer and Svensson**
2. It Would Be Obvious to Transfer an Image in Bauer's File Format Using Svensson's Program Loader
3. Claim Construction
   - "System Memory"
   - "Hardware Buffer"
   - "Image Header"
   - "Scatter Loader Controller"
4. Bauer and Svensson Disclose a "System Memory" and a "Hardware Buffer"
5. Bauer and Svensson Disclose "Scatter Loading"
6. Bauer And Svensson Alone or with Kim Teach Separate Receipt of the Image Header from Each Data Segment

A POSITA Would Have Been Motivated To Combine Bauer And Svensson

- Bauer and Svensson are closely interrelated:

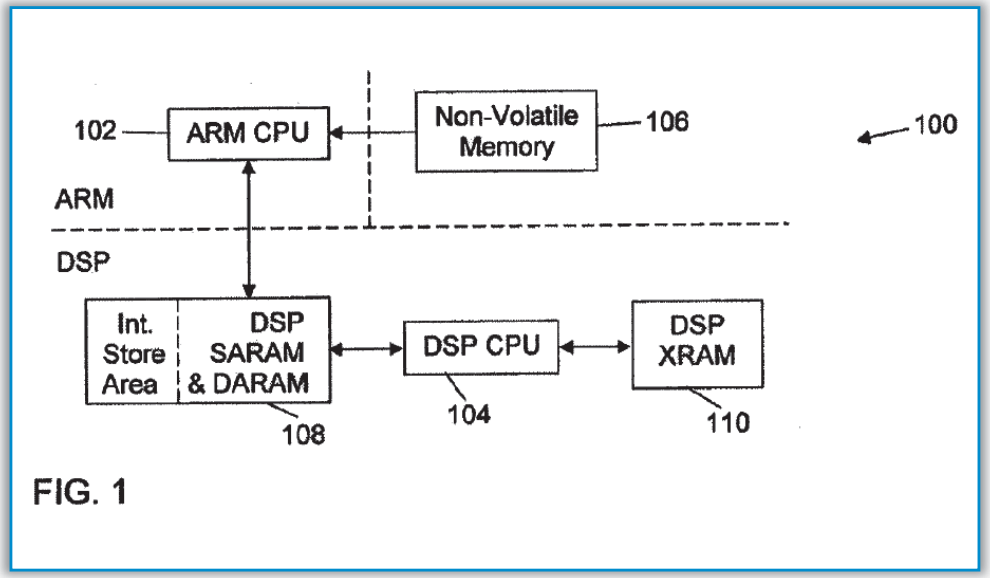


FIG. 1

Ex. 1010 (Svensson) at Fig. 1.

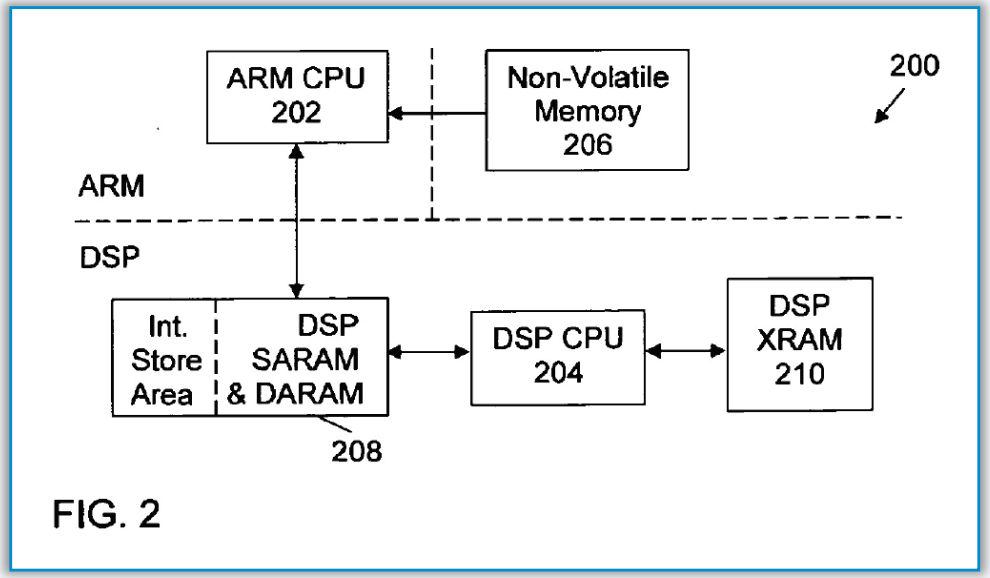


FIG. 2

Ex. 1009 (Bauer) at Fig. 2.

-01334 Pet. at 23-25; Reply Br. at 19-21; Ex. 1002 (Lin Decl.) ¶¶ 101-106.

A POSITA Would Have Been Motivated To Combine Bauer And Svensson

- Patent Owner's own expert Dr. Rinard admits it would have been obvious to combine Bauer and Svensson:

Dr. Martin Rinard
Patent Owner's Expert

Q. Do you agree with me that a person of ordinary skill in the art would combine the teachings of Bauer and Svensson?

A. Okay. Here I'm on Paragraph 107 [of my report], and ***I say "it is conceivable that the POSA," a person of ordinary skill in the art, "would be motivated to combine Bauer and Svensson."***

Q. And you think that's an accurate statement, correct?

A. Yes.

Reply Br. at 20-21; Ex. 1022 (Rinard Dep.) at 177:3-12 (emphasis added).

A POSITA Would Have Been Motivated To Combine Bauer And Svensson

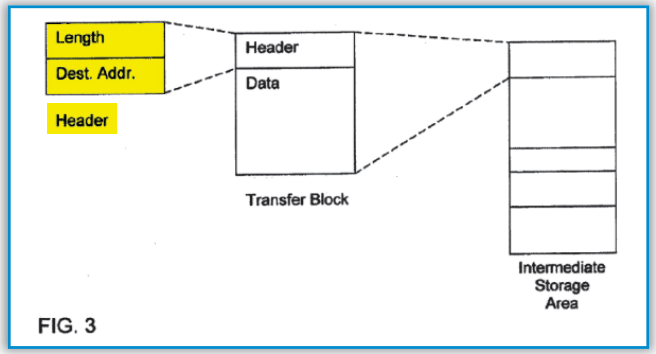
- Bauer explicitly states that its file format can be used with Svensson's program loader:

> [0031] There are many possible applications of this format and its individually coded sections. For example, an operating system memory manager can load and unload sections of memory according to images in this format. It can also be used as a file format in which executable files are stored, and linkers and program loaders can be readily adapted to support (read, write, and interpret) the format. Object code and data can also be stored in this file format, with a program loader reading the stored information and processing stored sections accordingly. One example of such a program loader is described in U.S. patent application Ser. No. 11/040,798 filed on Jan. 22, 2005, by M. Svensson et al. for "Operating-System-Friendly Bootloader".

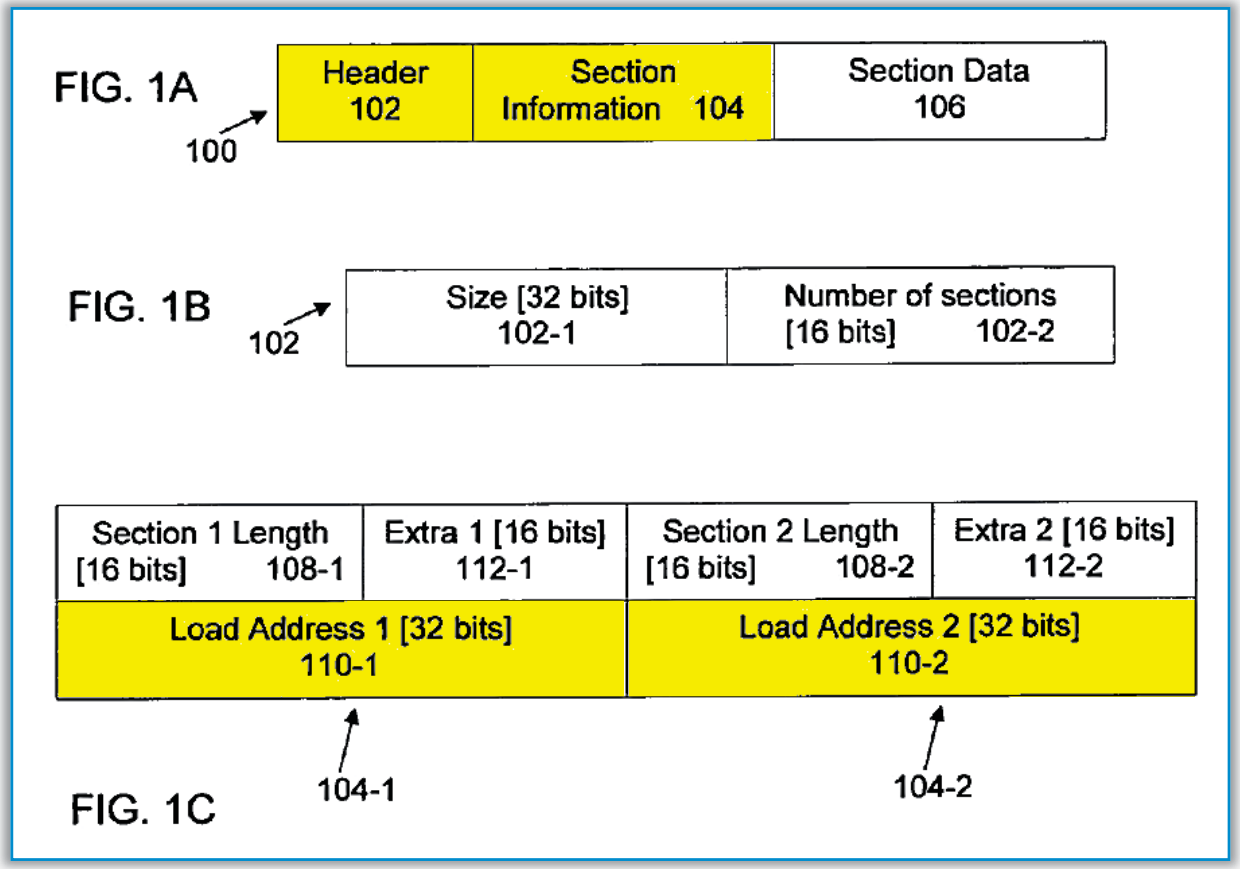
Ex. 1009 (Bauer) at ¶31 (highlighting added); -01334 Pet. at 20, 24, 32-33; Reply Br. at 19-20; Ex. 1002 (Lin Decl.) ¶¶ 101-106, 120-122.

A POSITA Would Have Been Motivated To Combine Bauer And Svensson

- Obvious to combine file format of Bauer with related system of Svensson as expressly instructed by the references:



Ex. 1010 (Svensson) at Fig. 3 (highlighting added).



Ex. 1009 (Bauer) at Figs. 1A-1C (highlighting added).

-01334 Pet. at 23-25, 31-36; Reply Br. at 19-21; Ex. 1002 (Lin Decl.) ¶¶ 101-106, 120-128.

Overview:
Issues Raised By Patent Owner

1. Motivation to Combine Bauer and Svensson
2. **It Would Be Obvious to Transfer an Image in Bauer's File Format Using Svensson's Program Loader**
3. Claim Construction
   - "System Memory"
   - "Hardware Buffer"
   - "Image Header"
   - "Scatter Loader Controller"
4. Bauer and Svensson Disclose a "System Memory" and a "Hardware Buffer"
5. Bauer and Svensson Disclose "Scatter Loading"
6. Bauer And Svensson Alone or with Kim Teach Separate Receipt of the Image Header from Each Data Segment

Obvious to Use Bauer's File Format with Svensson's Program Loader

- Bauer explicitly instructs to use Svensson's program loader with Bauer's file format when loading an image for execution:

> [0031] There are many possible applications of this format and its individually coded sections. For example, an operating system memory manager can load and unload sections of memory according to images in this format. It can also be used as a file format in which executable files are stored, and linkers and program loaders can be readily adapted to support (read, write, and interpret) the format. Object code and data can also be stored in this file format, with a program loader reading the stored information and processing stored sections accordingly. One example of such a program loader is described in U.S. patent application Ser. No. 11/040,798 filed on Jan. 22, 2005, by M. Svensson et al. for "Operating-System-Friendly Bootloader".

Ex. 1009 (Bauer) at ¶31 (highlighting added); -01334 Pet. at 20, 24, 32-33; Reply Br. at 23-24.

Obvious to Use Bauer's File Format with Svensson's Program Loader

- Bauer sets forth that its file format from Figures 1A-1C can be used in any one or more of the memories in Figure 2:

[0036] Most commercially available DSP devices include on-chip memories, and as indicated in **FIG. 2**, the DSP includes "internal" single-access RAM (SARAM) and dual-access RAM (DARAM) **208**, as well as an "external" RAM (XRAM) **210**. An intermediate storage area, indicated by the dashed line, may be defined within the memory **208**. The arrows in **FIG. 2** indicate access paths, e.g., busses and direct memory access (DMA) paths, between the CPUs and the memories, any one or more of which may store an image in the format depicted in **FIGS. 1A-1C**. The ARM host CPU

Ex. 1009 (Bauer) at ¶36 (highlighting added).

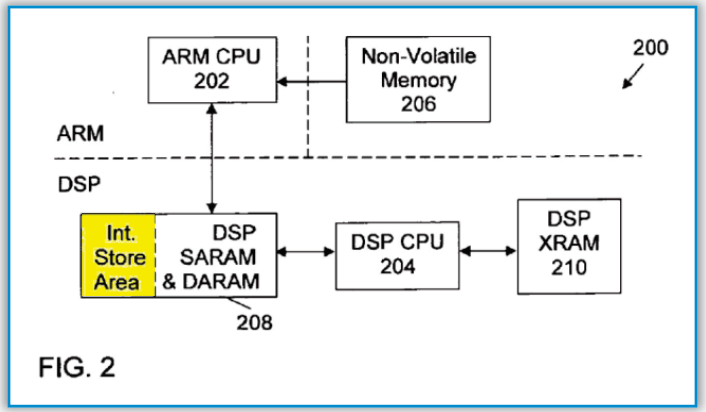


FIG. 2

Ex. 1009 (Bauer) at Fig. 2 (highlighting added).

Reply Br. at 24-25; Ex. 1022 (Rinard Dep.) at 127:16-128:2; -01334 Pet. at 33, 45-46.

Obvious to Use Bauer's File Format with Svensson's Program Loader

- Patent Owner's own expert Dr. Rinard admits Bauer's file format can be stored in any of memories 206, 208, 210:

Dr. Martin Rinard
Patent Owner's Expert

Q. Okay. So any of memories 206, 208 and 210 in Figure 2 of Bauer can store an image in the file format of Figures 1A to 1C of Bauer, correct?

A. ***Yeah.*** I mean, this is a – Figures 1A to 1C disclose a method of storing information. You can store information in memories. ***Any of these memories can store information in that format.***

Ex. 1022 (Rinard Dep.) at 127:16-128:2 (emphasis added)

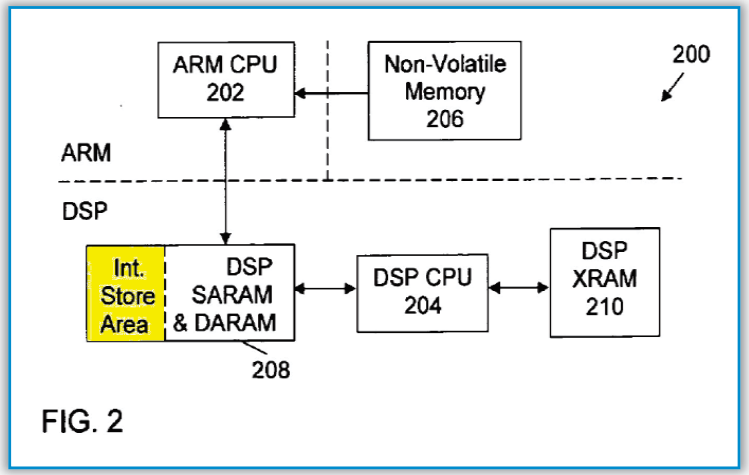


FIG. 2

Ex. 1009 (Bauer) at Fig. 2 (highlighting added).

Reply Br. at 25-26.

Obvious to Use Bauer's File Format with Svensson's Program Loader

- Bauer teaches that its approach "simplifies optimization" and "makes memory loading efficient":

> [0043] Having information about the sections collected in the header **102** and section information **104** simplifies optimization in a number of circumstances, for instance, if sections are to be loaded into memory. The block **104** lists all sections, preferably in order of memory location, and this makes memory loading efficient as there is no need to search through an image for section headers when loading.

Ex. 1009 (Bauer) at ¶43 (highlights added), Figs. 1A-1C; Reply Br. at 19, 26; -01334 Pet. at 19-20, 32, 35, 44.

Obvious to Use Bauer's File Format with Svensson's Program Loader

- Bauer explains that its file format can be used so that a loader will "retrieve" header 102 and section information 104 before reading any of the data segments:

> [0030] Thus, it will be appreciated that the format described here, in contrast to prior data formats, supports individual coding of sections, where a section can contain any type of data, such as executable, binary, text, etc. Information about the sections is located in a header and section information at, for example, the beginning of the image, and so the information about the sections can be retrieved before the sections are read. Moreover, the format

Ex. 1009 (Bauer) at ¶30 (highlights added), Figs. 1A-1C; Reply Br. at 27-29; -01334 Pet. at 46.

Overview:
Issues Raised By Patent Owner

1. Motivation to Combine Bauer and Svensson
2. It Would Be Obvious to Transfer an Image in Bauer's File Format Using Svensson's Program Loader
3. **Claim Construction**
   - "System Memory"
   - "Hardware Buffer"
   - "Image Header"
   - "Scatter Loader Controller"
4. Bauer and Svensson Disclose a "System Memory" and a "Hardware Buffer"
5. Bauer and Svensson Disclose "Scatter Loading"
6. Bauer And Svensson Alone or with Kim Teach Separate Receipt of the Image Header from Each Data Segment

Claim Construction: "System Memory"

- Petitioner (in petitions) & Board's Institution Decision:
  - No construction necessary
- Patent Owner's construction should be rejected:
  - "memory that is addressable by the secondary processor"
- Petitioner (reply):
  - No construction necessary or "memory where an executable software image can be loaded and executed"

POR at 9-12; 1334 DI at 8; Reply Br. at 3, 6.

Claim Construction: "System Memory"

- Both parties' experts agree that a "system memory" is where an executable software image can be "loaded and executed":

Dr. Martin Rinard
Patent Owner's Expert

> Q. Do you agree with Dr. Lin that ***system memory is memory where programs can be loaded and executed*** by a processor?
>
> ***A. That's one of the things that system memory does, that you can do with system memory.*** It's not the only thing.

Dr. Bill Lin
Petitioner's expert

> Q. Would you consider a memory that stores an operating system for execution by a processor to be a system memory?
>
> …
>
> A. So a ***system memory would be a portion of the memory where programs could be loaded and executed.*** …

Reply Br. at 5; Ex. 1023 (Lin Reply Decl.) ¶12; Ex. 1022 (Rinard Dep.) at 61:9-14 (emphasis added); Ex. 2001 (Lin Dep.) at 25:6-12 (emphasis added).

Claim Construction: "System Memory"

- '949 specification describes "system memory" as memory where programs are loaded and executed:

> buffer for receiving at a least a portion of an executable software image. The secondary processor includes a scatter loader controller for loading the executable software image directly from the hardware buffer to the system memory. The

> processor **307**. The image header includes information used to identify where the modem image executable data is to be eventually placed into the system memory of the secondary processor **305**. The header information is used by the second-

> to different locations in the system memory **305**. In one aspect, the executable software image is loaded into the system memory of the secondary processor without an entire executable software image being stored in the hardware buffer of the secondary processor.

Reply Br. at 5-6; Ex. 1001 ('949 patent) at 2:61-63, 8:18-21, 9:37-41 (highlighting added); Ex. 1023 (Lin Reply Decl.) ¶13.

Claim Construction: "Hardware Buffer"

- Petitioner and Board's Institution Decision:
  - No construction necessary
- Patent Owner's construction should be rejected:
  - "a buffer within a hardware transport mechanism that receives data sent from the primary processor to the secondary processor"

Reply Br. at 8-11; -1334 DI at 8.

Claim Construction: "Hardware Buffer"

- Claim 1 of the '949 patent merely requires the "hardware buffer" to be part of the "secondary processor"—without requiring it to exist in any specific place within that processor, and without even mentioning a "hardware transport mechanism":

> 1. A multi-processor system comprising:
> a secondary processor comprising:
> system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image, the image header and each data segment being received separately, and

Reply Br. at 9; Ex. 1001 ('949 patent) at claim 1 (highlighting added).

Claim Construction: "Hardware Buffer"

- '949 specification uses the term "hardware buffer" only twice, merely to require the "hardware buffer" to be part of the "secondary processor"—without mentioning a "hardware transport mechanism":

> A multi-processor system is offered. The system includes a secondary processor having a system memory and a hardware buffer for receiving at a least a portion of an executable software image. The secondary processor includes a scatter loader controller for loading the executable software image directly from the hardware buffer to the system memory. The

> to different locations in the system memory 305. In one aspect, the executable software image is loaded into the system memory of the secondary processor without an entire executable software image being stored in the hardware buffer of the secondary processor.

Reply Br. at 9-10; Ex. 1001 ('949 patent) at 2:58-61, 9:37-41 (highlighting added).

Claim Construction: "Hardware Buffer"

- Patent Owner's reliance on Figure 3 is improper, given that it is merely "exemplary" and there is no reason to limit the claim to that specific embodiment:

> In one aspect of the present disclosure, the loading process 60
> is divided into two stages, as illustrated in the exemplary flow
> shown in FIG. 3. FIG. 3 shows a block diagram of a primary

Reply Br. at 10; Ex. 1001 ('949 patent) at 7:60-63 (highlighting added).

Claim Construction: "Image Header"

- Parties' agreed construction:
  - "header associated with the entire image that specifies where the data segments are to be placed in the system memory"
- Board's initial construction:
  - "the image header is perhaps better described as having information that can be used to determine the placement of the at least one data segment in the system memory"
- Claims invalid under agreed construction and also under Board's initial construction, which is broader

Reply Br. at 8; -1334 DI at 8; -1335 DI at 8; -1336 DI at 8.

Claim Construction: "Scatter Loader Controller"

- Petitioner and Board's Institution Decision:
  - No construction necessary
- Patent Owner's construction should be rejected:
  - "a component of a hardware transport mechanism that scatter loads data received from the primary processor directly into the system memory of the secondary processor"

Reply Br. at 11-13; -1334 DI at 8.

Claim Construction: "Scatter Loader Controller"

- Patent Owner's construction should be rejected:
  - No evidence a POSITA would have understood that the plain meaning of a "scatter loader controller" requires that it reside in a "hardware transport mechanism"
  - Claim 1 merely requires the "scatter loader controller" to be part of the "secondary processor"—without requiring it to exist in any specific place
    - Ex. 1001 ('949 patent) at claim 1 ("a secondary processor comprising … a scatter loader controller")

Reply Br. at 11-13; Ex. 1023 (Lin Reply Decl.) ¶¶28-29; Ex. 1001 ('949 patent) at claim 1.

Claim Construction: "Scatter Loader Controller"

- Patent Owner's reliance on Figure 3 is improper, given that it is merely "exemplary" and there is no reason to limit the claim to that specific embodiment:

> In one aspect of the present disclosure, the loading process is divided into two stages, as illustrated in the exemplary flow shown in FIG. 3. FIG. 3 shows a block diagram of a primary

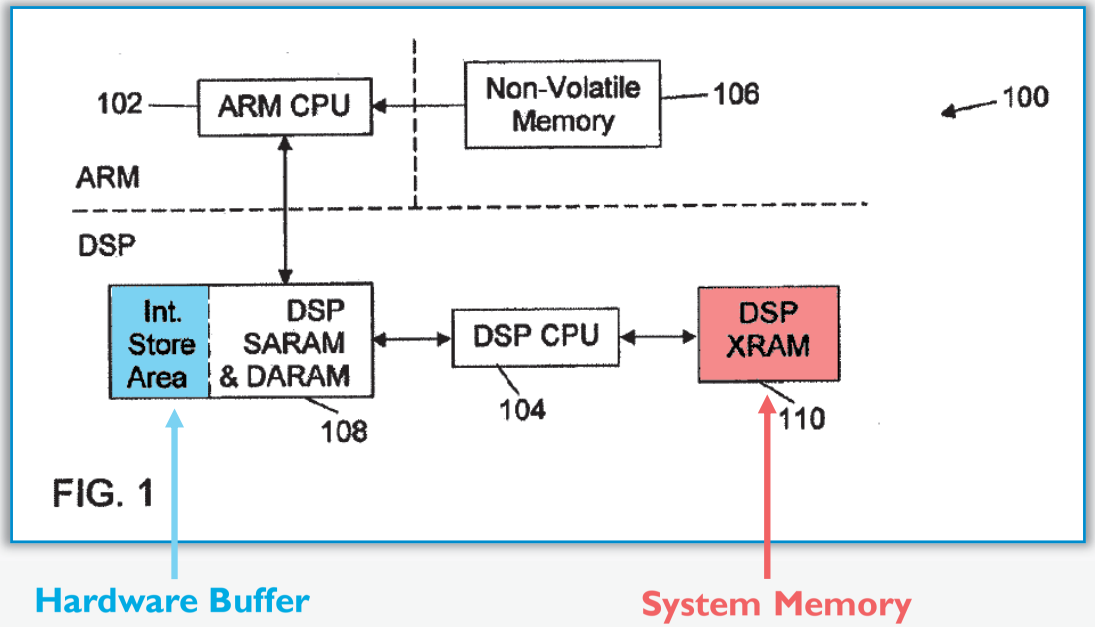
Reply Br. at 10, 12; Ex. 1001 ('949 patent) at 7:60-63 (highlighting added).

Overview:
Issues Raised By Patent Owner

1. Motivation to Combine Bauer and Svensson
2. It Would Be Obvious to Transfer an Image in Bauer's File Format Using Svensson's Program Loader
3. Claim Construction
   - "System Memory"
   - "Hardware Buffer"
   - "Image Header"
   - "Scatter Loader Controller"
4. **Bauer and Svensson Disclose a "System Memory" and a "Hardware Buffer"**
5. Bauer and Svensson Disclose "Scatter Loading"
6. Bauer And Svensson Alone or with Kim Teach Separate Receipt of the Image Header from Each Data Segment

Combination of Bauer And Svensson discloses "System Memory" & "Hardware Buffer"

- Patent Owner argues that Bauer and Svensson do not disclose a "hardware buffer" that is separate from "system memory." POR at 52-58.
  - But Figure 1 of Svensson (and Figure 2 of Bauer) discloses an intermediate storage area ("hardware buffer") that is separate from DSP XRAM 210 ("system memory"):



Reply Br. at 31-32; -1334 Pet. at 26-27, 46-48; Ex. 1009 (Bauer) at Fig. 2; Ex. 1010 (Svensson) at Fig. 1 (highlights and annotations added).

Combination of Bauer And Svensson discloses "System Memory" & "Hardware Buffer"

- Under the correct, plain meaning of "system memory," the intermediate storage area of Bauer/Svensson is not a "system memory" because code is not executed from it
- Patent Owner's expert Dr. Rinard agrees that code is executed from the XRAM 110, not the intermediate storage area:

Dr. Martin Rinard
Patent Owner's Expert

Q. Am I right that in ***Svensson the client processor 104 does not execute code directly from the intermediate storage area***?

A. That, I believe, is the intention of the patent, yes. Although in theory, I suppose it could, but that's not the intention of the patent**.**

Q. Do you agree with me that in ***Svensson the client processor 104 executes code from the XRAM 110***?

A. That's one of the places where it's described as potentially being able to execute from, **sure**.

Reply Br. at 34-36; Ex. 1022 (Rinard Dep.) at 107:1-7, 108:21-109:4 (emphasis added).

Combination of Bauer And Svensson discloses "System Memory" & "Hardware Buffer"

- Patent Owner's arguments for alleging lack of a "hardware buffer" also hinge on its proposed construction of "hardware buffer" as being limited to a structure within a "hardware transport mechanism"
  - The "hardware transport mechanism" requirement is incorrect, and Patent Owner's argument should be rejected for this reason
  - Bauer's and Svensson's intermediate storage area meets Patent Owner's construction

Reply Br. at 8-11, 47-49; -1334 Pet. at 26-27; POR at 14-15.

Overview:
Issues Raised By Patent Owner

1. Motivation to Combine Bauer and Svensson
2. It Would Be Obvious to Transfer an Image in Bauer's File Format Using Svensson's Program Loader
3. Claim Construction
   - "System Memory"
   - "Hardware Buffer"
   - "Image Header"
   - "Scatter Loader Controller"
4. Bauer and Svensson Disclose a "System Memory" and a "Hardware Buffer"
5. **Bauer and Svensson Disclose "Scatter Loading"**
6. Bauer And Svensson Alone or with Kim Teach Separate Receipt of the Image Header from Each Data Segment

Bauer And Svensson Disclose "Scatter Loading"

- Patent Owner argues that Bauer does not disclose "scatter loading" into the DSP device's XRAM (the "system memory")
  - But Bauer teaches that each data segment (1) has its own load (destination) address specifying where to place the data segment in system memory and (2) can be arranged in the image in any suitable order:

> [0037] As depicted in **FIG. 1A**, the section information entry or entries **104** precede the data **106** of the section(s) in the image **100**. The section data **106** is advantageously arranged in the image in a sequence, and it is preferable that the section data **106** as well as the section information entries **104** are arranged in order of the section load addresses **110**, starting with the lowest address. It will be understood, however, that other orders are suitable, e.g., starting with the highest address, and that in general it is not necessary to order the section by their load addresses. The sections may be in an arbitrary order. As each section has a respective load address, the sections can appear in any order (e.g., by size, coding type, or whatever is suitable). It is

Reply Br. at 37-41; -1334 Pet. at 47-48; POR at 60; Ex. 1009 (Bauer) at ¶37 (highlights added).

Bauer And Svensson Disclose "Scatter Loading"

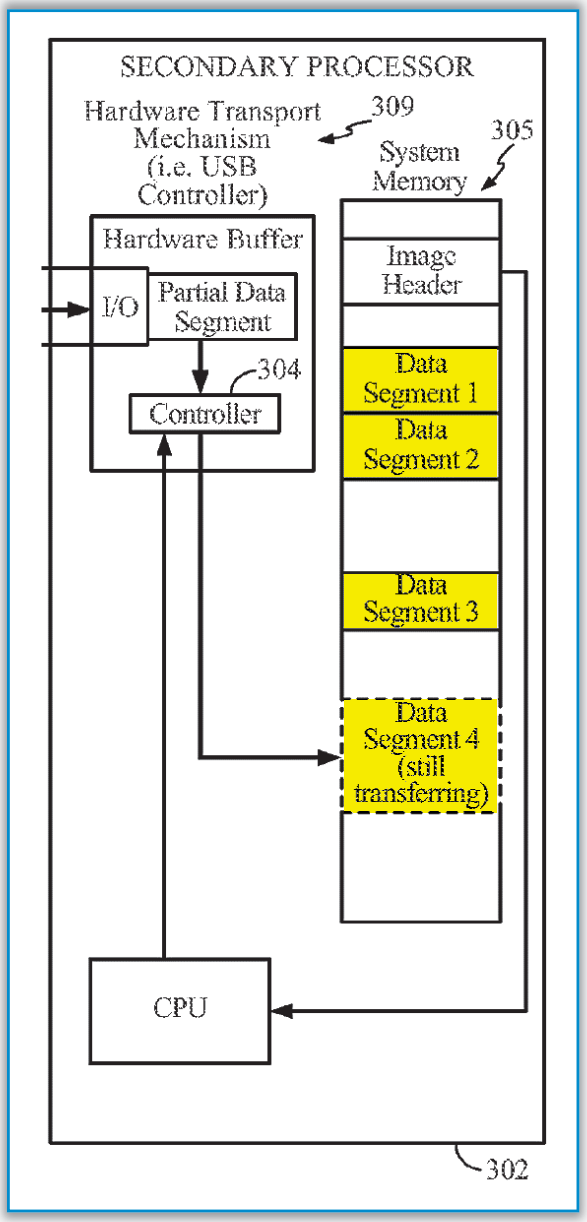
- The '949 specification recognizes that data segments are scattered when loaded into contiguous or non-contiguous locations:

where each segment can be loaded into a different memory region. Target memory locations of executable segments may or may not be contiguous with respect to each other. One

Ex. 1001 ('949 patent), 4:36-37 (highlights added).

As shown in FIG. **3**, the image segments are not necessarily placed into consecutive locations within the secondary processor's system memory **305**. Instead, the segments may be spread out in different locations of the memory. The exem-

Ex. 1001 ('949 patent), 9:12-15 (highlights added).

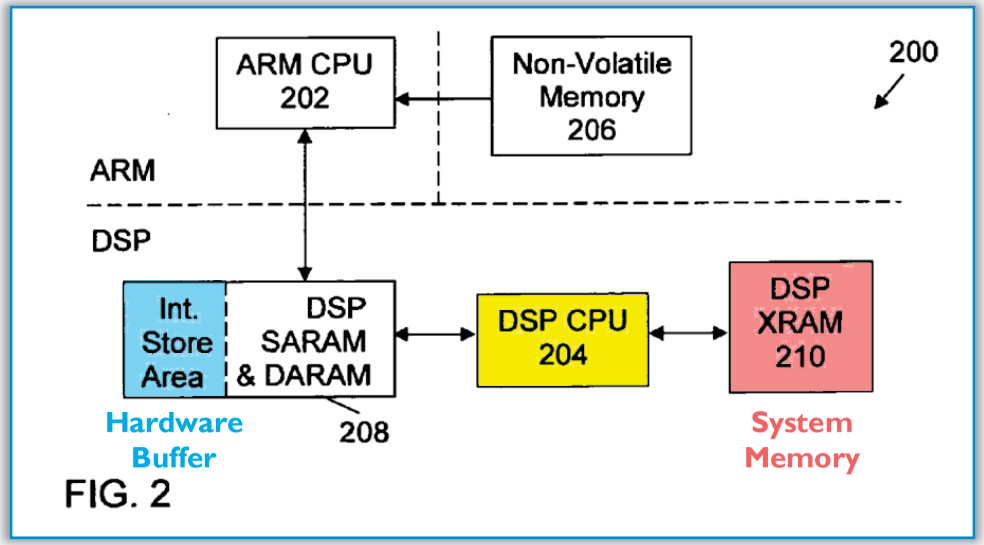


Ex. 1001 ('949 patent), Fig 3 (highlights added).

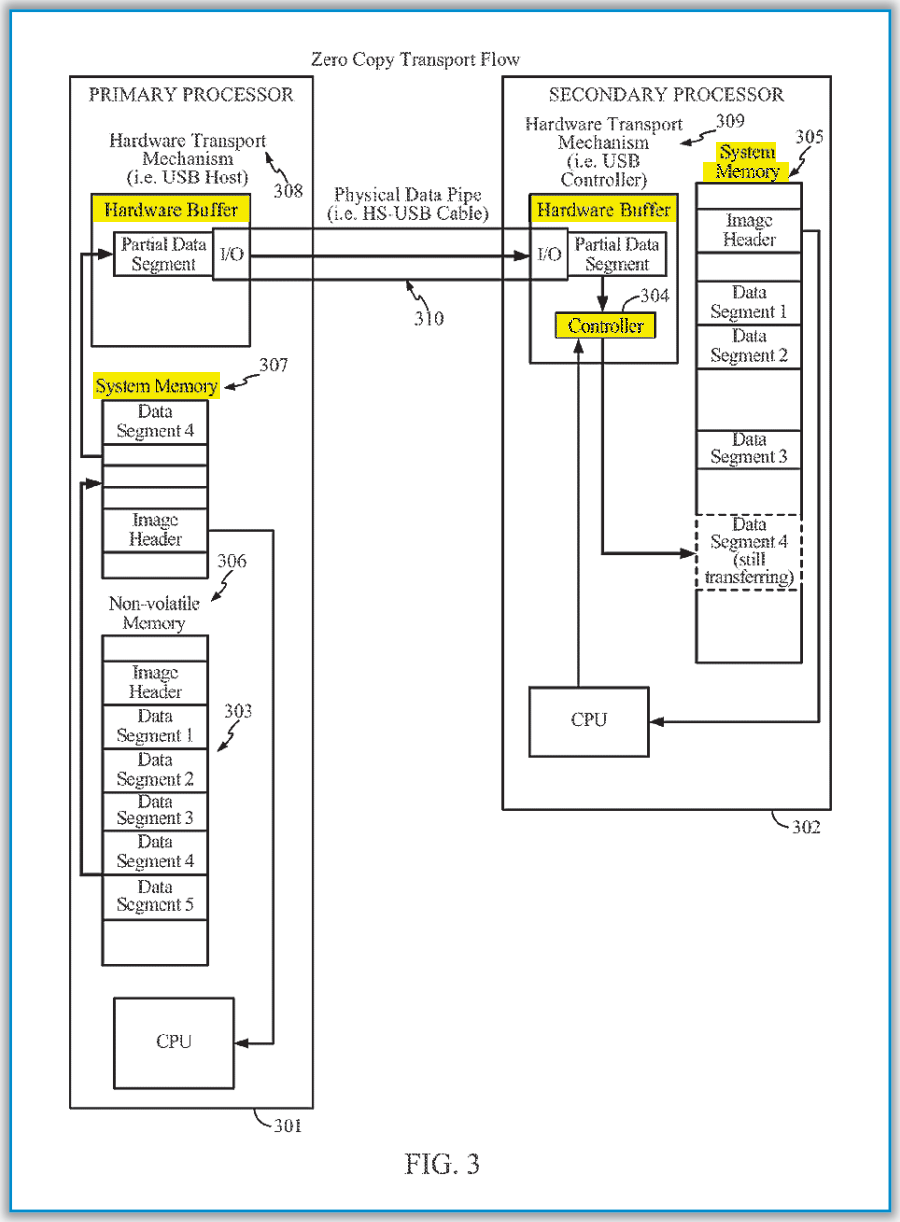
Reply Br. at 40-41; -1334 Pet. at 47-48.

Bauer And Svensson Disclose "Scatter Loading"

- Patent Owner argues that Bauer/Svensson do not teach "direct" "scatter loading" because there are other components between primary processor ARM CPU 202/102 and system memory DSP XRAM 210/110
  - But Figure 3 of the '949 patent has numerous components—including controller 304—in the path to the system memory



Ex. 1009 (Bauer), Fig 2 (highlights and annotations added)



Ex. 1001 ('949 patent), Fig 3 (highlights added).

Reply Br. at 36-37; POR at 56-57.

Bauer And Svensson Disclose "Scatter Loading"

- Patent Owner's expert Dr. Rinard admits that scatter loading was known in the prior art to the '949 patent:

Dr. Martin Rinard
Patent Owner's Expert

Q. Scatter loading image data from one location to another location was known in the prior art to the '949 patent, correct?

…

A. I think the general concept of scatter loading was known prior to the '949 patent, yes.

Reply Br. at 41-42; Ex. 1022 (Rinard Dep.) at 36:20-37:5 (emphasis added); -1334 Pet. at 47-48.

Overview:
Issues Raised By Patent Owner

1. Motivation to Combine Bauer and Svensson
2. It Would Be Obvious to Transfer an Image in Bauer's File Format Using Svensson's Program Loader
3. Claim Construction
   - "System Memory"
   - "Hardware Buffer"
   - "Image Header"
   - "Scatter Loader Controller"
4. Bauer and Svensson Disclose a "System Memory" and a "Hardware Buffer"
5. Bauer and Svensson Disclose "Scatter Loading"
6. **Bauer And Svensson Alone or with Kim Teach Separate Receipt of the Image Header from Each Data Segment**

Bauer Discloses Receiving the Image Header and Each Data Segment Separately

- Patent Owner argues that Bauer provides "no details" with respect to the separate receipt requirement. POR at 61.
  - But Bauer teaches that header 102 and section information 104 (the "image header") are "retrieved" before—and thus, separately from—the data segments:

> [0030] Thus, it will be appreciated that the format described here, in contrast to prior data formats, supports individual coding of sections, where a section can contain any type of data, such as executable, binary, text, etc. Information about the sections is located in a header and section information at, for example, the beginning of the image, and so the information about the sections can be retrieved before the sections are read. Moreover, the format

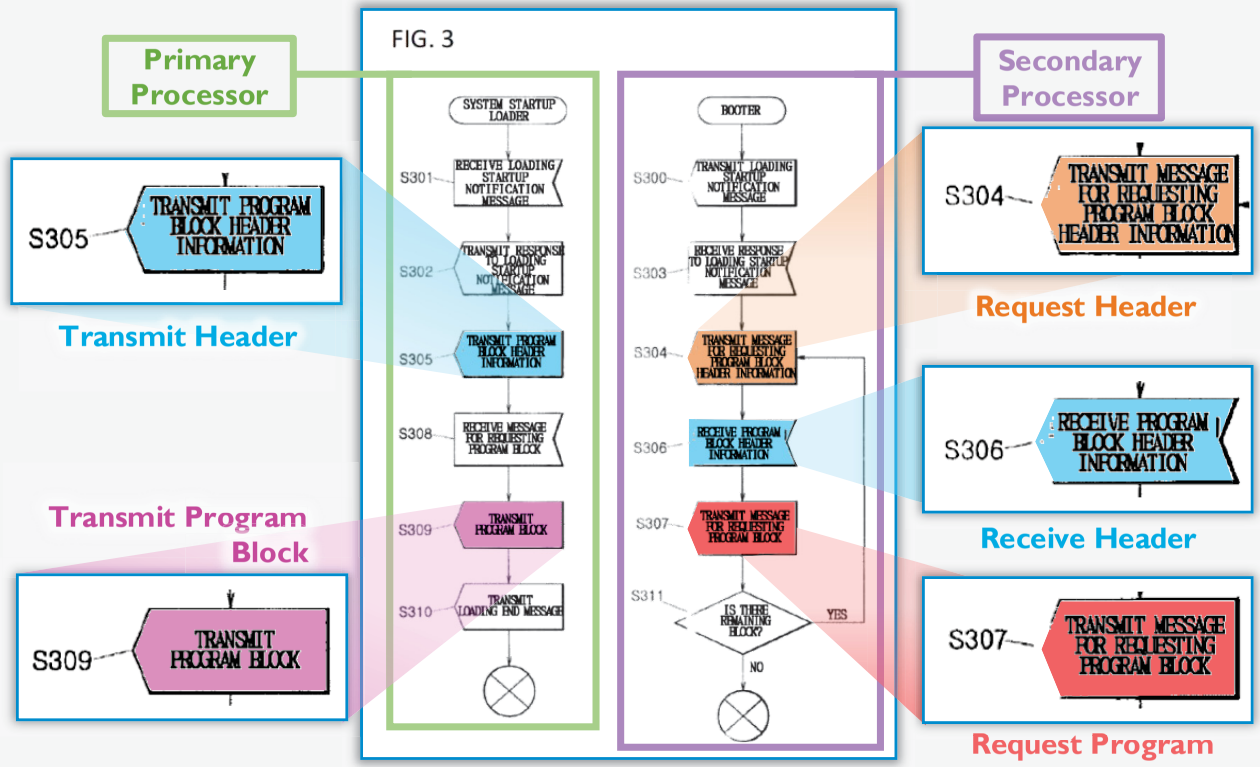
> compression, of the sections. The header and section information are arranged in an image having this format such that they are readable before the sections are processed. For

Reply Br. at 42-43; -01334 Pet. at 37-39; Ex. 1009 (Bauer) at ¶30, Abstract (highlights added).

Kim Discloses Receiving the Image Header and Each Data Segment Separately

- Patent Owner never contends that Kim does not teach separate receipt of the image header from the data blocks, but instead argues that Kim would not be combined with Bauer and Svensson because it would be contrary to the teachings of Svensson. POR at 67-69.

- Kim teaches what was already known in the prior art and a POSITA would combine it with Bauer and Svensson



Ex. 1011, 1012 (Kim) at Fig. 3 (highlights and annotations added); -01334 Pet. at 21-22, 40-42.

Reply Br. at 45-47; -01334 Pet. at 21-22, 40-42.

Ex-1012 (Kim) at Fig. 3 (highlights and annotations added)

Respectfully Submitted,

Dated: December 9, 2019

/Thomas E. Anderson/
Thomas E. Anderson
Reg. No. 37,063
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on December 9, 2019, I caused a true and correct copy of the foregoing material:

- PETITIONER'S DEMONSTRATIVE EXHIBITS

to be served via electronic mail on the following attorneys of record:

David B. Cochran, Reg. No. 39,142 (dcochran@jonesday.com)

Matthew W. Johnson, Reg. No. 59,108 (mwjohnson@jonesday.com)

Joseph M. Sauer, Reg. No. 47,919 (jmsauer@jonesday.com)

Joshua R. Nightingale, Reg. No. 67,865 (jrnightingale@jonesday.com)

David M. Maiorana, Reg. No. 41,449 (dmaiorana@jonesday.com)

/Thomas E. Anderson/
Thomas E. Anderson
Reg. No. 37,063
Counsel for Petitioner