Trials@uspto.gov
571-272-7822

Paper 10
Entered: March 18, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

Case IPR2018-01335
Patent 8,838,949 B2

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and AARON W. MOORE, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation ("Petitioner") filed a Petition requesting *inter partes* review of claims 10–17 of U.S. Patent No. 8,838,949 B2 ("the '949 patent," Ex. 1101). Paper 3 ("Pet."). Qualcomm Incorporated ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp."). Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

After considering the Petition, the Preliminary Response, and associated evidence, we institute an *inter partes* review as to all challenged claims and on all grounds raised in the Petition.

A. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 2–3; Paper 4, 2. Among those related matters are IPR2018-01334 and IPR2018-01336, each of which involves different claims of the '949 patent.

B. Real Parties in Interest

Petitioner identifies itself and Apple Inc. as real parties in interest. Pet. 2.

C. The '949 Patent and Illustrative Claim

The '949 patent generally relates to loading software from one processor to another in a multi-processor system. Ex. 1101, at [57]. One example disclosed in the '949 patent involves loading modem image executable data by first retrieving and processing an image header, which "includes information used to identify where the modem image executable data is to be eventually placed into the system memory of the secondary processor." Ex. 1101, 8:9–21. Figure 3 of the '949 patent is reproduced below.

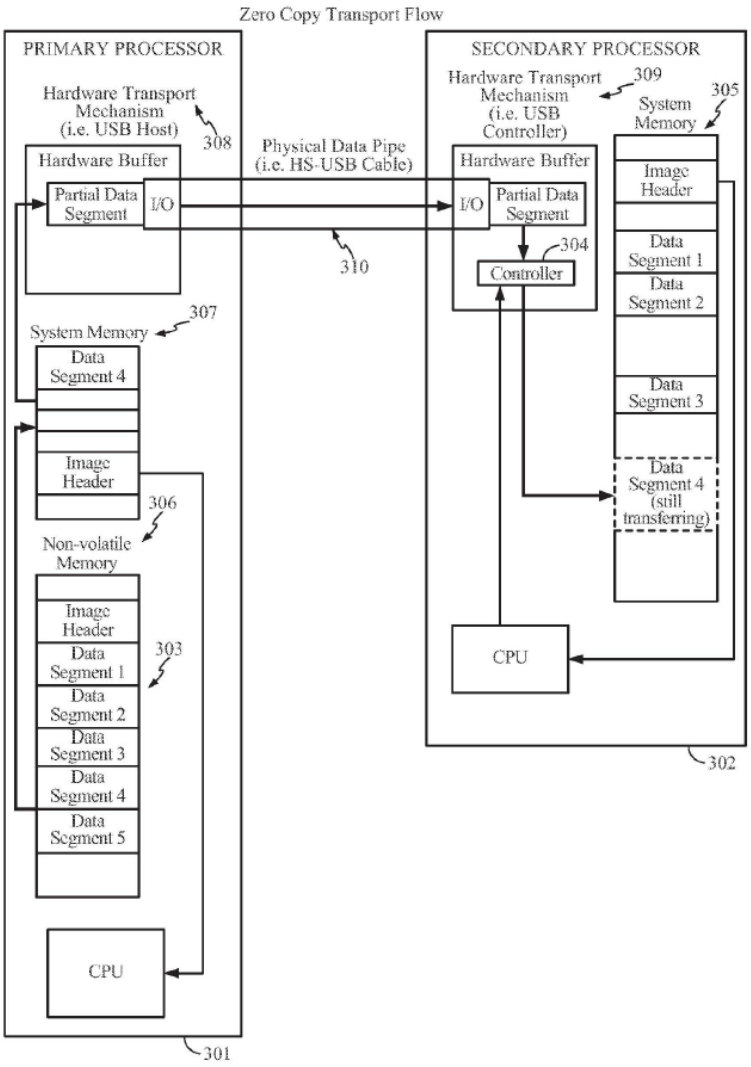

FIG. 3

Figure 3 shows "operational flow for an exemplary loading process for loading an executable image from a primary processor to a secondary processor according to one aspect of the present disclosure." Ex. 1101, 4:10–13. Referring to various components depicted in Figure 3, the '949 patent discloses the following:

> The header information is used by the secondary processor 302 to program the scatter loader/direct memory access controller 304 receive address when receiving the actual executable data. Data segments are then sent from system memory 307 to the primary hardware transport mechanism 308. The segments are then sent from the hardware transport mechanism 308 of the primary processor 301 to a hardware transport mechanism 309 of the secondary processor 302 over an inter-chip communication bus 310 (e.g., a HS-USB cable.) The first segment transferred may be the image header, which contains information used by the secondary processor to locate the data segments into target locations in the system memory of the secondary processor 305. The image header may include information used to determine the target location information for the data.

Ex. 1101, 8:21–35.

Challenged claims 10 and 16 are independent and are reproduced below.

> 10. A method comprising:
>
> receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment, the image header and each data segment being received separately;
>
> processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store each data segment;

receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment; and

scatter loading, by the secondary processor, each data segment [directly[1]] to the determined at least one location within the system memory, and each data segment being scatter loaded based at least in part on the processed image header.

16. An apparatus comprising:

means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment, the image header and each data segment being received separately;

means for processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store each data segment;

means for receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment; and

means for scatter loading, by the secondary processor, each data segment directly to the determined at least one location within the system memory, and each data segment being scatter loaded based at least in part on the processed image header.

D. References

Petitioner relies upon the following references:

Bauer	US 2006/0288019 A1	Dec. 21, 2006	Ex. 1109
Zhao	US 2007/0140199 A1	June 21, 2007	Ex. 1113

[1] The issued patent recites "reedy," which appears to be a printing error. The April 30, 2014 claim listing submitted by the applicants during prosecution states "directly."

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