

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

QUALCOMM, INC.,
Patent Owner.

Case IPR2018-01346
Patent 9,535,490 B2

Before DANIEL N. FISHMAN, DANIEL J. GALLIGAN, and
AARON W. MOORE, *Administrative Patent Judges*.

FISHMAN, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation (“Petitioner”) requests *inter partes* review of claims 9, 11–13, 26, and 27 (the “challenged claims”) of U.S. Patent No. 9,535,490 B2 (“the ’490 patent,” Ex. 1401) pursuant to 35 U.S.C. §§ 311 *et seq.* Paper 3 (“Petition” or “Pet.”). Qualcomm Incorporated (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Upon consideration of the Petition and Patent Owner’s Preliminary Response, we conclude the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one challenged claim of the ’490 patent. Therefore, we institute review of all challenged claims and all asserted grounds.

A. *Real Parties-In-Interest and Related Matters*

Apple Inc. is identified as an additional real party-in-interest. Pet. 1. The parties inform us that the ’490 patent is presently asserted against Petitioner in the litigation *Qualcomm Inc. v. Apple Inc.*, Case No. 3:17-cv-01375-DMS-MDD (S.D. Cal.), and against Apple in a proceeding before the International Trade Commission (“ITC”) captioned *In the Matter of Certain Mobile Electronic Devices and Radio Frequency Components Thereof*, Inv. No. 337-TA-1065. Pet. 1–2; Paper 4, 2. The parties further inform us that the ’490 patent is at issue in *inter partes* review Cases IPR2018-01261, IPR2018-01293, IPR2018-01295, and IPR2018-01344. Pet. 2; Paper 4, 2.

B. The '490 Patent

The '490 patent is generally directed to power saving techniques in computing devices. Ex. 1401, Title (54), Abstract (57). According to the '490 patent, although stationary desktop computers and servers are generally immune to power consumption issues, “mobile devices constantly struggle to find a proper balance between available functions and battery life.” *Id.* at 1:28–31. The '490 patent further indicates that mobile devices utilize internal bus structures to connect components within the mobile device and that increased performance demands have led to use of faster, higher-power-consuming interconnect bus structures within mobile devices (e.g., Peripheral Component Interconnect Express “PCIe” and Universal Serial Bus “USB” 3.0). *Id.* at 1:36–60.

Figure 1C of the '490 patent is reproduced below.

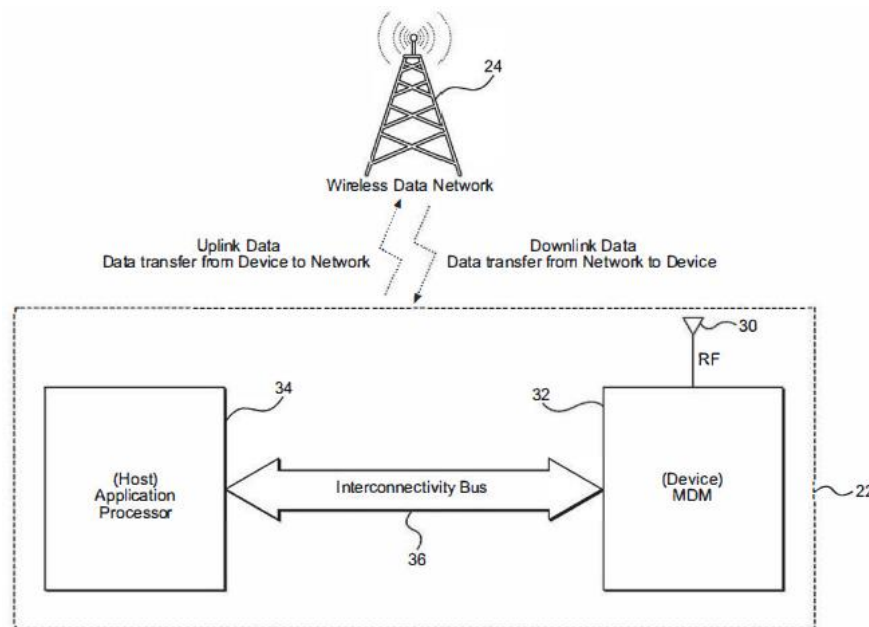


FIG. 1C

Figure 1C is a block diagram of mobile terminal 22 with interconnectivity bus 36 coupling application processor 34 and modem

processor 32. In one embodiment disclosed by the '490 patent, bus 36 may be a PCIe bus. *Id.* at 8:6–9. According to the '490 patent, “[w]hile placing the interconnectivity bus 36 in a sleep mode generally saves power, such sleep modes do have a drawback in that they consume relatively large amounts of power as they transition out of the sleep mode.” *Id.* at 8:9–12.

According to the '490 patent, the PCIe bus can be transitioned from a low power state (e.g., saving battery life) to an active state in which information may be exchanged. *Id.* at 8:23–26. Figure 3 of the '490 patent is reproduced below.

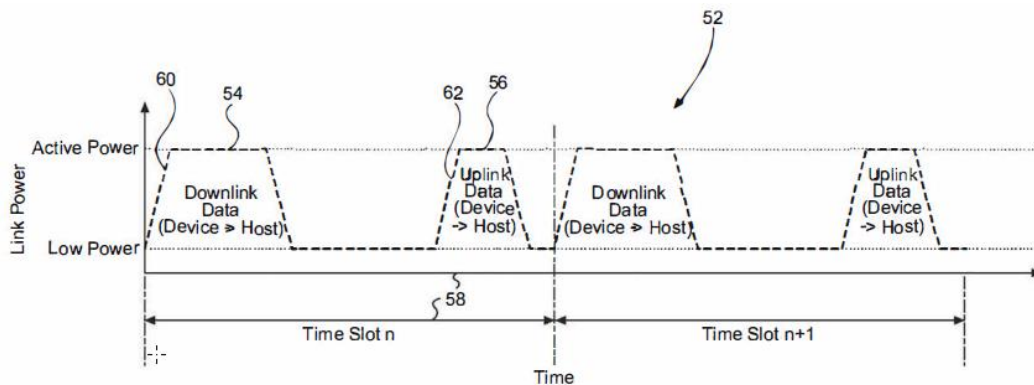


FIG. 3

Figure 3 depicts graph 52, without the purported improvement of the '490 patent, presenting time on the X-axis versus the power state of a PCIe link on the Y-axis. Time is shown as a sequence of time slots 58 (n, n+1, etc.). *Id.* at 8:20. The '490 patent asserts that, within a given time slot 58, exchange of downlink data 54 requires first transition 60 from a low power state to an active power state and back to a low power state, followed by a similar second transition 62 for exchange of uplink data 54. *Id.* at 8:21–34. According to the '490 patent, where the time slot duration is one millisecond, as is common, there may be thousands of such transitions (60,

62) per second. *Id.* at 8:34–38. Thousands of such transitions per second consume a significant amount of power in a battery powered mobile terminal. *Id.* at 8:38–40.

The '490 patent purports to improve battery life by reducing the number of such transitions. Figure 5 of the '490 patent is reproduced below.

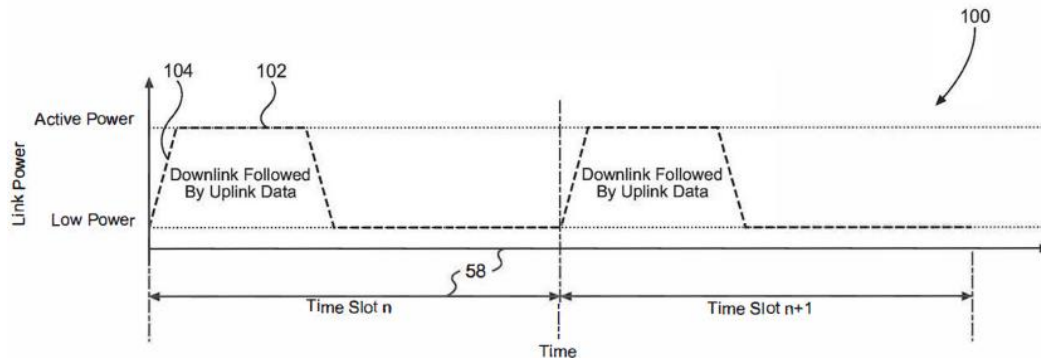


FIG. 5

Figure 5 depicts graph 100, as improved by the purported invention of the '490 patent, presenting time on the X-axis versus the power state of a PCIe link on the Y-axis. According to the '490 patent, combining transmission of downlink data and uplink data during a single active power state period 102 requires only one transition 104 from a low power state to an active power state during a time slot 58. *Id.* at 10:36–40. According to the '490 patent, reducing the number of transitions increases the duration of the low power state in each time slot, thus conserving battery power in a mobile terminal. *Id.* at 10:40–45.

The '490 patent proposes a number of structures and techniques within a mobile terminal for combining uplink and downlink transmissions to reduce the number of low power to active power transitions.

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