

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTEL CORPORATION,  
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,  
Patent Owner.

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Case IPR2018-01404  
Patent No. 7,279,727 B2

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Before MATTHEW R. CLEMENTS, JEFFREY W. ABRAHAM, and  
SCOTT E. BAIN, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
35 U.S.C. § 314(a)

## I. INTRODUCTION

Intel Corp. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1, 10, and 11 of U.S. Patent No. 7,279,727 B2 (Ex. 1003, “the ’727 patent”). Paper 2 (“Pet.”). Godo Kaisha IP Bridge 1 (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

To institute an *inter partes* review, we must determine that the information presented in the Petition shows “a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). For the reasons set forth below, upon considering the Petition and evidence of record, we determine that the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims.

On April 24, 2018, the Supreme Court held that a final written decision under 35 U.S.C. § 318(a) must decide the patentability of all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (2018). Accordingly, we institute *inter partes* review on all of the challenged claims based on all of the grounds identified in the Petition.

Our findings of fact and conclusions discussed below are based on the evidentiary record developed thus far. This decision to institute trial is not a final decision as to the patentability of any challenged claim. Any final decision will be based on the full record developed during trial.

## II. BACKGROUND

### A. *Related Matters*

The parties indicate that the '727 patent is at issue in *Godo Kaisha IP Bridge 1 v. Intel Corp.*, Case No. 2:17-cv-676 (E.D. Tex. Sept. 29, 2017). Pet. 1; Paper 5, 2. Patent Owner also identifies IPR2018-01155, which involves related U.S. Patent No. 7,709,900 B2. Paper 5, 2.

### B. *The '727 Patent*

The '727 Patent, titled “Semiconductor Device,” issued on October 9, 2007. Ex. 1003, at [54], [45]. The object of the '727 patent is “to provide a structure of a semiconductor device which can suppress variations in gate length caused by an optical proximity effect.” *Id.* at 2:58–61. In semiconductor fabrication, the optical proximity effect refers to “the influence of diffracted light[, which] causes a large error between the pattern dimension in the layout design and the actual pattern dimension on the semiconductor substrate.” *Id.* at 1:33–45.

Figures 7A and 7B of the '727 patent, reproduced below, illustrate the problem of the optical proximity effect in the prior art.

FIG. 7A  
PRIOR ART

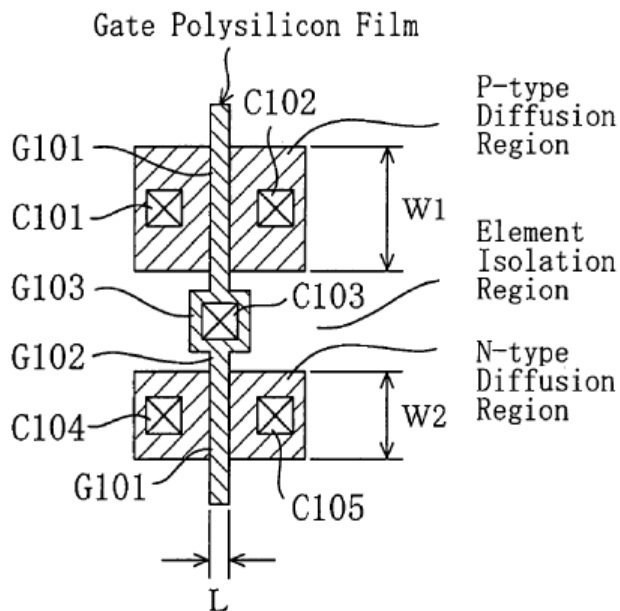
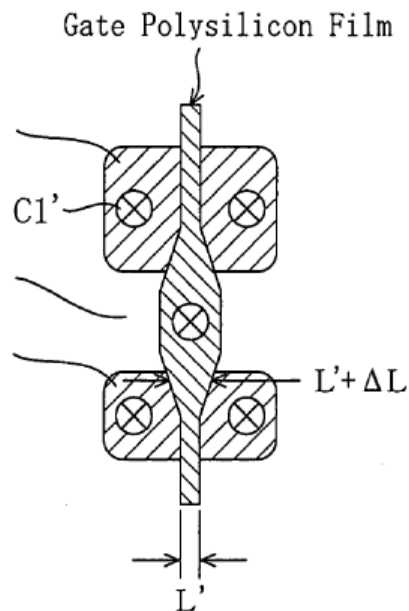


FIG. 7B  
PRIOR ART



Figures 7A and 7B present “a plan view illustrating the design geometry of a known semiconductor device (e.g., standard cell) and a plan view illustrating the geometry of the known semiconductor device after fabricated, respectively.” *Id.* at 2:10–13. As shown in Figure 7, “a gate polysilicon film is provided across a P-type diffusion region and an N-type diffusion region which are surrounded with an element isolation region.” *Id.* at 2:14–17. The part of the film located on the isolation region forms gate interconnect G102, which includes contact pad G103 and contact C103 to connect gate interconnect G102 and an interconnect provided in an upper level. *Id.* at 2:23–28.

Figure 7B shows the resulting device after subjecting the design in Figure 7A to a semiconductor device manufacturing process. *Id.* at 2:36–41.

The '727 patent explains that the “the boundary between the gate interconnect part G102 and the contact pad G103 has a reflex angle rounded under the influence of the optical proximity effect when exposed to light.” *Id.* at 2:42–45. The optical proximity effect also causes an error with respect to the desired gate length. *Id.* at 2:45–49. According to the '727 patent, it was “possible to suppress the error of the gate length caused by the optical proximity effect by keeping a sufficient distance between the contact pad G103 and the diffusion region. However, this increases the area of the semiconductor device, decreases integration density, and hence is not practical.” *Id.* at 2:49–54.

The '727 patent solved the optical proximity effect problem by using a gate conductor film having a constant dimension in the gate length direction, as shown in Figures 1A and 1B. *Id.* at 2:66–3:5.

FIG. 1A

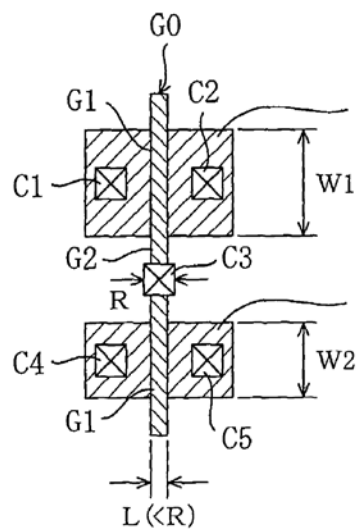
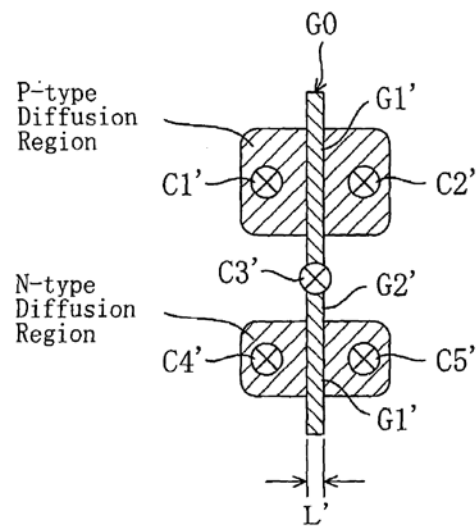


FIG. 1B



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