

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner

v.

QUALCOMM INC.,
Patent Owner.

IPR2018-01460
Patent 9,024,418 B2

Before MICHELLE N. WORMMEESTER, AMANDA F. WIEKER,
and AARON W. MOORE, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge*.

JUDGMENT
FINAL WRITTEN DECISION
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

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I. INTRODUCTION

A. *Background*

Apple Inc. (“Petitioner”) filed a Petition for *inter partes* review of claims 1–5, 8–10, and 12–20 of U.S. Patent No. 9,024,418 B2 (Ex. 1001, “the ’418 patent”). Paper 2 (“Pet.”). Qualcomm Inc. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

On March 15, 2019, we instituted an *inter partes* review of claims 1–5, 8–10, and 12–20. Paper 7 (“Inst. Dec.”) 20. Patent Owner then filed a Patent Owner Response (Paper 20, “PO Resp.”), Petitioner filed a Reply (Paper 36, “Pet. Reply”), and Patent Owner filed a Sur-Reply (Paper 39, “PO Sur-Reply”).

An oral hearing was held on December 12, 2019, and a transcript of the hearing is included in the record. Papers 46, 47 (“Tr.”).

The Board has jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner *has* shown by a preponderance of the evidence that claims 3, 9, 10, and 14 of the ’418 patent are unpatentable, and that Petitioner *has not* shown that claims 1, 2, 4, 5, 8, 12, 13, 15–19, and 20 are unpatentable.

B. *Related Matters*

The ’418 patent was at issue in *Qualcomm Incorporated v. Apple Incorporated*, Civil Action No. 3:17-CV-02402 (S.D. Cal.), when the Petition was filed, but that litigation has since been dismissed. *See* Pet. 1; Petitioner’s Updated Mandatory Notices (Paper 16) 1.

C. The '418 Patent

The '418 patent concerns “[a] local interconnect structure . . . that includes a gate-directed local interconnect coupled to an adjacent gate layer through a diffusion-directed local interconnect.” Ex. 1001, Abstract.

The claimed structure can be explained with reference to Figure 4A, annotated with colors below:

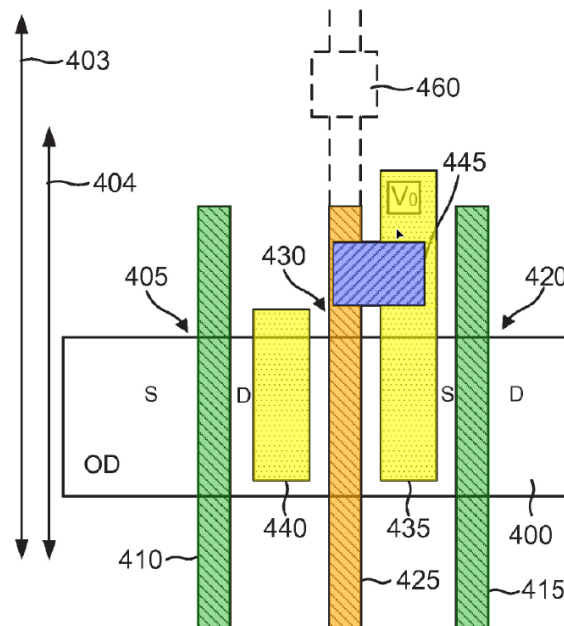


FIG. 4A

Figure 4A shows “the layout for a pair of transistors in a continuous diffusion region including a blocking transistor.” Ex. 1001, 3:9–10.

This embodiment¹ includes continuous diffusion layer 400, which forms the basis for two transistors. The transistors consist of gate layers 410 and 415, shown in green, and the associated source and sink regions in the continuous diffusion layer. An additional gate layer 430, shown in orange, operates as a blocking transistor. The source region for the right transistor is

¹ See Ex. 1001, 5:66–7:3.

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