Trials@uspto.gov
571-272-7822

Paper No. 78
Date: April 30, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROSOFT CORPORATION,
Petitioner,

v.

FG SRC LLC,
Patent Owner.

IPR2018-01600
Patent 6,247,110 B1

Before KALYAN K. DESHPANDE, JUSTIN T. ARBES, and CHRISTA P. ZADO, *Administrative Patent Judges.*

ZADO, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We have authority to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision issues pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Microsoft Corporation ("Petitioner")[1] has shown, by a preponderance of the evidence, that claims 11, 12, 15, and 18–21 ("challenged claims") of U.S. Patent No. 6,247,110 B1 (Ex. 1001, "the '110 patent") are unpatentable. *See* 35 U.S.C. § 316(e) (2012); 37 C.F.R. § 42.1(d) (2017).

A. Procedural History

Petitioner filed a Petition for *inter partes* review of claims 1–7, 11, 12, 15, and 18–21 of the '110 patent. Paper 1 ("Pet." or "Petition"). FG SRC LLC, (Patent Owner")[2] subsequently filed a Preliminary Response. Paper 14 ("Prelim. Resp."). On February 19, 2019, the Board entered a decision instituting an *inter partes* review of all claims and all grounds presented in the Petition. Paper 20 ("Institution Decision" or "Inst. Dec.").

After institution, Patent Owner filed a Response to the Petition. Paper 37 ("Response" or "PO Resp."). In the Response, Patent Owner states that it "surrenders challenged claims . . . 1–7 of the '110 Patent." PO Resp. 4. In addition, on February 11, 2020, Patent Owner filed a statutory disclaimer of claims 1–7 of the '110 patent. Paper 75 (Notice of statutory disclaimer); Ex. 2170 (statutory disclaimer). Accordingly, claims 1–7 have

---

[1] Petitioner identifies only itself as a real party-in-interest to the Petition. Pet. 2.

[2] Saint Regis Mohawk Tribe, originally named as Patent Owner, assigned the '110 patent to DirectStream, LLC on May 21, 2019. Paper 26, 1. DirectStream, LLC assigned the '110 patent to FG SRC LLC on January 22, 2020. Paper 72, 1. Patent Owner identifies only itself as a real party-in-interest to this proceeding. *Id.*

been removed from this proceeding. Petitioner filed a Reply to Patent Owner's Response. Paper 55 ("Reply"). Thereafter, Patent Owner filed a Sur-Reply to Petitioner's Reply to Patent Owner's Response. Paper 61 ("Sur-Reply").

An oral hearing was held on February 3, 2019. A transcript of the hearing is included in the record. Paper 77 ("Tr.").

B. Related Matters

The parties advise that the '110 patent has been subject to, or relates to, the following district court proceedings: *SRC Labs, LLC et al. v. Microsoft Corp.*, 2:18-cv-00321 (W.D. Wash.); and *SRC Labs, LLC et al. v. Microsoft Corp.*, 1:17-cv-01172 (E.D. Va.). Pet. 3; Paper 4, 1. Patent Owner further advises the following proceeding may affect or be affected by this proceeding: *SRC Labs, LLC and Saint Regis Mohawk Tribe v. Amazon Web Services, Inc. et al.*, 2:18-cv-00317 (W.D. Wash.). Paper 72, 1. Also, the following proceedings before the Board involve Petitioner and Patent Owner: IPR2018-01594, IPR2018-01599, IPR2018-01601, IPR2018-01604, and IPR2018-01605.

C. The '110 Patent

The '110 patent relates generally to a multiprocessor computer architecture incorporating multiple programmable memory algorithm processors ("MAP") in a memory subsystem, wherein the MAP may comprise one or more field programmable gate arrays ("FPGAs"). Ex. 1001, code (57).

The specification of the '110 patent ("Specification") describes general purpose computers, stating that they are flexible in that they can handle a variety of functions, but are slower than they would be if they were designed to handle only one particular function:

> All general purpose computers are based on circuits that have some form of processing element. These may take the form of microprocessor chips or could be a collection of smaller chips coupled together to form a processor. In any case, these processors are designed to execute programs that are defined by a set of program steps. The fact that these steps, or commands, can be rearranged to create different end results using the same computer hardware is key to the computer's flexibility. Unfortunately, this flexibility dictates that the hardware then be designed to handle a variety of possible functions, which results in generally slower operation than would be the case were it able to be designed to handle only one particular function. On the other hand, a single function computer is inherently not a particularly versatile computer.

Ex. 1001, 1:22–36. The Specification states, however, that several groups had begun experimenting with creating a processor out of electrically reconfigurable circuits. *Id.* at 1:37–39. According to the Specification, this would allow the processor to be configured to execute particular functions more quickly than a processor of a general purpose computer, thereby accelerating application program execution speeds. *Id.* at 1:39–47. The Specification states, however, that certain functions cannot be implemented well in a system comprising reconfigurable processors due to limitations on the circuit densities that can be achieved. *Id.* In addition, systems including such reconfigurable processors intended for the processors to operate alone, which would present problems in systems involving program applications that use several processors to solve a single problem. *Id.* at 1:47–51.

To address these issues, the Specification states that the inventors "developed a Memory Algorithm Processor ('MAP') multiprocessor computer architecture that utilizes very high performance microprocessors in conjunction with user reconfigurable hardware elements." *Id.* at 1:61–64.

In a preferred embodiment, the MAP may comprise a Field Programmable Gate Array ("FPGA"). *Id.* at 2:2–5. The Specification discloses, particularly, a computer system including a *microprocessor* and one or more FPGAs:

> Particularly disclosed herein is the utilization of one or more FPGAs to perform user defined algorithms in conjunction with, and tightly coupled to, a *microprocessor*. More particularly, in a multi-processor computer system, the FPGAs are globally accessible by all of the system processors for the purpose of executing user definable algorithms.

Id. at 2:6–11 (emphasis added). However, the Specification also discloses, broadly, a computer including a *data processor* and a MAP

> Broadly, what is disclosed herein is a computer including at least *one data processor* for operating on user data in accordance with program instructions. The computer includes at least one memory array presenting a data and address bus and comprises a memory algorithm processor associated with the memory array and coupled to the data and address buses. The memory algorithm processor is configurable to perform at least one identified algorithm on an operand received from a write operation to the memory array.

Id. at 2:37–46 (emphasis added).

Figure 3 of the '110 patent is reproduced below.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.