

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROSOFT CORPORATION,
Petitioner,

v.

FG SRC LLC,
Patent Owner.

IPR2018-01604
Patent 7,421,524 B2

Before KALYAN K. DESHPANDE, JUSTIN T. ARBES, and
CHRISTA P. ZADO, *Administrative Patent Judges*.

DESHPANDE, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background

Microsoft Corporation (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1, 2, and 13–15 of U.S. Patent No. 7,421,524 B2 (Ex. 1001, “the ’524 patent”). Paper 2 (“Pet.”). FG SRC LLC (“Patent Owner”) filed a Preliminary Response pursuant to 35 U.S.C. § 313. Paper 15 (“Prelim. Resp.”).¹

On May 3, 2019, we issued a Decision ordering that “an *inter partes* review is hereby instituted with respect to all grounds set forth in the Petition.” Paper 21 (“Dec.”), 29. After institution, Patent Owner filed a Patent Owner’s Response (Paper 38, “PO Resp.”). In reply, Petitioner filed a Petitioner’s Reply to Patent Owner’s Response (Paper 56, “Pet. Reply”). In response, Patent Owner filed a Patent Owner’s Sur-Reply (Paper 62, “PO Sur-Reply”). Petitioner and Patent Owner also filed Motions to Exclude Evidence (Papers 63 (“Pet. Mot.”), 64 (“PO Mot.”)), Oppositions to the Motions (Papers 65 (“Pet. Opp. Mot.”), 66) and Replies to the Oppositions (Papers 68, 69). Petitioner and Patent Owner presented oral arguments on February 3, 2020, and a transcript has been entered into the record. Paper 75 (“Tr.”).

The Board has jurisdiction under 35 U.S.C. § 6. In this Final Written Decision, after reviewing all relevant evidence and arguments, we determine that Petitioner has met its burden of showing, by a preponderance of the

¹ Saint Regis Mohawk Tribe, originally named as Patent Owner, assigned the ’524 patent to DirectStream, LLC on May 21, 2019. Paper 27, 1. DirectStream, LLC assigned the ’524 patent to FG SRC LLC on January 22, 2020. Paper 73, 1.

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evidence, that claims 1, 2, and 13–15 of the '524 patent are unpatentable. Petitioner's Motion to Exclude is *denied-in-part* and *dismissed-in-part*. Patent Owner's Motion to Exclude is *denied-in-part* and *dismissed-in-part*.

B. Related Proceedings

The parties indicate that the '524 patent currently is involved in *SRC Labs, LLC et al. v. Microsoft Corp.*, Civil Action No. 2-18-cv-00321 (W.D. Wash.), which was transferred from *SRC Labs, LLC et al. v. Microsoft Corp.*, Civil Action No. 1-17-cv-01172 (E.D. Va.). Pet. 3; Prelim. Resp. 4–5. The following proceedings, before the Board, also involve the same parties: IPR2018-01594, IPR2018-01599, IPR2018-01600, IPR2018-01601, IPR2018-01602, IPR2018-01603, IPR2018-01605, IPR2018-01606, and IPR2018-01607.²

C. The '524 Patent (Ex. 1001)

The '524 patent is directed to the field of computer architecture, and, specifically, “a switch/network adapter port (‘SNAP’) for clustered computers employing a chain of multi-adaptive processors (‘MAP[]’) . . . in a dual in-line memory module (‘DIMM’) format.” Ex. 1001, 1:29–37.

A block diagram of an exemplary MAP element is disclosed in Figure 3:

² IPR2018-01602 and IPR2018-01603 have been consolidated with IPR2018-01601. IPR2018-01606 and IPR2018-01607 have been consolidated with IPR2018-01605.

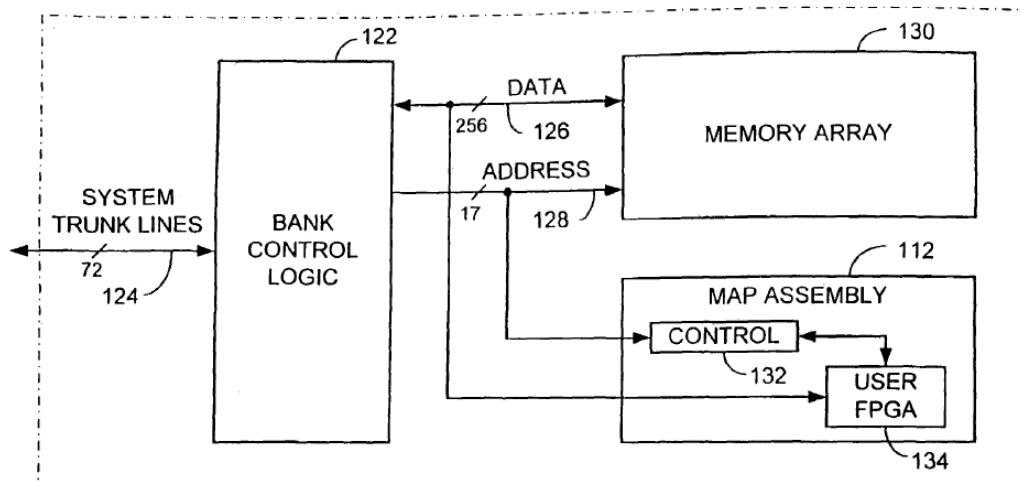


Fig. 3

Figure 3 illustrates memory bank 120 for a MAP element-based system computer architecture (not depicted in Figure 3). *Id.* at 4:60–64. “Each memory bank 120 includes a bank control logic block 122 bi-directionally coupled to the computer system trunk lines, for example, a 72 line bus 124.” *Id.* at 4:64–66. Memory array 130 is coupled to bank control logic 122 via bi-directional data bus 126 and address bus 128. *Id.* at 4:67–5:3. “MAP element 112 comprises a control block 132 coupled to the address bus 128.” *Id.* at 5:5–6. “[C]ontrol block 132 is also bi-directionally coupled to a user field programmable gate array (‘FPGA’),” and “user FPGA 134 is coupled directly to the data bus 126.” *Id.* at 5:6–10. The ’524 patent discloses that MAP element 112 has direct memory access (DMA) capability, which permits it to write to memory, and “it is possible to allow a MAP element 112 to feed results to another MAP element 112 through use of a chain port” because MAP element 112 receives operands via writes to memory. *Id.* at 5:50–54.

Computer system 200 including MAP element 212 in DIMM format is depicted in Figure 5:

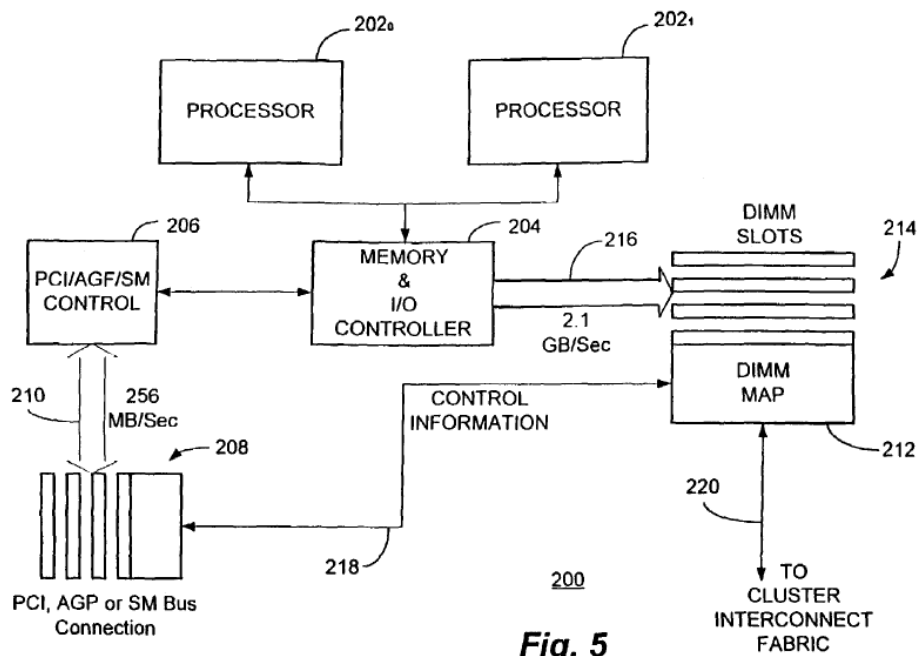


Fig. 5

Figure 5 illustrates “computer system 200 includ[ing] one or more processors 202₀ and 202₁ which are coupled to an associated PC memory and I/O controller 204.” *Id.* at 7:42–45. “[C]ontroller 204 is . . . conventionally coupled to a number of DIMM slots 214 by means of a much higher bandwidth DIMM bus 216 capable of data transfer rates of 2.1 GB/sec. or greater.” *Id.* at 7:56–59. DIMM MAP element 212 is associated with, or physically located within, one of DIMM slots 214, which may be coupled to another clustered computer MAP element by a cluster interconnect fabric connection 220 that is connected to MAP chain ports. *Id.* at 7:59–62, 7:65–8:1.

The ’524 patent discloses that because DIMM MAP element 212 is placed in one of DIMM slots 214, FPGA 134 of DIMM MAP element 212 accepts normal memory “read” and “write” transactions, and converts them to a format used by an interconnect switch or network. *Id.* at 8:13–17. According to the ’524 patent, however, “the electrical protocol of the

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