

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

Case IPR2019-00034
Patent 7,675,806 B2

Before ROBERT J. WEINSCHENK, MINN CHUNG, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

DECISION
Denying Petitioner's Request for Rehearing
37 C.F.R. § 42.71(d)

I. INTRODUCTION

Intel Corporation (“Petitioner”) filed a Request for Rehearing (Paper 12, “Request” or “Req. Reh’g”) of the Decision (Paper 11, “Dec.”), in which, based on the information presented, *inter alia*, in the Petition (Paper 3, “Pet.”), we denied institution of an *inter partes* review of claims 11, 12, 13, 15, and 17 (the “challenged claims”) of U.S. Patent No. 7,675,806 B2 (Ex. 1201, “the ’806 patent”). In its Request, Petitioner contends that the Decision misapprehended or overlooked Petitioner’s argument on how Schuckle (Ex. 1203) teaches certain claim limitations of claim 11. *See* Req. Reh’g 1–3, 6–12. The Request also asserts that the Decision misapprehended certain statements made in the Declaration of Bruce Jacob (Ex. 1202, “Jacob Decl.”). *See id.* at 10–12. In addition, the Request asserts that the Decision denying institution was based on a flawed claim interpretation (*see id.* at 1) of the claim term “first mode of operation” recited in claim 11 (*see id.* at 12–14).

As explained below, we have considered the arguments presented by Petitioner in its Request for Rehearing, but discern no reason to modify the Decision. Consequently, Petitioner’s Request for Rehearing is *denied*.

II. STANDARD OF REVIEW

“The burden of showing a decision should be modified lies with the party challenging the decision,” and the challenging party “must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed” in a paper of record. 37 C.F.R. § 42.71(d). Because Petitioner seeks rehearing of our Decision denying institution of trial based on the Petition, it must show an abuse of discretion. *See* 37 C.F.R. § 42.71(c) (“When rehearing a

decision on petition, a panel will review the decision for an abuse of discretion.”). An abuse of discretion occurs when a “decision was based on an erroneous conclusion of law or clearly erroneous factual findings, or . . . a clear error of judgment.” *PPG Indus., Inc. v. Celanese Polymer Specialties Co.*, 840 F.2d 1565, 1567 (Fed. Cir. 1988). With these principles in mind, we address the arguments presented in Petitioner’s Request.

III. ANALYSIS

Claim 11 recites four separate steps performed by “a processing core.” Ex. 1201, 10:47–57. These limitations are reproduced below with identifying labels used in the Petition:

(11[h]) a processing core located at the integrated circuit, the processing core operable to:

(11[i]) access the first memory and the second memory when in a first mode of operation, and (11[j]) to access the second memory but not the first memory when in a second mode of operation;

(11[k]) access the status information in the second mode of operation; and

(11[l]) enter the first mode of operation in response to the status information indicating data corresponding to the data stored at the first memory has changed.

See Pet. 59, 61, 63, 68, 69.

Based on the arguments and evidence presented in the Petition, the Decision found as follows:

Petitioner maps Schuckle’s “memory controller” (i.e., north bridge or memory controller 140)—*not* processor 110 of Schuckle—to the “processing core” recited in claim 11. [Pet.] 59–60 (citing Ex. 1203, 9:46–57, 10:12–14; Ex. 1202 (Jacob Decl.) ¶¶ 165, 167–168). Petitioner also maps the higher power state (i.e., the C0 or C1 state) of Schuckle to “a first mode of

operation” and the lower power state (i.e., the C2 or C3 state) of Schuckle to “a second mode of operation” recited in claim 11. *Id.* at 61 (citing Ex. 1203, 12:35–38 (claims 2, 3); Ex. 1202 ¶¶ 186–188), 63–64 (citing Ex. 1203, 7:4–19, 10:22–25, 10:43–48; Ex. 1202 ¶ 191).

Dec. 16–17. The Petition’s mapping of “Schuckle’s lower power state” to the claimed “second mode of operation” was based on Petitioner’s proposed construction of the claim term “second mode of operation” to mean “when a lower voltage is provided to the first and second memory.” Pet. 64; *see also id.* at 34–38 (discussing Petitioner’s proposed claim construction of the term “second mode of operation” to mean “when a lower voltage is provided to the first and second memory”). Consistent with these mappings, the Petition identified certain operations performed by Schuckle’s memory controller 140 as the steps performed by the claimed “processing core” recited in limitations 11[i], 11[j], and 11[k]. *Id.* at 61–69.

The Decision also found, based on the arguments and evidence presented in the Petition,

When it comes to limitation 11[l] (reciting “and [the processing core operable to] enter the first mode of operation in response to the status information indicating data corresponding to the data stored at the first memory has changed”), the Petition does not discuss Schuckle’s memory controller entering the first mode of operation, but instead relies on the operations of *processor 110* (rather than memory controller 140) of Schuckle to teach the step recited in limitation 11[l].

Dec. 18–19 (citing Pet. 69–70 (quoting Ex. 1203, 10:58–66, 11:44–53) (citing Ex. 1202 ¶¶ 199–200)). As also discussed in the Decision, in the cited paragraphs of his Declaration, Dr. Jacob similarly identified the operations of *processor 110* as corresponding to the step recited in

limitation 11[1]. *Id.* at 19 (quoting Ex. 1202 ¶¶ 199–200). After considering the argument and evidence presented in the Petition, we determined in the Decision that Petitioner did not demonstrate sufficiently how Schuckle’s memory controller 140 satisfies limitation 11[1] of claim 11. *Id.* at 21.

In its Request for Rehearing, Petitioner contends that the Petition did not rely on Schuckle’s processor 110 to teach limitation 11[1] but instead argued that Schuckle’s *memory controller* 140 performs the step recited in limitation 11[1]. Req. Reh’g 8–12. Specifically, the Request contends that the Petition presented the following argument:

The Petition explains that *memory controller 140*: (1) *exits the second mode of operation* (during which processor 110 and its L2 cache memory are inaccessible because they are in a “lower power” state); and (2) *enters into the first mode of operation* (during which processor 110 and its L2 cache memory are accessible because they are in a “higher power” state) when a cache tag status bit (“status information”) stored in the mirror tag memory indicates that data stored in the L2 cache memory (“first memory”) has changed.

Id. at 8 (emphases added). But the Request does not cite, nor do we discern, where in the Petition this argument was presented.

Although the Request cites page 69 of the Petition as allegedly showing that “*memory controller 140* ‘enter[s] the first mode of operation in response to the status information indicating data corresponding to the data stored at the first memory has changed,’ just as limitation 11[1] requires,” we find no such showing in the cited portion of the Petition. *See id.* (emphasis added) (citing Pet. 69–70).

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