

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

**QUALCOMM INC. AND QUALCOMM TECHNOLOGIES,
INC.,**

Petitioners

v.

APPLE INC.,

Patent Owner

U.S. PATENT NO. 8,271,812

**TITLE: HARDWARE AUTOMATIC PERFORMANCE STATE
TRANSITIONS IN SYSTEM ON PROCESSOR SLEEP AND
WAKE EVENTS**

Issue Date: September 18, 2012

PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312

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I. Introduction

Pursuant to 35 U.S.C. § 312 and 37 C.F.R. § 42.100 *et seq.*, Qualcomm Inc. and Qualcomm Technologies, Inc. (collectively, “Petitioners” or “Qualcomm”) request *inter partes* review of claims 8 and 9 (the “Challenged Claims”) of U.S. Patent No. 8,271,812 (“the ’812 Patent,” Ex. 1001), which is assigned to Apple, Inc. (“Patent Owner” or “Apple”).

The ’812 Patent relates to an integrated circuit, such as a system on chip (“SoC”), which includes one or more performance domains, with each domain having one or more components. Ex. 1001 Abstract, 2:31–34, 3:29–47 and Fig. 1. Among these components are processors, which can have “awake” and “sleep” performance states. *Id.* at 1:35–47, 6:37–50. When a processor is awake, it is supplied with a voltage and a clock signal, and can process instructions. *Id.*; *see also* Ex. 1002 (Declaration of Vijay K. Madiseti, Ph.D), ¶ 40. “In the sleep state, the processor is idle (not executing instructions),” and power is conserved. Ex. 1001, 6:38–39; *see also id.* at 1:35–47 (discussing clock and power gating); Ex. 1002, ¶ 41.

Components can have performance states that are related to whether a processor is awake or asleep. As the ’812 Patent explains:

When the processors are in the sleep state, these other components need not be operating at such a high performance level. Similarly, when the processors are awakened from the sleep state, the performance level at

which the processors and other components need to operate to support the activities being performed by the system may be different than the performance level prior to the processor entering the sleep state.

Ex. 1001, 1:40–47. Accordingly, processors, other non-processor components, and their performance domains may transition between “wake” and “sleep” performance states depending on whether a processor is awake or asleep. *Id.*; Ex. 1002, ¶¶ 42–48. The ’812 Patent further explains that in the prior art, “[t]he sleep/wake transitions of the processors and other components are changed under software control.” Ex. 1001, 1:48–49. However, software control of power management and sleep/wake transitions had purported drawbacks that limited the amount of power conserved and performance of the device. *Id.* at 1:49–58.

The ’812 Patent is directed to “a power management unit (PMU) [that] may automatically transition (in hardware) the performance states of one or more performance domains in a system.” Ex. 1001, Abstract, 1:62–65. According to the specification, “the power management unit may monitor the processor to detect that the processor is entering the sleep state or has entered the sleep state,” and transition performance domains to their “sleep” performance states. *Id.* at 2:3–5, 5:44–49, 9:39–10:2 and Fig. 3 (steps 40, 42, and 44). “[T]he power management unit may [also] be programmable with a second set of target performance states to which the performance domains are to transition when the processor exits the sleep state,” when

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