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de Cesare et al.

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(54) **HARDWARE AUTOMATIC PERFORMANCE STATE TRANSITIONS IN SYSTEM ON PROCESSOR SLEEP AND WAKE EVENTS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(51) **Int. Cl.**

G06F 1/00	(2006.01)
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G06F 3/00	(2006.01)
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G11C 5/14	(2006.01)
H04M 1/00	(2006.01)

(52) **U.S. Cl.**

USPC **713/300**; 713/320; 713/323; 713/324; 345/52; 345/211; 365/227; 455/574; 719/321

(58) **Field of Classification Search** 713/300, 713/320, 323, 324; 345/52, 211; 365/227; 455/574; 719/321

See application file for complete search history.

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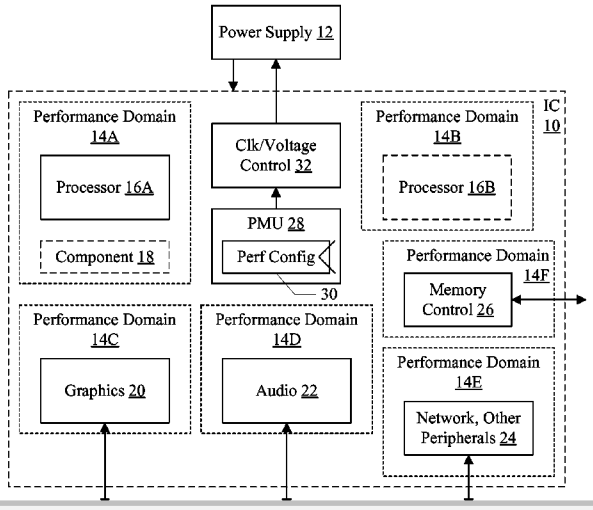
(57) **ABSTRACT**

In an embodiment, a power management unit (PMU) may automatically transition (in hardware) the performance states of one or more performance domains in a system. The target performance states to which the performance domains are to transition may be programmable in the PMU by software, and software may signal the PMU that a processor in the system is to enter the sleep state. The PMU may control the transition of the performance domains to the target performance states, and may cause the processor to enter the sleep state. In an embodiment, the PMU may be programmable with a second set of target performance states to which the performance domains are to transition when the processor exits the sleep state. The PMU may control the transition of the performance domains to the second targeted performance states and cause the processor to exit the sleep state.

24 Claims, 5 Drawing Sheets



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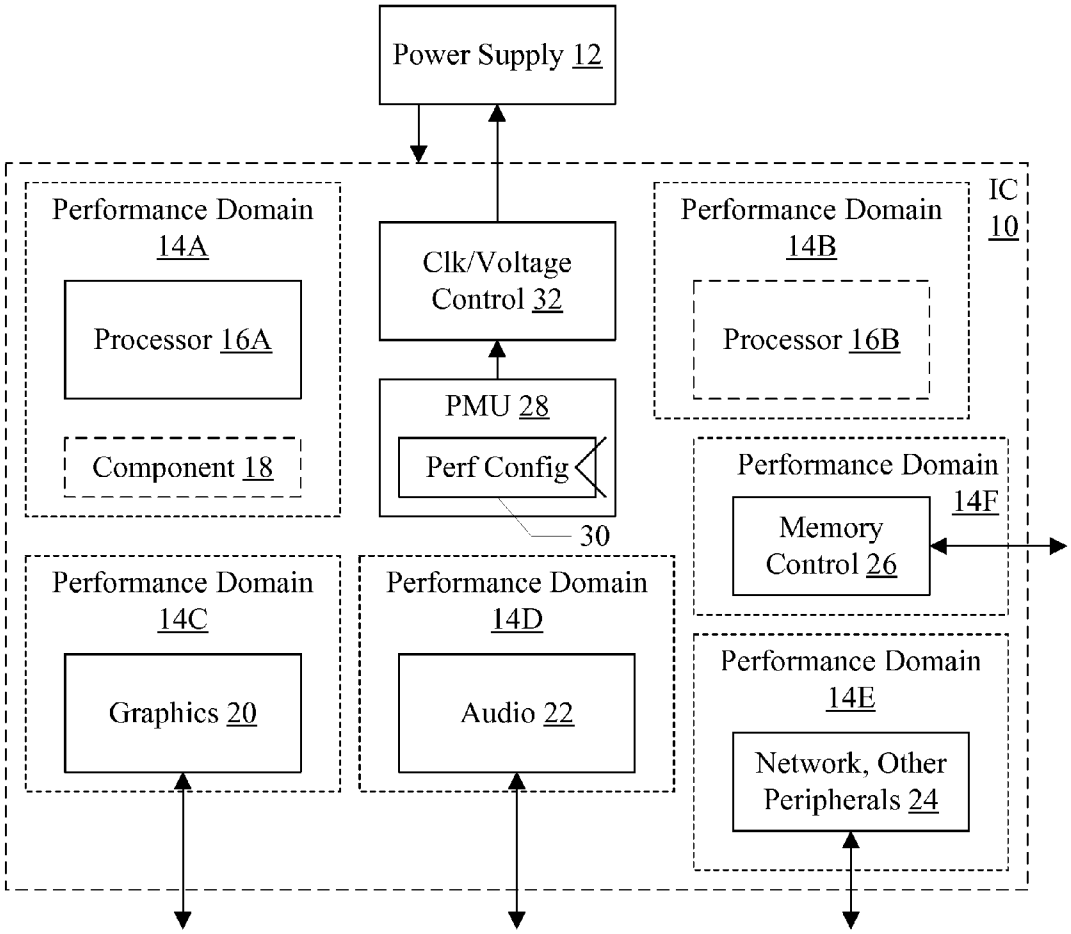

Fig. 1

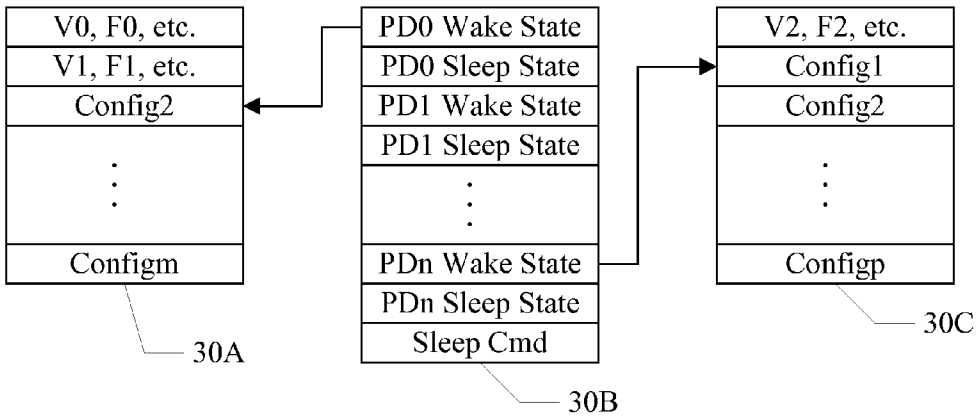

Fig. 2

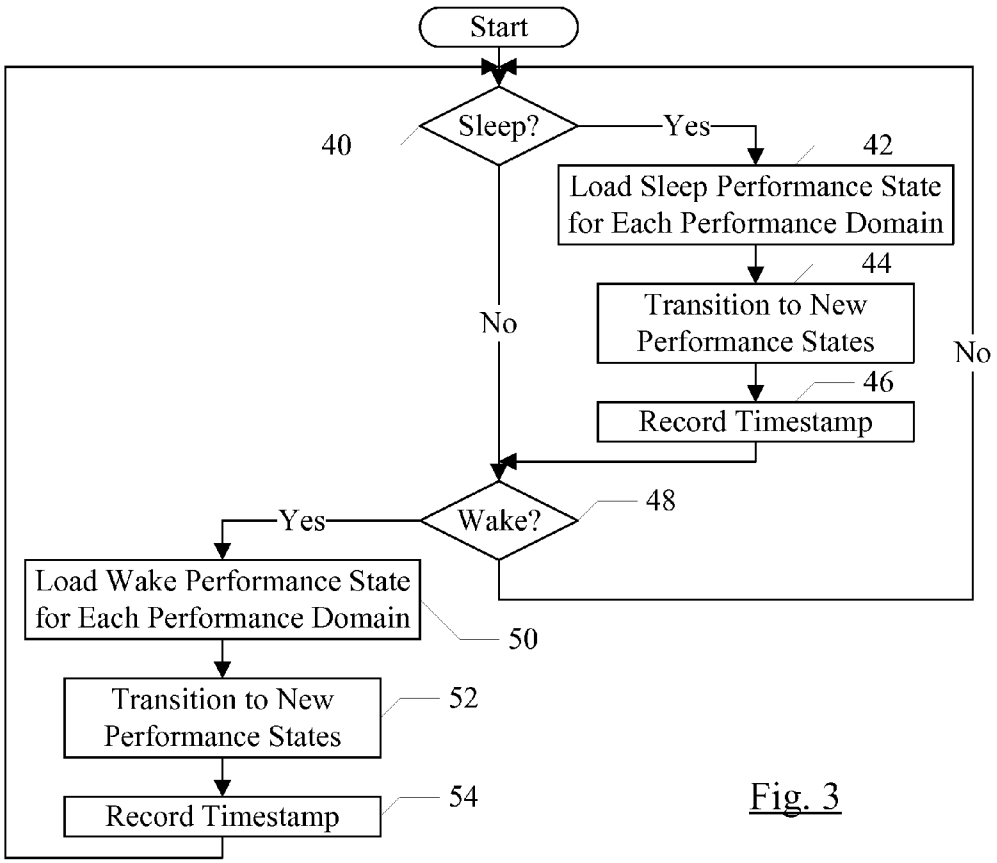

Fig. 3

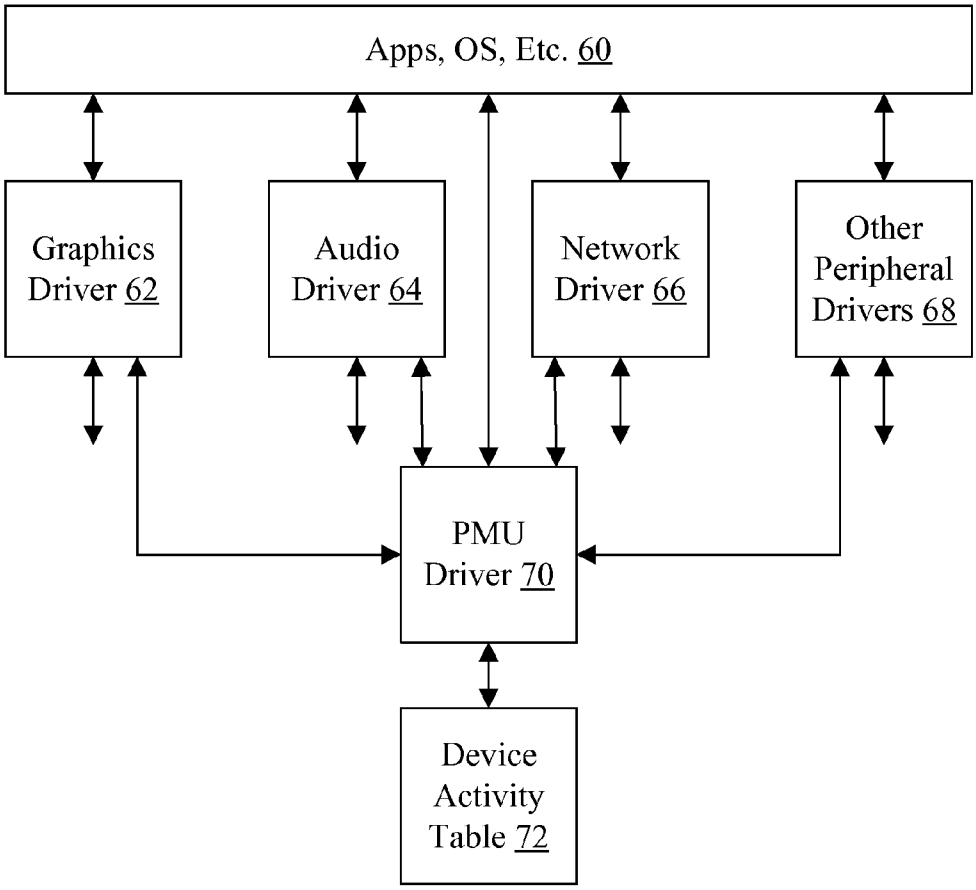

Fig. 4

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