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(54) **METHOD AND APPARATUS FOR CONTROLLING POWER MANAGEMENT STATE TRANSITIONS**

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(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 327 days.

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(51) **Int. Cl.**
G06F 1/32 (2006.01)
G06F 1/00 (2006.01)
G01R 21/06 (2006.01)

(57) **ABSTRACT**

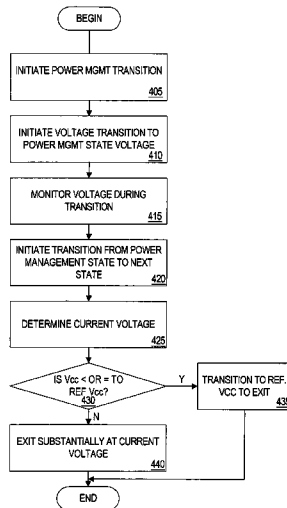
(52) **U.S. Cl.** 713/320; 713/323; 702/60
(58) **Field of Classification Search** 713/320, 713/323, 324; 702/60
See application file for complete search history.

An integrated circuit device, such as a processor initiates a transition to a first power management state. The device then receives a request to exit the first power management state and, in response exits the first power management state at the highest of a reference operating voltage, such as a minimum operating voltage, and a current voltage. For one aspect, an analog to digital converter may be used to determine the current voltage level. Further, for one aspect the first power management state may be a deeper sleep (C4) state, and the processor may quickly exit to a C2 state in response to a bus event such as a bus snoop.

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29 Claims, 8 Drawing Sheets



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Page 2

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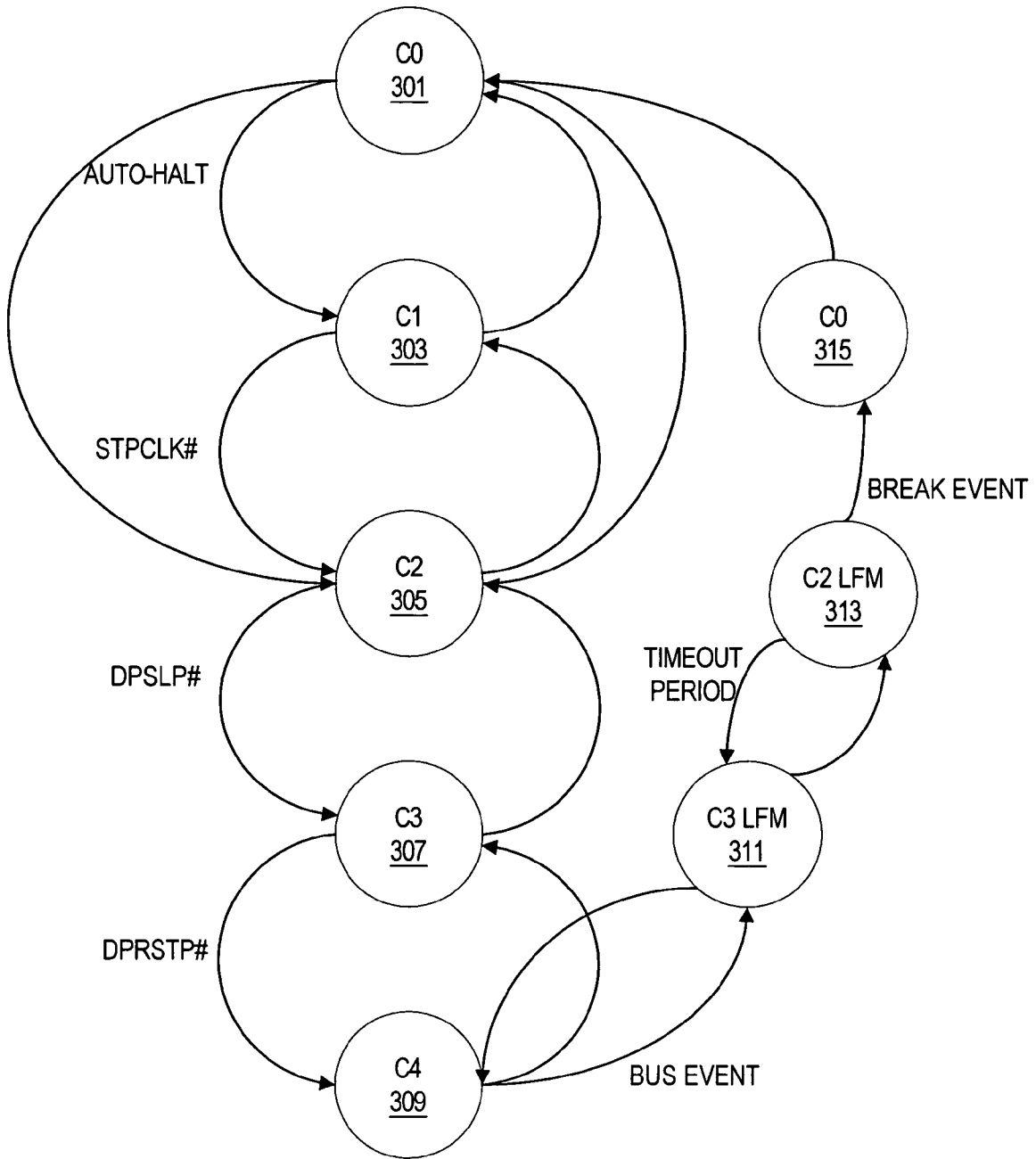


FIGURE 1

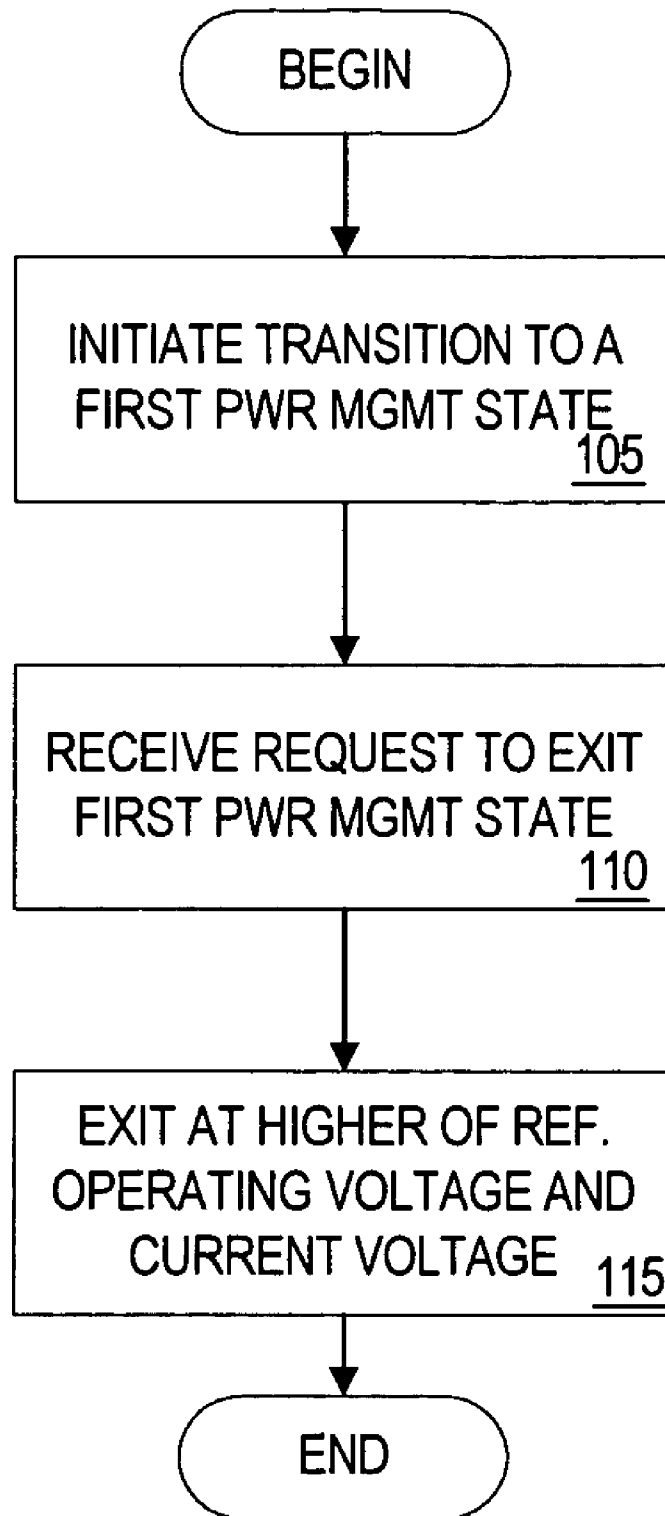


FIGURE 2

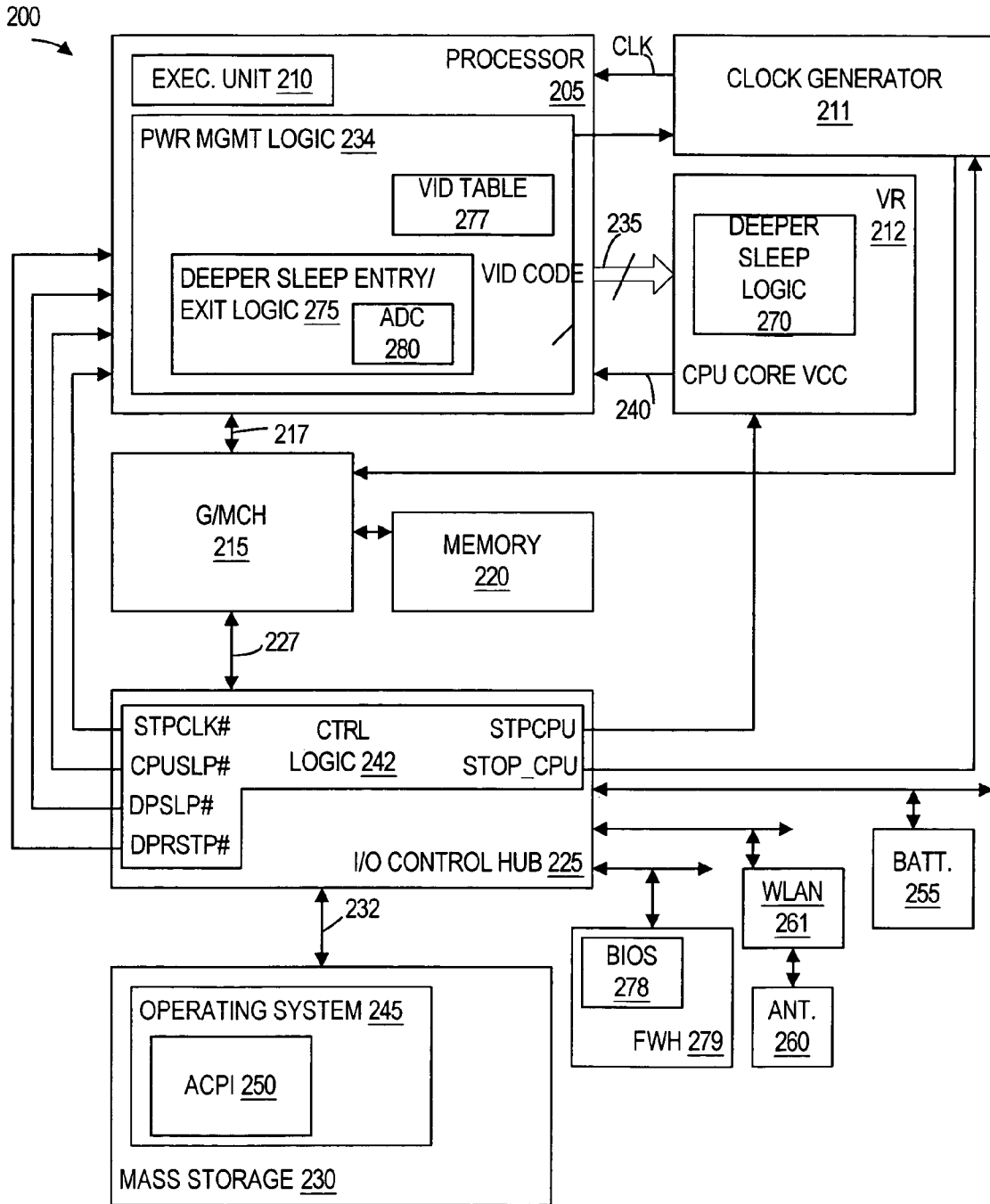


FIGURE 3

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