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(12) United States Patent

Kang et al.

(54) POWER COLLAPSE FOR A WIRELESS TERMINAL

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- (52) U.S. Cl. 455/73; 455/127.5; 455/343.1; 455/574
- (58) Field of Classification Search 455/572–574, 455/343.1–343.4, 127.1, 127.5
 See application file for complete search history.

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(45) **Date of Patent:** May 6, 2008

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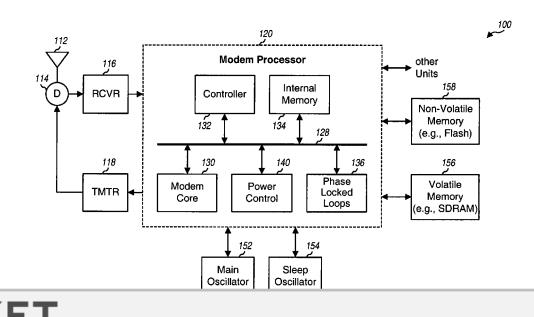
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(57) ABSTRACT

An integrated circuit for a modem processor includes processing units that are partitioned into "always-on" and "collapsible" power domains. An always-on power domain is powered on at all times. A collapsible power domain can be powered off if the processing units in the power domain are not needed. A power control unit within an always-on power domain powers down the collapsible power domains after going into sleep and powers up these domains after waking up from sleep. Tasks for powering down the collapsible power domains may include (1) saving pertinent hardware registers for these power domains, (2) freezing output pins of the IC to minimally disturb external units, (3) clamping input pins of the collapsed power domains, (4) powering down a main oscillator and disabling the oscillator clock, and so on. Complementary tasks are performed for powering up the collapsed power domains.

39 Claims, 6 Drawing Sheets



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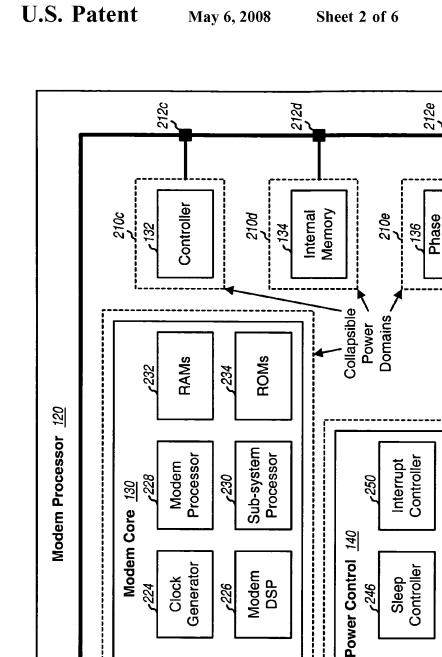
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100 (e.g., SDRAM) Memory (e.g., Flash) Non-Volatile Volatile Memory 158 156 other Units 136 Locked Phase Loops 128 Memory 154 Internal Oscillator Sleep Modem Processor 140 134 Control Power 120 FIG. 152 Oscillator Controller Main 130 ر 192 Modem Core RCVR TMTR 116 118 112 Δ 4 **`KF**

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Processing

Blocks

CDMA

2120

222

2100-

214

Power Domain - Always-On

Controller

Controller

Clock

212a

Power

r 252

r248

Registers

State

210a

-242

Connections

Power

Phase Locked Loops

FIG. 2A

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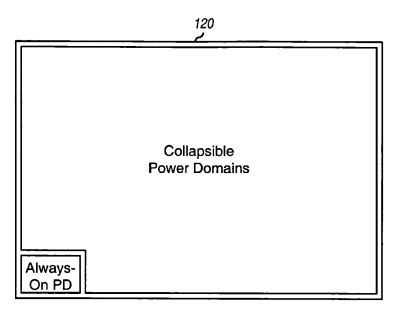
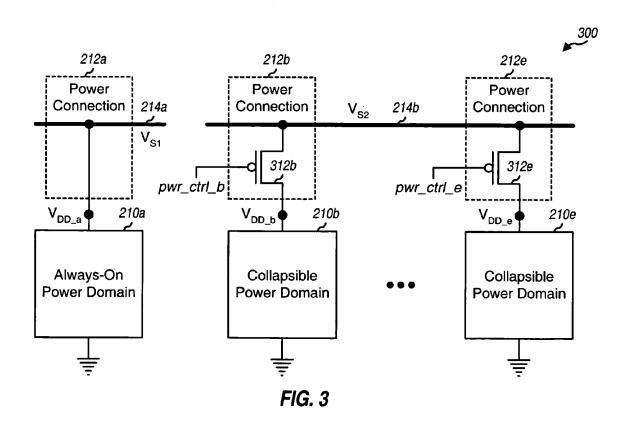
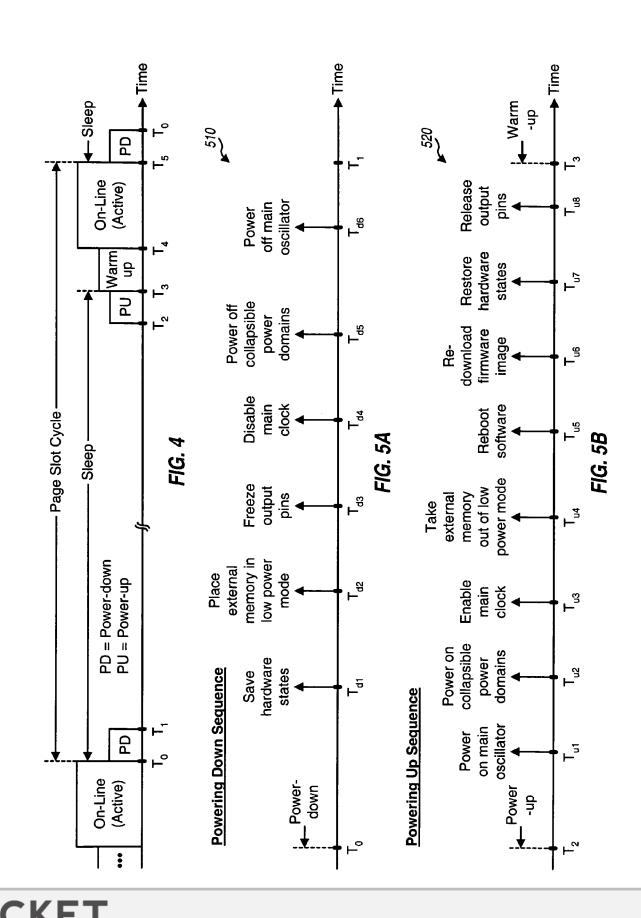


FIG. 2B





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