03-31-03

20040338 .032603

A

Practitioner's Docket No. 915-005.48 ***PATENT***

Preliminary Classification:

Proposed Class:

Subclass:

NOTE: "All applicants are requested to include a preliminary classification on newly filed patent applications. The preliminary classification, preferably class and subclass designations, should be identified in the upper right-hand corner of the letter of transmittal accompanying the application papers, for example 'Proposed Class 2, subclass 129.'" M.P.E.P. § 601, 7th ed.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): KIMMO MYLLY

WARNING: *37 C.F.R. § 1.41(a)(1) points out:*

"(a) A patent is applied for in the name or names of the actual inventor or inventors.

"(1) The inventorship of a nonprovisional application is that inventorship set forth in the oath or declaration as prescribed by § 1.63, except as provided for in § 1.53(d)(4) and § 1.63(d). If an oath or declaration as prescribed by § 1.63 is not filed during the pendency of a nonprovisional application, the inventorship is that inventorship set forth in the application papers filed pursuant to § 1.53(b), unless a petition under this paragraph accompanied by the fee set forth in § 1.17(i) is filed supplying or changing the name or names of the inventor or inventors."

For (title): A METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE

EXPRESS MAILING UNDER 37 C.F.R. § 1.10*
(Express Mail label number is mandatory.)
(Express Mail certification is optional.)

I hereby certify that this paper, along with any document referred to, is being deposited with the United States Postal Service on this date March 26, 2003, in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231 as "Express Mail Post Office to Addressee" Mailing Label No. EV137073922US

Margery B. Hood
(type or print name of person mailing paper)

Margery B. Hood
Signature of person certifying

WARNING: *Certificate of mailing (first class) or facsimile transmission procedures of 37 C.F.R. 1.8 cannot be used to obtain a date of mailing or transmission for this correspondence.*

***WARNING:** Each paper or fee filed by "Express Mail" **must** have the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 C.F.R. 1.10(b).*
*"Since the filing of correspondence under § 1.10 without the Express Mail mailing label thereon is an oversight that can be avoided by the exercise of reasonable care, requests for waiver of this requirement will **not** be granted on petition." Notice of Oct. 24, 1996, 60 Fed. Reg. 56,439, at 56,442.*

1. Type of Application

This new application is for a(n)

(check one applicable item below)

☒ Original (nonprovisional)

☐ Design

☐ Plant

WARNING: ***Do not*** *use this transmittal for a completion in the U.S. of an International Application under 35 U.S.C. § 371(c)(4), unless the International Application is being filed as a divisional, continuation or continuation-in-part application.*

WARNING: ***Do not*** *use this transmittal for the filing of a provisional application.*

NOTE: If one of the following 3 items apply, then complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF A PRIOR U.S. APPLICATION CLAIMED and a NOTIFICATION IN PARENT APPLICATION OF THE FILING OF THIS CONTINUATION APPLICATION.

☐ Divisional.

☐ Continuation.

☐ Continuation-in-part (C-I-P).

2. Benefit of Prior U.S. Application(s) (35 U.S.C. §§ 119(e), 120, or 121)

NOTE: "A nonprovisional application or international application designating the United States of America may claim an invention disclosed in one or more prior-filed copending nonprovisional applications or international applications designating the United States of America. In order for an application to claim the benefit of a prior-filed copending nonprovisional application or international application designating the United States of America, each prior-filed application must name as an inventor at least one inventor named in the later-filed application and disclose the named inventor's invention claimed in at least one claim of the later-filed application in the manner provided by the first paragraph of 35 U.S.C. 112. In addition, each prior-filed application must be:

(i) An international application entitled to a filing date in accordance with PCT Article 11 and designating the United States of America; or

(ii) Complete as set forth in § 1.51(b); or

(iii) Entitled to a filing date as set forth in § 1.53(b) or § 1.53(d) and include the basic filing fee set forth in § 1.16; or

(iv) Entitled to a filing date as set forth in § 1.53(b) and have paid therein the processing and retention fee set forth in § 1.21(l) within the time period set forth in § 1.53(f).

37 C.F.R. § 1.78(a)(1).

WARNING: *If an application claims the benefit of the filing date of an earlier filed application under 35 U.S.C. §§ 120, 121 or 365(c), the 20-year term of that application will be based upon the filing date of the earliest U.S. application that the application makes reference to under 35 U.S.C. §§ 120, 121 or 365(c). (35 U.S.C. § 154(a)(2) does not take into account, for the determination of the patent term, any application on which priority is claimed under 35 U.S.C. §§ 119, 365(a) or 365(b).) For a c-i-p application, applicant should review whether any claim in the patent that will issue is supported by an earlier application and, if not, the applicant should consider canceling the reference to the earlier filed application. The term of a patent is not based on a claim-by-claim approach. See Notice of April 14, 1995, 60 Fed. Reg. 20,195, at 20,205.*

WARNING: *37 C.F.R. § 1.78(a)(2) deals with the time in which the claim for the benefit of an earlier filing date must be made and states:*

"(2)(i) Except for a continued prosecution application filed under § 1.53(d), any nonprovisional application or international application designating the United States of America claiming the benefit of one or more prior-filed copending nonprovisional applications or international applications designating the United States of America must contain or be amended to contain a reference to each such prior-filed application, identifying it by application number (consisting of the series code and serial number) or international application number and international filing date and indicating the relationship of the applications. Cross references to other related applications may be made when appropriate (see § 1.14).

(ii) This reference must be submitted during the pendency of the later-filed application. If the later-filed application is an application filed under 35 U.S.C. 111(a), this reference must also be submitted within the later of four months from the actual filing date of the later-filed application or sixteen months from the filing date of the prior-filed application. If the later-filed application is a nonprovisional application which entered the national stage from an international application after compliance with 35 U.S.C. 371, this reference must also be submitted within the later of four months from the date on which the national stage commenced under 35 U.S.C. 371(b) or (f) in the later-filed international application or sixteen months from the filing date of the prior-filed application. These time periods are not extendable. Except as provided in paragraph (a)(3) of this section, the failure to timely submit the reference required by 35 U.S.C. 120 and paragraph (a)(2)(i) of this section is considered a waiver of any benefit under 35 U.S.C. 120, 121, or 365(c) to such prior-filed application. The time periods in this paragraph do not apply if the later-filed application is:

(A) An application for a design patent;

(B) An application filed under 35 U.S.C. 111(a) before November 29, 2000; or

(C) A nonprovisional application which entered the national stage after compliance with 35 U.S.C. 371 from an international application filed under 35 U.S.C. 363 before November 29, 2000.

(iii) If the later-filed application is a nonprovisional application, the reference required by this paragraph must be included in an application data sheet (§ 1.76), or the specification must contain or be amended to contain such reference in the first sentence following the title.

(iv) The request for a continued prosecution application under § 1.53(d) is the specific reference required by 35 U.S.C. 120 to the prior-filed application. The identification of an application by application number under this section is the identification of every application assigned that application number necessary for a specific reference required by 35 U.S.C. 120 to every such application assigned that application number."

NOTE: If the new application being transmitted is a divisional, continuation or a continuation-in-part of a parent case, or where the parent case is an International Application which designated the U.S., or benefit of a prior provisional application is claimed, then check the following item and complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

☐ The new application being transmitted claims the benefit of prior U.S. application(s). Enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

3. Papers Enclosed

A. Required for filing date under 37 C.F.R. § 1.53(b) (Regular) or 37 C.F.R. § 1.153 (Design) Application

15 Pages of specification

4 Pages of claims

4 Sheets of drawing

WARNING: ***DO NOT*** *submit original drawings. A high quality copy of the drawings should be supplied when filing a patent application. The drawings that are submitted to the Office must be on strong, white, smooth, and non-shiny paper and meet the standards according to § 1.84. If corrections to the drawings are necessary, they should be made to the original drawing and a high-quality copy of the corrected original drawing then submitted to the Office. Only one copy is required or desired. For comments on proposed then-new 37 C.F.R. § 1.84, see Notice of March 9, 1988 (1990 O.G. 57-62).*

NOTE: *"Identification of drawings. Identifying indicia, if provided, should include the title of the invention, inventor's name and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin."*

(complete the following, if applicable)

☐ The enclosed drawing(s) are photograph(s).

NOTE: *37 C.F.R. 1.84*

"(b) Photographs.

"(1) Black and white. Photographs, including photocopies of photographs, are not ordinarily permitted in utility and design patent applications. The Office will accept photographs in utility and design patent applications, however, if photographs are the only practicable medium for illustrating the claimed invention. For example, photographs or photomicrographs of: electrophoresis gels, blots (e.g., immunological, western, Southern, and northern), auto radiographs, cell cultures (stained and unstained), histological tissue cross sections (stained and unstained), animals, plants, in vivo imaging, thin layer chromatography plates, crystalline structures, and, in a design patent application, ornamental effects, are acceptable. If the subject matter of the application admits of illustration by a drawing, the examiner may require a drawing in place of the photograph. The photographs must be of sufficient quality so that all details in the photographs are reproducible in the printed patent.

"(2) Color photographs. Color photographs will be accepted in utility and design patent applications if the conditions for accepting color drawings and black and white photographs have been satisfied. See paragraphs (a)(2) and (b)(1) of this section."

☐ The enclosed drawing(s) are in color. Three (3) sets of color drawings and a "PETITION TO ACCEPT COLOR DRAWING(S)" are attached. 37 C.F.R. §§ 1.84(a)(2) and 1.84(b).

NOTE: *37 C.F.R. 1.84(a)*

"(2) Color. On rare occasions, color drawings may be necessary as the only practical medium by which to disclose the subject matter sought to be patented in a utility or design patent application or the subject matter of a statutory invention registration. The color drawings must be of sufficient quality such that all details in the drawings are reproducible in black and white in the printed patent. Color drawings are not permitted in international applications (see PCT Rule 11.13), or in an application, or copy thereof, submitted under the Office electronic filing system. The Office will accept color drawings in utility or design patent applications and statutory invention registrations only after granting a petition filed under this paragraph explaining why the color drawings are necessary. Any such petition must include the following:

(i) The fee set forth in § 1.17(h);

(ii) Three (3) sets of color drawings;

(iii) A black and white photocopy that accurately depicts, to the extent possible, the subject matter shown in the color drawing; and

(iv) An amendment to the specification to insert (unless the specification contains or has been previously amended to contain) the following language as the first paragraph of the brief description of the drawings:

The patent or application file contains at least one drawing executed in color. Copies of this patent or patent application publication with color drawing(s) will be provided by the Office upon request and payment of the necessary fee."

☒ formal

☐ informal

B. Other Papers Enclosed

2 Pages of declaration and power of attorney

1 Pages of abstract

____ Other

4. Additional papers enclosed

- ☐ Amendment to claims
  - ☐ Cancel in this applications claims _____ before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)
  - ☐ Add the claims shown on the attached amendment. (Claims added have been numbered consecutively following the highest numbered original claims.)
- ☒ Preliminary Amendment
- ☒ Information Disclosure Statement (37 C.F.R. § 1.98)

NOTE: 37 C.F.R. § 1.97 (b) An information disclosure statement shall be considered by the Office if filed by the applicant within any one of the following time periods:

(1) Within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d);

(2) Within three months of the date of entry of the national stage as set forth in § 1.491 in an international application;

(3) Before the mailing of a first Office action on the merits; or

WARNING: *In order to ensure consideration of information previously submitted but which has not been considered in the parent application, an applicant must* ***resubmit*** *the information, complying with 37 C.F.R. § 1.97 and 37 C.F.R. § 1.98, in the continuing application filed under 37 C.F.R. § 1.53(b). See § 609B(3), M.P.E.P., 7th Edition, Rev. 1.*

- ☒ Form PTO–1449 (PTO/SB/08A and 08B)
- ☒ Citations
- ☐ Declaration of Biological Deposit
- ☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
- ☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative
- ☐ Special Comments
- ☐ Other

5. Declaration or oath (including power of attorney)

NOTE: A newly executed declaration is not required in a continuation or divisional application provided that the prior nonprovisional application contained a declaration as required, the application being filed is by all or fewer than all the inventors named in the prior application, there is no new matter in the application being filed, and a copy of the executed declaration filed in the prior application (showing the signature or an indication thereon that it was signed) is submitted. The copy must be accompanied by a statement requesting deletion of the names of person(s) who are not inventors of the application being filed. If the declaration in the prior application was filed under § 1.47, then a copy of that declaration must be filed accompanied by a copy of the decision granting § 1.47 status or, if a nonsigning person under § 1.47 has subsequently joined in a prior application, then a copy of the subsequently executed declaration must be filed. See 37 C.F.R. §§ 1.63(d)(1)–(3).

NOTE: A declaration filed to complete an application must be executed, identify the specification to which it is directed, identify each inventor by full name including family name and at least one given name, without abbreviation together with any other given name or initial, and the residence, post office address and country or citizenship of each inventor, and state whether the inventor is a sole or joint inventor. 37 C.F.R. § 1.63(a)(1)–(4).

NOTE: "The inventorship of a nonprovisional application is that inventorship set forth in the oath or declaration as prescribed by § 1.62, except as provided for in § 1.53(d)(4) and § 1.63(d). If an oath or declaration as prescribed by § 1.63 is not filed during the pendency of a nonprovisional application, the inventorship is that inventorship set forth in the application papers filed pursuant to § 1.53(b), unless a petition under this paragraph accompanied by the fee set forth in § 1.17(i) is filed supplying or changing the name or names of the inventor or inventors." 37 C.F.R. § 1.41(a)(1).

☒ Enclosed

Executed by

(check **all** *applicable boxes)*

☒ inventor(s).

☐ legal representative of inventor(s). 37 C.F.R. §§ 1.42 or 1.43.

☐ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.

☐ This is the petition required by 37 C.F.R. § 1.47 and the statement required by 37 C.F.R. § 1.47 is also attached. See item 13 below for fee.

☐ Not Enclosed.

NOTE: Where the filing is a completion in the U.S. of an International Application or where the completion of the U.S. application contains subject matter in addition to the International Application, the application may be treated as a continuation or continuation-in-part, as the case may be, utilizing ADDED PAGE FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION CLAIMED.

☐ Application is made by a person authorized under 37 C.F.R. § 1.41(c) on behalf of *all* the above named inventor(s).

(The declaration or oath, along with the surcharge required by 37 C.F.R. § 1.16(e) can be filed subsequently).

☐ Showing that the filing is authorized.
(not required unless called into question. 37 C.F.R. § 1.41(d))

6. Inventorship Statement

WARNING: *If the named inventors are each not the inventors of all the claims an explanation, including the ownership of the various claims at the time the last claimed invention was made, should be submitted.*

The inventorship for all the claims in this application are:

☐ The same.

or

☐ Not the same. An explanation, including the ownership of the various claims at the time the last claimed invention was made,

☐ is submitted.

☐ will be submitted.

7. Language

NOTE: An application including a signed oath or declaration may be filed in a language other than English. An English translation of the non-English language application and the processing fee of $130.00 required by 37 C.F.R. § 1.17(k) is required to be filed with the application, or within such time as may be set by the Office. 37 C.F.R. § 1.52(d).

☒ English

☐ Non-English

☐ The attached translation includes a statement that the translation is accurate. 37 C.F.R. § 1.52(d).

8. Assignment

☒ An assignment of the invention to Nokia Corporation

☒ is attached. A separate ☐ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☒ FORM PTO 1595 is also attached.

☐ will follow.

NOTE: "If an assignment is submitted with a new application, send two separate letters-one for the application and one for the assignment." Notice of May 4, 1990 (1114 O.G. 77-78).

WARNING: *A newly executed "CERTIFICATE UNDER 37 C.F.R. § 3.73(b)" must be filed when a continuation-in-part application is filed by an assignee. Notice of April 30, 1993, 1150 O.G. 62-64.*

☐ This is a ☐ continuation ☐ divisional application and the assignment document for the parent application 0 /_____ was filed on _____.

Reel _____

Frame _____

9. Certified Copy

Certified copy(ies) of application(s)

Country	Appln. No.	Filed
Finland	20020594	March 27, 2002
Country	Appln. No.	Filed
Country	Appln. No.	Filed

from which priority is claimed

☒ is (are) attached.

☐ will follow.

NOTE: 37 C.F.R. § 1.55 Claim for foreign priority.

"(a) • • •

(1)(i) In an original application filed under 35 U.S.C. 111(a), the claim for priority must be presented during the pendency of the application, and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior foreign application. This time period is not extendable. The claim must identify the foreign application for which priority is claimed, as well as any foreign application for the same subject matter and having a filing date before that of the application for which priority is claimed, by specifying the application number, country (or intellectual property authority), day, month, and year of its filing. The time periods in this paragraph do not apply in an application under 35 U.S.C. 111(a) if the application is:

(A) A design application; or

(B) An application filed before November 29, 2000.

• • • • •

(c) Unless such claim is accepted in accordance with the provisions of this paragraph, any claim for priority under 35 U.S.C. 119(a)-(d) or 365(a) not presented within the time period provided by paragraph (a) of this section is considered to have been waived. If a claim for priority under 35 U.S.C. 119(a)-(d) or 365(a) is presented after the time period provided by paragraph (a) of this section, the claim may be accepted if the claim identifying the prior foreign application by specifying its application number, country (or intellectual property authority), and the day, month, and year of its filing was unintentionally delayed. A petition to accept a delayed claim for priority under 35 U.S.C. 119(a)-(d) or 365(a) must be accompanied by:

(1) The claim under 35 U.S.C. 119(a)-(d) or 365(a) and this section to the prior foreign application, unless previously submitted;

(2) The surcharge set forth in § 1.17(t); and

(3) A statement that the entire delay between the date the claim was due under paragraph (a)(1) of this section and the date the claim was filed was unintentional. The Commissioner may require additional information where there is a question whether the delay was unintentional."

NOTE: 37 C.F.R. § 1.63 Oath or declaration.

"(a) An oath or declaration filed under § 1.51(b)(2) as a part of a nonprovisional application must:

* * * *

(c) Unless such information is supplied on an application data sheet in accordance with § 1.76, the oath or declaration must also identify:

(2) Any foreign application for patent (or inventor's certificate) for which a claim for priority is made pursuant to § 1.55, and any foreign application having a filing date before that of the application on which priority is claimed, by specifying the application number, country, day, month, and year of its filing."

The foreign application forming the basis for the claim for priority must be referred to in the oath or declaration. 37 C.F.R. § 1.55(a) and 1.63.

NOTE: This item is for any foreign priority for which the application being filed directly relates. If any parent U.S. application or International Application from which this application claims benefit under 35 U.S.C. § 120 is itself entitled to priority from a prior foreign application, then complete item 18 on the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

10. Fee Calculation (37 C.F.R. § 1.16)

A. ☒ Regular application

CLAIMS AS FILED					
Number filed		Number Extra		Rate	Basic Fee 37 C.F.R. § 1.16(a) ~~$740.00~~ $750.00
Total Claims (37 C.F.R. § 1.16(c))	26 – 20 =	6	×	$ 18.00	108.00
Independent Claims (37 C.F.R. § 1.16(b))	4 – 3 =	1	×	$ 84.00	84.00
Multiple dependent claim(s), if any (37 C.F.R. § 1.16(d))			+	$280.00	

☐ Amendment cancelling extra claims is enclosed.

☐ Amendment deleting multiple-dependencies is enclosed.

☐ Fee for extra claims is not being paid at this time.

NOTE: If the fees for extra claims are not paid on filing they must be paid or the claims cancelled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency. 37 C.F.R. § 1.16(d).

Filing Fee Calculation $ 942.00

B. ☐ Design application
($330.00—37 C.F.R. § 1.16(f))

Filing Fee Calculation $ _____

C. ☐ Plant application
($510.00—37 C.F.R. § 1.16(g))

Filing fee calculation $ _____

11. Assertion of Small Entity Status

☐ Applicant hereby asserts status as a small entity under 37 C.F.R. § 1.27

NOTE: 37 C.F.R. § 1.27(c) deals with the assertion of small entity status, whether by a written specific declaration thereof or by payment as a small entity of the basic filing fee or the fee for the entry into the national phase and states:

"(c) Assertion of small entity status. Any party (person, small business concern or nonprofit organization) should make a determination, pursuant to paragraph (f) of this section, of entitlement to be accorded small entity status based on the definitions set forth in paragraph (a) of this section, and must, in order to establish small entity status for the purpose of paying small entity fees, actually make an assertion of entitlement to small entity status, in the manner set forth in paragraphs (c)(1) or (c)(3) of this section, in the application or patent in which such small entity fees are to be paid.

(1) Assertion by writing. Small entity status may be established by a written assertion of entitlement to small entity status. A written assertion must:

(i) Be clearly identifiable;

(ii) Be signed (see paragraph (c)(2) of this section); and

(iii) Convey the concept of entitlement to small entity status, such as by stating that applicant is a small entity, or that small entity status is entitled to be asserted for the application or patent. While no specific words or wording are required to assert small entity status, the intent to assert small entity status must be clearly indicated in order to comply with the assertion requirement.

(2) Parties who can sign and file the written assertion. The written assertion can be signed by:

(i) One of the parties identified in § 1.33(b) (e.g., an attorney or agent registered with the Office), § 3.73(b) of this chapter notwithstanding, who can also file the written assertion;

(ii) At least one of the individuals identified as an inventor (even though a § 1.63 executed oath or declaration has not been submitted), notwithstanding § 1.33(b)(4), who can also file the written assertion pursuant to the exception under § 1.33(b) of this part; or

(iii) An assignee of an undivided part interest, notwithstanding §§ 1.33(b)(3) and 3.73(b) of this chapter, but the partial assignee cannot file the assertion without resort to a party identified under § 1.33(b) of this part.

(3) Assertion by payment of the small entity basic filing or basic national fee. The payment, by any party, of the exact amount of one of the small entity basic filing fees set forth in §§ 1.16(a), (f), (g), (h), or (k), or one of the small entity basic national fees set forth in §§ 1.492(a)(1), (a)(2), (a)(3), (a)(4), or (a)(5), will be treated as a written assertion of entitlement to small entity status even if the type of basic filing or basic national fee is inadvertently selected in error.

(i) If the Office accords small entity status based on payment of a small entity basic filing or basic national fee under paragraph (c)(3) of this section that is not applicable to that application, any balance of the small entity fee that is applicable to that application will be due along with the appropriate surcharge set forth in § 1.16(e), or § 1.16(l).

(ii) The payment of any small entity fee other than those set forth in paragraph (c)(3) of this section (whether in the exact fee amount or not) will not be treated as a written assertion of entitlement to small entity status and will not be sufficient to establish small entity status in an application or a patent."

WARNING: *37 C.F.R. § 1.27(c)(4): "Assertion required in related, continuing, and reissue applications. Status as a small entity must be specifically established by an assertion in each related, continuing and reissue application in which status is appropriate and desired. Status as a small entity in one application or patent does not affect the status of any other application or patent, regardless of the relationship of the applications or patents. The refiling of an application under § 1.53 as a continuation, divisional, or continuation-in-part application (including a continued prosecution application under § 1.53(d)), or the filing of a reissue application, requires a new assertion as to continued entitlement to small entity status for the continuing or reissue application."*

WARNING: *"Small entity status must not be established when the person or persons signing the . . . statement can **unequivocally** make the required self-certification." M.P.E.P., § 509.03 (emphasis added).*

(complete the following, if applicable)

☐ Status as a small entity was asserted in the prior application

_____ / _____, filed on _____, from which benefit is being claimed for this application under:

35 U.S.C. § ☐ 119(e)
☐ 120
☐ 121
☐ 365(c)

and which status as a small entity is still proper and asserted for this application.

☐ A copy of the written assertion of small entity filed in the prior application is included.

NOTE: *A refund based on establishment of small entity status, of a portion of fees timely paid in full prior to establishing status as a small entity may only be obtained if an assertion under § 1.27(c) and a request for a refund of the excess amount are filed within three months of the date of the timely payment of the full fee. The three-month time period is not extendable under § 1.136. 37 C.F.R. § 1.28(a).*

Filing Fee Calculation (50% of **A, B** or **C** above)

$ _____

12. Request for International-Type Search (37 C.F.R. § 1.104(d))

(complete, if applicable)

☐ Please prepare an international-type search report for this application at the time when national examination on the merits takes place.

13. Fee Payment Being Made at This Time

☐ Not Enclosed

☐ No filing fee is to be paid at this time.
(This and the surcharge required by 37 C.F.R. § 1.16(e) can be paid subsequently.)

☒ Enclosed

☒ Filing fee	$ 942.00
☒ Recording assignment ($40.00; 37 C.F.R. § 1.21(h)) (See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION".)	$ 40.00
☐ Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached ($130.00; 37 C.F.R. §§ 1.47 and 1.17(i))	$ _____
☐ For processing an application with a specification in a non-English language ($130.00; 37 C.F.R. §§ 1.52(d) and 1.17(k))	$ _____
☐ Processing and retention fee ($130.00; 37 C.F.R. §§ 1.53(d) and 1.21(l))	$ _____
☐ Fee for international-type search report ($40.00; 37 C.F.R. § 1.21(e))	$ _____

NOTE: 37 C.F.R. § 1.21(l) establishes a fee for processing and retaining any application that is abandoned for failing to complete the application pursuant to 37 C.F.R. § 1.53(f) and this, as well as the changes to 37 C.F.R. §§ 1.53 and 1.78(a)(1), indicate that in order to obtain the benefit of a prior U.S. application, either the basic filing fee must be paid, or the processing and retention fee of § 1.21(l) must be paid, within 1 year from notification under § 53(f).

Total fees enclosed $ 982.00

14. Method of Payment of Fees

☒ Attached is a ☒ check ☐ money order in the amount of $ 982.00

☐ Authorization is hereby made to charge the amount of $ _____

☐ to Deposit Account No. _____

☐ to Credit card as shown on the attached credit card information authorization form PTO-2038.

WARNING: *Credit card information should **not** be included on this form as it may become public.*

☒ Charge any additional fees required by this paper or credit any overpayment ~~in the manner authorized above~~. to Deposit Account No. 23-0442.

A duplicate of this paper is attached.

15. Authorization to Charge Additional Fees

WARNING: *If no fees are to be paid on filing, the following items should not be completed.*

WARNING: *Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges, if extra claim charges are authorized.*

WARNING: *Even though small entity status is accorded where the wrong type of small entity basic filing fee or basic national fee is selected but the exact amount of the fee is paid, applicant still needs to pay the correct small entity amount for the basic filing or basic national fee where selection of the wrong type of fee results in a deficiency. While an accompanying general authorization to charge any additional fees suffices to pay the balance due of the proper small entity basic filing or basic national fee, specific authorizations to charge fees under § 1.17 or extension of time fees do not suffice to pay any balance due of the proper small entity basic filing or basic national fee because they do not actually authorize payment of small entity amounts. Changes To Implement the Patent Business Goals; Final Rule [Fed. Reg.: September 8, 2000, pages 54603-54683, at 54611; OG: October 3, 2000, pages 14-39].*

☒ The Office is hereby authorized to charge, in the manner shown above, the following additional fees that may be required by this paper and during the entire pendency of this application.

- ☒ 37 C.F.R. § 1.16(a), (f) or (g) (filing fees)
- ☐ 37 C.F.R. § 1.16(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 C.F.R. § 1.16(d)), it might be best not to authorize the PTO to charge additional claim fees, except possibly when dealing with amendments after final action.

- ☐ 37 C.F.R. § 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)
- ☐ 37 C.F.R. § 1.17(a)(1)–(5) (extension fees pursuant to § 1.136(a)).
- ☐ 37 C.F.R. § 1.17 (application processing fees)

NOTE: ". . .A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. An authorization to charge all required fees, fees under § 1.17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission. Submission of the fee set forth in § 1.17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C.F.R. § 1.136(a)(3).

- ☐ 37 C.F.R. § 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. § 1.311(b))

*NOTE: Section 1.311(b) provides that an authorization to charge the issue fee (§ 1.18) to a deposit account may be filed in an individual application **only after the mailing of the notice of allowance.** Accordingly, general authorizations to pay fees and specific authorizations to pay the issue fee that are filed prior to the mailing of a notice of allowance will generally not be treated as requesting payment of the issue fee and will not be given effect to act as a reply to the notice of allowance. Applicant, when paying the issue fee, should submit a new authorization to charge fees, such as by completing box 6b on the current PTOL-85B form. Where no reply to the notice of allowance is received, the application will stand abandoned notwithstanding the presence of general authorizations to pay fees or a specific authorization to pay the issue fee that were submitted prior to mailing of the notice of allowance. Where an attempt is made to pay the issue fee but an incorrect amount is submitted, § 1.311(b)(1), or where the Office's issue fee transmittal form (currently PTOL-85(B)) is completed by applicant and submitted, § 1.311(b)(2), in reply to a notice of allowance, an exception will be made. Such submissions will operate as a request to charge the issue fee to any deposit account identified in a previously filed (i.e., submitted prior to the mailing of the notice of allowance) authorization to charge fees, and will be allowed to act as payment of the correct issue fee. § 1.311(b). See also the change to § 1.26(b). Notice of September 8, 2000, Fed. Reg. 54603-54683, at 54646 and 54647.*

NOTE: *37 C.F.R. § 1.28(b) requires "Notification of any change in status resulting in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying, . . . the issue fee. . . " From the wording of 37 C.F.R. § 1.28(b), (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.*

16. Instructions as to Overpayment

NOTE: *". . . Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C.F.R. § 1.26(a).*

- [x] Credit Account No. 23-0442
- [ ] Refund

Francis J. Maguire (signature)

SIGNATURE OF PRACTITIONER

Reg. No. 31,391

Francis J. Maguire
Ware, Fressola, Van Der Sluys & Adolphson LLP

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☐ **Incorporation by reference of added pages**

(check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED)

☐ Plus Added Pages for New Application Transmittal Where Benefit of Prior U.S. Application(s) Claimed

Number of pages added _____

☐ Plus Added Pages for Papers Referred to in Item 4 Above

Number of pages added _____

☐ Plus added pages deleting names of inventor(s) named in prior application(s) who is/are no longer inventor(s) of the subject matter claimed in this application.

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☐ Plus "Assignment Cover Letter Accompanying New Application"

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☒ **Statement Where No Further Pages Added**

(if no further pages form a part of this Transmittal, then end this Transmittal with this page and check the following item)

☒ This transmittal ends with this page.

915-005.48

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of :

Kimmo Mylly :

Filed: Herewith :

For: A METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE

PRELIMINARY AMENDMENT A

Assistant Commissioner for Patents
U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Please preliminarily amend the above-referenced application as follows:

FILING OF PAPERS AND FEES BY "EXPRESS MAIL"
WITH CERTIFICATE IN ACCORDANCE WITH 37 CFR 1.10

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as "Express Mail" in an envelope with Mailing Label No. EV137073922US placed thereon prior to mailing and addressed to the U.S. Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202.

Margery B. Hood

Margery B. Hood

Dated: March 26, 2003

IN THE SPECIFICATION:

The paragraph beginning at page 3, line 6 has been amended as follows:

--In said MultiMediaCard Association, a maximum limit has been proposed for the power consumption of memory cards of the MultiMediaCard™ type. Thus, in electronic devices supporting this standard, the provision is made to supply a defined maximum power to the peripheral device. Moreover, the power consumption of memory cards of the MultiMediaCard™ type should thus not exceed the defined maximum limit. Such an arrangement is difficult, for example, for the reason that the power consumption of new memory cards to be developed is limited to this maximum value, wherein it may be an impediment for the implementation of such memory cards whose power consumption cannot be made smaller than the selected maximum limit. If the maximum limit is set so high that the power consumption of other memory cards to be developed later on is also very likely to be smaller than this, it will mean that relatively efficient and large regulators must be used in electronic devices, perhaps unnecessarily.--

The paragraph beginning at page 5, line 29 has been amended as follows:

--Fig. 1 shows the system according to a preferred embodiment of the invention in a ~~reduced block chart~~ simplified block diagram,--

The paragraph beginning at page 5, line 32 has been amended as follows:

--Fig. 2 shows a system according to a second preferred embodiment of the invention in a ~~reduced manner~~ simplified block diagram,--

The paragraph beginning at page 5, line 35 has been amended as follows:

--Fig. 3 shows signalling in the method according to a preferred embodiment of the invention in a ~~reduced~~ simplified manner, and--

The paragraph beginning at page 6, line 1 has been amended as follows:

--Fig. 4 shows a peripheral device according to yet another preferred embodiment of the invention in a ~~reduced block chart~~ simplified block diagram.--

The paragraph beginning at page 6, line 7 has been amended as follows:

--In the system according to an advantageous embodiment of the invention, shown in Fig. 1, the electronic device 1 is exemplified by a wireless communication device. In this example, the peripheral device 2 is a memory card, such as a memory card complying with the MultiMediaCard™ standard. However, it will be ~~obvious~~ evident that the present invention is not limited solely to such electronic devices and peripheral devices, but the invention can also be applied in connection with other electronic devices and peripheral devices. The peripheral device 2 can be, for example, an interface card or also another device. The electronic device 1 contains a control block 3 comprising one or more processors, such as a micro controller unit (MCU). Furthermore, the electronic device 1 comprises a memory 4, a user interface 5 and means 6 for performing mobile station functions, such as GSM and/or UMTS mobile communication means. The user interface 5 preferably comprises a display, a keypad and audio means in a way known as such. For the connection of the peripheral device 2, the electronic device 1 is provided with connecting means 7 which

comprise at least one connector 8 as well as the necessary I/O blocks 9, for example to connect the buses of the peripheral device 2 and the electronic device 1 to each other.--

The paragraph beginning at page 6, line 28 and ending at page 7, line 4 has been amended as follows:
--The peripheral device is also provided with corresponding connecting means 10 for connecting the peripheral device 2 to the electronic device 1. The connecting means 10 of the peripheral device comprise at least one connector 11 which can be connected to the connector 8 of the electronic device 1, and an I/O block 12. The power supply to the peripheral device 2 is arranged from the electronic device 1 via the connectors 8, 11. The I/O blocks are used for communication between the electronic device 1 and the peripheral device 2. This can take place as parallel data transmission or serial data transmission. For example, said peripheral device according to the MultiMediaCard™ specifications applies serial data transmission. However, in view of the present invention, ~~it is not significant, in~~ which format is used for the data transmission between the electronic device 1 and the peripheral device 2 is ~~carried out~~ not significant.--

The paragraph beginning at page 7, line 20 and ending at page 8, line 12 has been amended as follows:
--The following is a description of the operation of the method according to a preferred embodiment of the invention in a system shown in Fig. 1. For example, information on whether a peripheral device 2 is placed in the connector 8 of the connecting means of the electronic device, is transmitted via the I/O blocks to the electronic device 1. This can be implemented, for example, by providing the I/O block 9, 12 with a detection line 15 whose state is changed when the peripheral device 2 is placed in the

connector 8. In this advantageous embodiment of the invention, the detection line 15 is implemented so that the detection line 15 is set in the logical 1 state by means of a pull-up resistance R in the electronic device 1. In the system of Fig. 1, the change of state is achieved in such a way that the peripheral device 2 ~~earths~~ grounds the detection line 15, wherein the state of the detection line 15 is changed to the logical 0 state. This change of state is detected in the electronic device 1, for example, in such a way that the change of state causes an interrupt in the control block 3, wherein a corresponding interrupt service program is run and the running of the initializing functions of the peripheral device are started. After the operating voltages have been coupled to the peripheral device, the processor 13 of the peripheral device 2 will start to run its own initializing operations. For example, the power consumption of the peripheral device 2 is set to a default value which, in this advantageous embodiment, is a power consumption value according to the first maximum limit. In this context, it is assumed that the first maximum limit is lower than the second maximum limit. The processor also sets the frequency of the clock generator 16 to correspond to this power consumption value. Typically, the frequency of the clock generator is set to a minimum value. In all peripheral devices 2, it is not necessarily possible to control the frequency of the clock generator 16, wherein the clock generator 16 cannot be used for controlling the power consumption.--

The paragraph beginning at page 8, line 14 and ending at page 9, line 3 has been amended as follows:

--In the operations of initializing the peripheral device, performed by the electronic device 1, the type of the peripheral device 2 is preferably examined, which may affect the type of

initialization operations to be performed. However, this description will only discuss the operations which are essential in view of the invention. The signalling to be performed in this method according to the advantageous embodiment of the invention is illustrated in a ~~reduced~~ simplified manner in the appended Fig. 3. The determination of the type of the peripheral device 2 will be followed by determining the first and second maximum limits for power consumption which have been stored on the device 2, such as a card. Thus, a maximum limit reading message is preferably transmitted from the electronic device 1 to the peripheral device 2. This is illustrated by ~~arrow~~ a signal on a line 301 in the chart of Fig. 3. The message is received in the peripheral device 2 and its content is preferably examined in ~~a~~ the processor 13. On the basis of the message, the processor 13 reads the first maximum limit and the second maximum limit from the memory 14 (block 302 in Fig. 3). If there are more than two maximum limits, the number of the maximum limits is preferably stored in the memory means, wherein the processor 13 reads the values of all the maximum limits from the memory 14. After this, the processor 13 generates a reply message (block 303) containing the requested information, such as the first and second maximum limits and, if necessary, also the number of the maximum limits. In the case of several maximum limits, also the values of the other maximum limits are preferably included in the message. The message is transmitted via the I/O blocks 9, 12 to the electronic device (~~arrow~~ as indicated by a signal on a line 304), in which the control block reads the information of the received message and, if necessary, stores ~~them~~ the information in the memory 4 of the electronic device.--

The paragraph beginning at page 9, line 5 has been amended as follows:

--After the maximum limits of power consumption supported by the peripheral device are known in the electronic device 1, it is possible to start to adjust the power consumption of the peripheral device, if necessary. Let us assume that the electronic device 1 is capable of supplying the power corresponding to the second maximum limit to the peripheral device 2. Thus, a power control message is transmitted from the electronic device 1 to the peripheral device 2 (~~arrow~~ as indicated by a signal on a line 305). This power control message indicates the power consumption value which is to be set as the maximum value for the peripheral device 2, for example said second maximum limit. The processor 13 of the peripheral device examines the type of the received message, and after determining that it is a power control message, reads the maximum value for power consumption indicated in the message (block 306). Next, the processor 13 of the peripheral device sets, for example the operating frequency of the clock generator 16 to a value corresponding to this maximum value for power consumption, for example to the highest possible frequency. In some embodiments, the bus widths within the processor can also be changed according to the maximum limit used for power consumption. Furthermore, the peripheral device 2 preferably informs the electronic device 1 that the power consumption has been limited to the requested value (~~arrow~~ as indicated by a signal on a line 307).--

The paragraph beginning at page 9, line 27 and ending at page 10, line 16 has been amended as follows:

--If the electronic device 1 cannot supply the peripheral device 2 with the power of the second maximum limit, or if, for another reason, the electronic device 1 tends to set the maximum value for power consumption lower than the second maximum limit, it is possible to perform signalling, by which the electronic

device 1 and the peripheral device try to find such a maximum limit for power consumption which is suitable in the situation. This can be carried out, for example, in such a way that the electronic device 1 selects, between the first and second maximum limits, a value which is a maximum value ~~in~~ from the point of view of the electronic device 1. Information about this limit is transferred to the peripheral device 2, in which the suggested value is examined in the processor 13, and if it is found acceptable, this information is transferred to the electronic device 1. If the peripheral device 2 cannot set its own power consumption to such a level which corresponds to the suggested maximum value, the peripheral device 2 will suggest a lower value between the first and second maximum values. If this value is possible ~~in~~ from the point of view of the electronic device 1, the electronic device 1 will transmit this information to the peripheral device 2, in which the power consumption is set to this value. If the value suggested by the peripheral device 2 is not suitable, the electronic device 1 advantageously selects another, preferably lower value which, however, is at least equal to the first maximum limit, and reports it to the peripheral device 2. The above-presented steps are iterated, until such a power consumption value is found which is suitable for both the electronic device 1 and the peripheral device 2. In some cases, it may occur that the only suitable value is the first maximum value, wherein the power consumption does not need to be adjusted, because this value is the default value.--

The paragraph beginning at page 10, line 18 has been amended as follows:

--There may also be a need to change the value of the power consumption during the operation of the electronic device 1 and the peripheral device 2 connected ~~to the same~~ together. For

example, if the peripheral device is a transceiver card, such as a mobile station card or a modem card, there may be a need to significantly change the power consumption limit of the peripheral device 2, for example, for the time of a transmission. Thus, at the stage when *e.g.* the peripheral device 2 detects a need to change the power consumption, it transmits a message to the electronic device 1 and proposes a new power consumption value which is, however, in the range between the first and second maximum values. An exchange of messages is performed between the electronic device 1 and the peripheral device 2 by applying the above-described principles, to control the power consumption of the peripheral device according to the need. When the need for power consumption is changed again, a new adjustment of the power consumption can be made.--

The paragraph beginning at page 12, line 7 has been amended as follows:

--Consequently, the power consumption of the peripheral device 2 can be adjusted *e.g.* by changing the clock frequency and/or the bus width, but it ~~is obvious~~ should be evident that other methods for adjusting ~~the~~ power consumption are also known and are applicable in connection with the invention. ~~The power~~ Power consumption can also be controlled by controlling the operating voltage, if the operating voltage of the peripheral device 2 does not need to be a given constant value. Peripheral devices are known, in which the operating voltage can be selected to be, for example, either 3 V, 3.3 V, or 5 V. Yet another example to be mentioned in this context of the possibilities to control the power consumption of the peripheral device is to control the current consumption of the peripheral device.--

The paragraph beginning at page 12, line 20 has been amended

as follows:
--Further, the power consumption of the peripheral device 2 can also be adjusted by changing the clock frequency of the bus of the connection between the peripheral device and the electronic device, if it is independently adjustable. The clock frequency of the bus can be changed *e.g.* by the electronic device 1 and/or by the peripheral device 2, if necessary. The electronic device 1 controls a clock generator(s) (not shown) which produces the timing signals for the bus according to the same principles ~~than what~~ as was presented above.--

The paragraph beginning at page 15, line 4 has been amended as follows:
--It will be ~~obvious~~ evident to those of skill in the art that the steps to be taken in the setting of the power consumption can also be implemented in another way than the above-presented hand-shake in the form of messages. For example, the connection means 7, 10 can be provided with connection lines which are used to set the power consumption of the peripheral device. Furthermore, the invention can be applied in such a way that certain alternative (allowable) values are defined for said maximum limits, wherein the first maximum limit and the second maximum limit for each peripheral device is selected from the set of these alternative limits.--

The paragraph beginning at page 15, line 32 has been amended as follows:
--It ~~is obvious~~ should be evident that the present invention is not limited solely to the above-presented embodiments but ~~it~~ can be modified within the scope of the appended claims.--

IN THE CLAIMS:

1. (Amended) A method for determining ~~the~~ power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device, ~~**wherein**~~ wherein the method comprising determining, for the power consumption, at least a first maximum value and a second maximum value which is higher than the first maximum value, and performing, between the electronic device and the peripheral device, setting of ~~the~~ a maximum for the power consumption of the peripheral device to a value which is between said first and second maximum values.

2. (Amended) The method according to claim 1, ~~**wherein**~~ wherein said first maximum ~~limit~~ value is used as a default value for the power consumption, wherein the power consumption of the peripheral device is set, at ~~the~~ a startup stage, to be substantially not higher than said first maximum limit.

3. (Amended) The method according to claim 1, ~~**wherein**~~ wherein said second maximum ~~limit~~ value is used as ~~the~~ a highest allowable ~~limit~~ value for the power consumption.

4. (Amended) The method according to claim 1, ~~**wherein**~~ wherein messages are transferred between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value substantially between said first maximum ~~limit~~ value and said second maximum ~~limit~~ value.

5. (Amended) The method according to claim 1, ~~**wherein**~~ wherein at least one content is stored in the peripheral device, ~~to be used~~ for use in connection with the electronic device, wherein at ~~the~~ a stage of storing the content, the power consumption set for

the peripheral device is a value corresponding to said second maximum ~~limit~~ value, and at ~~the~~ a stage of using the content, the power consumption set for the peripheral device is a value corresponding to said first maximum ~~limit~~ value.

6. (Amended) The method according to the claim 1, ~~wherein~~ wherein at least one clock signal is generated in the peripheral device and ~~that~~ wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

7. (Amended) The method according to the claim 1, ~~wherein~~ wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling ~~the~~ a width of said bus ~~width of the peripheral device~~.

8. (Amended) The method according to the claim 1, ~~wherein~~ wherein the peripheral device is provided with two or more storage blocks (2) ~~is~~ controlled by controlling ~~the~~ a number of storage ~~blocksprocessed~~ blocks processed by the peripheral device substantially simultaneously.

9. (Amended) A system comprising an electronic device with means for connecting a peripheral device and means for supplying power to the peripheral device, and which system comprises means for determining ~~the~~ power consumption, ~~wherein~~ wherein at least a first maximum value and a second maximum value which is higher than the first maximum value are defined for the power consumption, and ~~that~~ wherein the means for determining the power consumption comprise means for setting ~~the~~ a maximum ~~of the~~ power consumption of the peripheral device to a value which is between

said first maximum value and second maximum value.

10. (Amended) The system according to claim 9, comprising means for transferring messages between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value substantially between said first maximum ~~limit~~ value and said second maximum ~~limit~~ value.

11. (Amended) The system according to claim 9, ~~wherein~~ wherein the peripheral device comprises means for generating at least one clock signal, and ~~that~~ wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

12. (Amended) The system according to claim 9, ~~wherein~~ wherein the peripheral device comprises at least one bus, and ~~that~~ wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting the bus width of the peripheral device.

13. (Amended) The method according to the claim 9, ~~wherein~~ wherein the peripheral device is provided with two or more storage blocks, and ~~that~~ wherein the means for controlling the power consumption of the peripheral device comprise means for adjusting ~~the~~ a number of storage blocks processed by the peripheral device substantially simultaneously.

14. (Amended) The system according to the claim 9, ~~wherein~~ wherein the electronic device is a portable electronic device .

15. (Original) The system according to claim 14, comprising means for performing mobile station functions.

16. (Amended) An electronic device provided with means for connecting a peripheral device and means for supplying power to the peripheral device, and means for determining ~~the~~ power consumption, ~~**wherein**~~ wherein at least a first maximum value and a second maximum value which is higher than the first maximum value~~,~~ are defined for the power consumption, and ~~that~~ wherein the means for determining the power consumption comprise means for setting ~~the~~ a maximum ~~of the~~ power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value.

17. (Amended) The electronic device according to claim 16, comprising means for transmitting messages ~~from~~ to the peripheral device and for receiving messages from the peripheral device, to set ~~the~~ power consumption of the peripheral device to a value substantially between said first maximum limit and said second maximum limit.

18. (Amended) The electronic device according to claim 16, ~~**wherein**~~ wherein it is a portable electronic device.

19. (Original) The electronic device according to claim 18, comprising means for performing mobile station functions.

20. (Amended) A peripheral device provided with means for connecting the peripheral device to an electronic device~~, from which the~~ for supplying power ~~required for using the peripheral device is arranged to be supplied~~ to the peripheral device, ~~**wherein**~~ wherein at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for ~~the~~ power consumption, and ~~that~~ wherein the peripheral device comprises means for setting ~~the~~ a maximum ~~of~~

~~the~~ power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value.

21. (Amended) The peripheral device according to claim 20, ~~**wherein**~~ wherein at least one content is stored in the peripheral device ~~to be used~~ for use in connection with the electronic device.

22. (Amended) The peripheral device according to claim 20, comprising means for generating at least one clock signal and means for controlling the power consumption of the peripheral device by ~~controlling the frequency~~ frequency control of said at least one clock signal.

23. (Amended) The peripheral device according to claim 20, comprising at least one bus and means for controlling the power consumption of the peripheral device by controlling ~~the~~ a bus width of said bus of the peripheral device.

24. (Amended) The peripheral device according to the claim 20, ~~**wherein**~~ wherein the peripheral device is provided with two or more storage blocks, and that the means for controlling the power consumption of the peripheral device comprise means for controlling ~~the~~ a number of storage blocks processed by the peripheral device substantially simultaneously.

25. (Amended) The peripheral device according to the claim 20, ~~**wherein**~~ wherein said first maximum value and said second maximum value are stored in the peripheral device.

26. (Amended) The peripheral device according to the claim 20, ~~**wherein it**~~ wherein said peripheral device is a MultiMediaCard™ peripheral device.

IN THE ABSTRACT:

--Abstract of the Disclosure

The present invention relates to a method and a system for determining the power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device. At least a first maximum value and a second maximum value, higher than the first maximum value, are determined for the power consumption. ~~Between~~ Signaling between the electronic device and the peripheral device~~,~~ sets a maximum value for the power consumption of the peripheral device ~~is set to a value~~ which is between said first and second maximum values. The invention also relates to an electronic device and a peripheral device, in which the method is applied.

~~Fig. 1~~--

915-005.48

REMARKS

This preliminary amendment is submitted for the purpose of placing the application into standard U.S. format and to correct certain informalities in the text. Approval and allowance are respectfully requested.

Respectfully submitted,

Francis J. Maguire
Attorney for the Applicant
Registration No. 31,391

/mo
March 25, 2003
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(203) 261-1234

A method and a system for determining the power consumption in connection with an electronic device, and an electronic device

Cross-Reference to Related Applications

This application claims priority under 35 USC §119 to Finnish Patent Application No. 20020594 filed on March 27, 2002.

Field of the Invention

The present invention relates to a method for determining the power consumption in an electronic device, to which a peripheral device is connected, which is supplied with power from the electronic device. The invention also relates to a system which comprises an electronic device provided with means for connecting a peripheral device and means for supplying power to the peripheral device, and which system comprises means for determining the power consumption. Furthermore, the invention relates to an electronic device provided with means for connecting a peripheral device, means for supplying power to the peripheral device, and means for determining the power consumption of the peripheral device. Moreover, the invention relates to a peripheral device provided with means for connecting the peripheral device to an electronic device, from which the power needed for using the peripheral device is arranged to be supplied to the peripheral device.

Background of the Invention

At present, several such electronic devices are in use, to which it is possible to connect various peripheral devices, *e.g.* to expand the properties of the electronic device and to produce auxiliary functions. For example, it is possible to connect peripheral devices, such as connection cards (*e.g.* PCMCIA cards), to laptop computers to connect the laptop computer to a local area network, a landline or wireless telephone network, *etc.* Furthermore, peripheral devices can be used to expand the memory of the laptop computer, to connect an external fixed disk, a CDROM station, or the like.

The MultiMediaCard™ Association is, among other things, developing a standard for memory expansion boards (MultiMediaCard™; MultiMediaCard™ is a trademark of Infineon Technologies AG). These memory expansion boards can be used in various portable electronic devices, such as wireless communication devices and communicator type devices, to expand the memory capacity.

Because the peripheral devices can be connected to a variety of devices, the power consumption of the peripheral device should not exceed the maximum power that can be supplied from the electronic device to the peripheral device. Otherwise, the operation of the peripheral device and/or the electronic device may be disturbed and the electronic device may even be overheated. On the other hand, the power consumption requirements of different peripheral devices may be very different, wherein manufacturers of electronic devices should provide for the maximum power consumption in the power supply of the peripheral device connection. Solutions are known, such as Nokia Communicator 9110/9210, in which the power supply of the peripheral device connection of the electronic device is provided with a relatively efficient regulator, for example in the order of 150 mA/3 V. Such an efficient regulator is a relatively bulky component, which may cause placement problems, particularly in portable electronic devices. The provision for the maximum power consumption will be unnecessary in such electronic devices, whose users do not use, in connection with the electronic device, such a peripheral device whose power consumption is close to the maximum power consumption of the peripheral device designed for the electronic device. On the other hand, another user of a similar electronic device may use such a peripheral device whose power consumption is in the order of the maximum power consumption of the peripheral device designed for the electronic device.

In some electronic devices and peripheral devices to be connected to them, the operating voltage is selected at the stage when the peripheral device is turned on, *e.g.* when the electronic device is turned on or when the peripheral device is connected. Thus, signalling will be performed between the electronic device and the peripheral device, for the

electronic device to determine the level of the operating voltage required by the peripheral device and to select an operating voltage suitable for the peripheral device to the operating voltage line(s) of the peripheral device.

In said MultiMediaCard Association, a maximum limit has been proposed for the power consumption of memory cards of the MultiMediaCard™ type. Thus, in electronic devices supporting this standard, the provision is made to supply a defined maximum power to the peripheral device. Moreover, the power consumption of memory cards of the MultiMediaCard™ type should thus not exceed the defined maximum limit. Such an arrangement is difficult, for example, for the reason that the power consumption of new memory cards to be developed is limited to this maximum value, wherein it may be an impediment for the implementation of such memory cards whose power consumption cannot be made smaller than the selected maximum limit. If the maximum limit is set so high that the power consumption of other memory cards to be developed later on is also very likely to be smaller than this, it will mean that relatively efficient and large regulators must be used in electronic devices.

The power consumption of the peripheral device is normally proportional to the clock frequency used in the peripheral device, wherein an increase in the clock frequency will increase the power consumption. In a corresponding manner, to decrease the power consumption, the clock frequency of the peripheral device can be decreased, if this is possible in view of the other functions of the peripheral device. However, the operating rate of the peripheral device will thus decrease, which is not necessarily desirable. Also, the bus width used in the peripheral device has an effect on how much power is consumed in the peripheral device.

Summary of the Invention

It is an aim of the present invention to provide an improved method and system for determining the power consumption to be suitable in each situation. It is another aim of the invention to provide an electronic

device and a peripheral device for applying the method. The invention is based on the idea of determining at least a first and a second maximum value for the power consumption, wherein the electronic device and the peripheral device set the power consumption to a value between these first and second maximum values. Thus, in different operating situations, for example the peripheral device can adjust its power consumption to be suitable for the situation. The method according to the present invention is primarily characterized in determining, for the power consumption, at least a first maximum value and a second maximum value which is higher than the first maximum value, and setting, between the electronic device and the peripheral device, the maximum for the power consumption of the peripheral device to a value which is substantially between said first and second maximum values. The system according to the invention is primarily characterized in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum for the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value. The electronic device according to the invention is primarily characterized in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum for the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value. Furthermore, the peripheral device according to the invention is primarily characterized in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum for the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value.

The present invention shows remarkable advantages over solutions of prior art. By the method according to the invention, it is possible to

avoid the use of an unnecessarily large regulator in an electronic device, which saves costs, and wherein the size of the electronic device can, in some cases, be reduced and, on the other hand, problems of heating caused by high power consumption can be avoided. Also the power consumption can be reduced, which is advantageous particularly in portable devices. By means of the invention, the peripheral device connection can also be provided with flexibility, because the power consumption of the peripheral device can be adjusted and set to a value suitable for each situation of use. Also, the clock frequency and bus width of the peripheral device can be changed in the system according to an advantageous embodiment of the invention. Furthermore, the invention makes it possible that new peripheral devices to be developed will function in connection with electronic devices made earlier, and existing peripheral devices will function in connection with new electronic devices to be developed. With the solution according to the invention, it is also possible to achieve an improvement in the user-friendliness of the electronic device, for example, in a situation in which the peripheral device cannot fully operate on a lower level of power consumption but it can, however, inform the electronic device about this. Thus, the electronic device can take care of the shutdown (turning off) of the peripheral device in the appropriate way and notify the user of this.

Brief Description of the Drawings

In the following, the invention will be described in more detail with reference to the appended drawings, in which

Fig. 1 shows the system according to a preferred embodiment of the invention in a reduced block chart,

Fig. 2 shows a system according to a second preferred embodiment of the invention in a reduced manner,

Fig. 3 shows signalling in the method according to a preferred embodiment of the invention in a reduced manner, and

Fig. 4 shows a peripheral device according to yet another preferred embodiment of the invention in a reduced block chart.

Detailed Description of the Invention

In the system according to an advantageous embodiment of the invention, shown in Fig. 1, the electronic device 1 is exemplified by a wireless communication device. In this example, the peripheral device 2 is a memory card, such as a memory card complying with the MultiMediaCard™ standard. However, it will be obvious that the present invention is not limited solely to such electronic devices and peripheral devices, but the invention can also be applied in connection with other electronic devices and peripheral devices. The peripheral device 2 can be, for example, an interface card or also another device. The electronic device 1 contains a control block 3 comprising one or more processors, such as a micro controller unit (MCU). Furthermore, the electronic device 1 comprises a memory 4, a user interface 5 and means 6 for performing mobile station functions, such as GSM and/or UMTS mobile communication means. The user interface 5 preferably comprises a display, a keypad and audio means in a way known as such. For the connection of the peripheral device 2, the electronic device 1 is provided with connecting means 7 which comprise at least one connector 8 as well as the necessary I/O blocks 9, for example to connect the buses of the peripheral device 2 and the electronic device 1 to each other.

The peripheral device is also provided with corresponding connecting means 10 for connecting the peripheral device 2 to the electronic device 1. The connecting means 10 of the peripheral device comprise at least one connector 11 which can be connected to the connector 8 of the electronic device 1, and an I/O block 12. The power supply to the peripheral device 2 is arranged from the electronic device 1 via the connectors 8, 11. The I/O blocks are used for communication between the electronic device 1 and the peripheral device 2. This can take place as parallel data transmission or serial data transmission. For example, said peripheral device according to the MultiMediaCard™ specifica-

tions applies serial data transmission. However, in view of the present invention, it is not significant, in which format the data transmission between the electronic device 1 and the peripheral device 2 is carried out.

The peripheral device 2 also comprises a processor 13 or the like for controlling the functions of the peripheral device 2. Furthermore, the peripheral device comprises a memory 14, such as a read/write memory (RAM), *e.g.* for the storage of data, as well as a read-only memory (ROM, NVRAM) for the storage of the program code. The processor is responsible, for example, for controlling the I/O blocks in the data transmission between the peripheral device 2 and the electronic device 1. At least a first maximum value and a second maximum value for power consumption, which are used in the method according to the present invention, are also stored in the memory 14 of the peripheral device. Furthermore, the peripheral device comprises means for generating one or more clock signals required for the operation of the processor, such as a clock generator 16.

The following is a description of the operation of the method according to a preferred embodiment of the invention in a system shown in Fig. 1. For example, information on whether a peripheral device 2 is placed in the connector 8 of the connecting means of the electronic device, is transmitted via the I/O blocks to the electronic device 1. This can be implemented, for example, by providing the I/O block 9, 12 with a detection line 15 whose state is changed when the peripheral device 2 is placed in the connector 8. In this advantageous embodiment of the invention, the detection line 15 is implemented so that the detection line 15 is set in the logical 1 state by means of a pull-up resistance R in the electronic device 1. In the system of Fig. 1, the change of state is achieved in such a way that the peripheral device 2 earths the detection line 15, wherein the state of the detection line 15 is changed to the logical 0 state. This change of state is detected in the electronic device 1, for example, in such a way that the change of state causes an interrupt in the control block 3, wherein a corresponding interrupt service program is run and the running of the initializing functions of the peripheral device are started. After the operating voltages have been

coupled to the peripheral device, the processor 13 of the peripheral device 2 will start to run its own initializing operations. For example, the power consumption of the peripheral device 2 is set to a default value which, in this advantageous embodiment, is a power consumption value according to the first maximum limit. In this context, it is assumed that the first maximum limit is lower than the second maximum limit. The processor also sets the frequency of the clock generator 16 to correspond to this power consumption value. Typically, the frequency of the clock generator is set to a minimum value. In all peripheral devices 2, it is not necessarily possible to control the frequency of the clock generator 16, wherein the clock generator 16 cannot be used for controlling the power consumption.

In the operations of initializing the peripheral device, performed by the electronic device 1, the type of the peripheral device 2 is preferably examined, which may affect the type of initialization operations to be performed. However, this description will only discuss the operations which are essential in view of the invention. The signalling to be performed in this method according to the advantageous embodiment of the invention is illustrated in a reduced manner in the appended Fig. 3. The determination of the type of the peripheral device 2 will be followed by determining the first and second maximum limits for power consumption which have been stored on the card. Thus, a maximum limit reading message is preferably transmitted from the electronic device 1 to the peripheral device 2. This is illustrated by arrow 301 in the chart of Fig. 3. The message is received in the peripheral device 2 and its content is preferably examined in a processor 13. On the basis of the message, the processor 13 reads the first maximum limit and the second maximum limit from the memory 14 (block 302 in Fig. 3). If there are more than two maximum limits, the number of the maximum limits is preferably stored in the memory means, wherein the processor 13 reads the values of all the maximum limits from the memory 14. After this, the processor 13 generates a reply message (block 303) containing the requested information, such as the first and second maximum limits and, if necessary, also the number of the maximum limits. In the case of several maximum limits, also the values of the other maximum limits are preferably included in the message. The message is trans-

mitted via the I/O blocks 9, 12 to the electronic device (arrow 304), in which the control block reads the information of the received message and, if necessary, stores them in the memory 4 of the electronic device.

After the maximum limits of power consumption supported by the peripheral device are known in the electronic device 1, it is possible to start to adjust the power consumption of the peripheral device, if necessary. Let us assume that the electronic device 1 is capable of supplying the power corresponding to the second maximum limit to the peripheral device 2. Thus, a power control message is transmitted from the electronic device 1 to the peripheral device 2 (arrow 305). This power control message indicates the power consumption value which is to be set as the maximum value for the peripheral device 2, for example said second maximum limit. The processor 13 of the peripheral device examines the type of the received message, and after determining that it is a power control message, reads the maximum value for power consumption indicated in the message (block 306). Next, the processor 13 of the peripheral device sets, for example the operating frequency of the clock generator 16 to a value corresponding to this maximum value for power consumption, for example to the highest possible frequency. In some embodiments, the bus widths within the processor can also be changed according to the maximum limit used for power consumption. Furthermore, the peripheral device 2 preferably informs the electronic device 1 that the power consumption has been limited to the requested value (arrow 307).

If the electronic device 1 cannot supply the peripheral device 2 with the power of the second maximum limit, or if, for another reason, the electronic device 1 tends to set the maximum value for power consumption lower than the second maximum limit, it is possible to perform signalling, by which the electronic device 1 and the peripheral device try to find such a maximum limit for power consumption which is suitable in the situation. This can be carried out, for example, in such a way that the electronic device 1 selects, between the first and second maximum limits, a value which is a maximum value in view of the electronic device 1. Information about this limit is transferred to the peripheral device 2, in which the suggested value is examined 13, and if it is

found acceptable, this information is transferred to the electronic device 1. If the peripheral device 2 cannot set its own power consumption to such a level which corresponds to the suggested maximum value, the peripheral device 2 will suggest a lower value between the first and second maximum values. If this value is possible in view of the electronic device 1, the electronic device 1 will transmit this information to the peripheral device 2, in which the power consumption is set to this value. If the value suggested by the peripheral device 2 is not suitable, the electronic device 1 advantageously selects another, preferably lower value which, however, is at least equal to the first maximum limit, and reports it to the peripheral device 2. The above-presented steps are iterated, until such a power consumption value is found which is suitable for both the electronic device 1 and the peripheral device 2. In some cases, it may occur that the only suitable value is the first maximum value, wherein the power consumption does not need to be adjusted, because this value is the default value.

There may also be a need to change the value of the power consumption during the operation of the electronic device 1 and the peripheral device 2 connected to the same. For example, if the peripheral device is a transceiver card, such as a mobile station card or a modem card, there may be a need to significantly change the power consumption limit of the peripheral device 2, for example, for the time of a transmission. Thus, at the stage when *e.g.* the peripheral device 2 detects a need to change the power consumption, it transmits a message to the electronic device 1 and proposes a new power consumption value which is, however, in the range between the first and second maximum values. An exchange of messages is performed between the electronic device 1 and the peripheral device 2 by applying the above-described principles, to control the power consumption of the peripheral device according to the need. When the need for power consumption is changed again, a new adjustment of the power consumption can be made.

The need to change the power consumption of the peripheral device may also develop in the electronic device 1. For example, when the operation of the electronic device 1 shifts to a power saving mode, or

when the charge of a battery (not shown) in the electronic device is reduced, the electronic device 1 may control the peripheral device 2 to shift to a less power consuming state.

The peripheral device according to the invention can also be connected to such an electronic device 1 which does not have a possibility to adjust the power consumption. Thus, the peripheral device 2 sets a default value, *i.e.* preferably the first maximum limit, as the power consumption value. Consequently, the peripheral device according to the invention can also be connected to such an electronic device 1 in which the steps of the method according to the invention are not carried out to control the power consumption of the peripheral device 2.

Above, the use of more than two different maximum limits were mentioned as the maximum values for power consumption. In this context, it is assumed that the other maximum limits are between the first and second maximum limits. These different maximum limits are feasible, for example, in such applications, in which different bus widths can be selected in the peripheral device. For example, in the system of Fig. 2, the bus width of the connection between the peripheral device and the electronic device can be selected to be any of the three values: 8, 16 or 32 bits. At the same time, this bus width selected for the connection is, in this advantageous embodiment, also used in the internal bus 17 of the peripheral device 2. Typically, the power consumption is the higher, the wider the bus used. Thus, the presumption is preferably that the bus width at the start-up stage is 8 bits, but the electronic device 1 and the peripheral device 2 may negotiate on the use of another bus width, *i.e.* on the change of the maximum limit for power consumption. This can be implemented by applying the principles described above. However, it will be obvious that said bus widths are only some non-restricting examples of bus widths.

The frequency of the clock generator 16 of the peripheral device is not necessarily adjustable in a stepless manner, but it is possible to select a value for the frequency from some predetermined values. Thus, the maximum limits for power consumption corresponding to these different frequencies can be stored as said maximum limits in the peripheral

device, or if only the first maximum limit (lowest power consumption) and the second maximum limit (highest power consumption) are stored, it is possible to perform the exchange of messages between the electronic device 1 and the peripheral device, as described above in this description, to adjust the suitable power consumption limit.

Consequently, the power consumption of the peripheral device 2 can be adjusted *e.g.* by changing the clock frequency and/or the bus width, but it is obvious that other methods for adjusting the power consumption are also known and are applicable in connection with the invention. The power consumption can also be controlled by controlling the operating voltage, if the operating voltage of the peripheral device 2 does not need to be a given constant value. Peripheral devices are known, in which the operating voltage can be selected to be, for example, either 3 V, 3.3 V, or 5 V. Yet another example to be mentioned in this context of the possibilities to control the power consumption of the peripheral device is to control the current consumption of the peripheral device.

Further, the power consumption of the peripheral device 2 can also be adjusted by changing the clock frequency of the bus of the connection between the peripheral device and the electronic device, if it is independently adjustable. The clock frequency of the bus can be changed *e.g.* by the electronic device 1 and/or by the peripheral device 2, if necessary. The electronic device 1 controls a clock generator(s) (not shown) which produces the timing signals for the bus according to the same principles than what was presented above.

In an advantageous embodiment of the invention, at least a part of the memory of the peripheral device 2 is divided into two or more memory blocks, to form so-called storage banks. Thus, in the peripheral device, one or more of these memory blocks can be selected for use, *e.g.* on the basis of the maximum power consumption value defined for the peripheral device 2. With higher power consumption values, it is typically possible to take more memory blocks into use than with lower power consumption values. Figure 4 shows an example of the structure of such a peripheral device. In the peripheral device 2 shown in Fig. 4,

the memory 14 is provided with four memory blocks 14a, 14b, 14c, 14d, but it will be obvious that in practical applications, the number of storage banks can, within the scope of the invention, also be other than four. To take the memory blocks 14a–14d into use and to remove them from service, connection lines 18a–18d are preferably provided from the processor 13, to couple *e.g.* the operating voltage to the desired memory blocks 14a–14d, or the coupling lines are used to switch each memory block 14a–14d either to an active mode or to a power-saving mode. Also the above-presented method can be used to control the power consumption of the peripheral device 2 instead of or in addition to the methods for controlling the power consumption as presented above in this description.

In the electronic device 1, the power control can be performed, for example, by providing the electronic device 1 with a power source whose output voltage can be changed. Thus, in the electronic device 1, the operating voltage to be supplied to the peripheral device is selected to be the voltage value corresponding to the power consumption at the time.

The method according to the invention can also be applied in the implementation of various contents for use in connection with electronic devices 1, for example in the following way. As the peripheral device 2, it is possible to use a memory card, such as a card complying with the definitions of the MultiMediaCard™ standard, in which contents can be stored. In this context, contents refer to data files, application programs, electronic books, audiovisual information, such as music, videos, *etc.* For example, a content provider stores such contents on the memory card. Thus, the memory card 2 is connected to an electronic device provided with means for transferring the content to the memory card 2. Thus, before starting the storage, the electronic device and the memory card 2 set the power consumption of the memory card preferably to a value corresponding to the second maximum limit. This is possible, because in such an electronic device 1 used for storing contents, the power consumption of the memory card has hardly any significance, but the electronic device 1 can supply the memory card 2 with the sufficient power. The storage can thus be performed at a

maximum rate, because the clock frequency and/or bus width of the memory card can be set to the maximum. Also, the checkup of the content stored on the memory card 2, to detect possible storage defects, can be performed at a maximum rate. Thanks to the maximum storage and/or checkup rate, the content production rate of the electronic device 1 can be increased when compared with methods of prior art.

In a corresponding manner, at the stage when the content stored on the memory card 2 is to be used in an electronic device 1, the power consumption of the memory card 2 can be set to a level which is suitable for the electronic device 1, for example to the lowest possible power consumption. Thus, when applying the method of the invention, the content production rate does not need to be limited according to the maximum power consumption value possible in the use of the content.

Because the method according to the invention can be used for the power control of the peripheral device, the peripheral device 2 can be connected to a variety of electronic devices. In some electronic devices, it is only possible to supply the peripheral device with the power (voltage and current) corresponding to the minimum power consumption, wherein the electronic device 1 does not need a large regulator, and the size of the electronic device does not need to be increased because of the need of space for a large regulator. On the other hand, power consumption does not need to be restricted in peripheral devices 2 to be developed, because the suitable power consumption value can be negotiated by the electronic device and the peripheral device. Thus, if the peripheral device is connected to such an electronic device, in which a relatively high power can be supplied to the peripheral device connection, the peripheral device can be used as efficiently as possible (with a high clock frequency / large bus width). At the stage of initialization, even such a peripheral device will operate with a lower power consumption, until a suitable power consumption value has been selected. In the system according to the invention, it is possible to provide for the use of peripheral devices which will be developed in the future and may require even high power in electronic

devices. However, it is not necessary to consider cards with a high power consumption in the design of all electronic devices.

It will be obvious that the steps to be taken in the setting of the power consumption can also be implemented in another way than the above-presented handshake in the form of messages. For example, the connection means 7, 10 can be provided with connection lines which are used to set the power consumption of the peripheral device. Furthermore, the invention can be applied in such a way that certain alternative (allowable) values are defined for said maximum limits, wherein the first maximum limit and the second maximum limit for each peripheral device is selected from the set of these alternative limits.

It should also be mentioned that the peripheral device 2 does not need to be a card-format peripheral device, but the peripheral device 2 used can also be another device which can be connected to the electronic device 1. One non-restrictive example to be mentioned of such a peripheral device is a camera which is connected, for example, to a wireless communication device, a computer, or the like. Thus, by controlling the power consumption, it is possible to affect the functional properties of the camera. For example, the rate of updating the images of the camera on the display of the electronic device may be lower with a lower power consumption than with a higher power consumption. Thus, the electronic device 1 may preferably set the power consumption of the camera used as the peripheral device 2 on the basis of how high a power can be supplied by the electronic device 1 to the peripheral device. In an advantageous embodiment of the invention, also the user of the electronic device 1 can set a maximum limit for the power consumption, wherein the user can, if necessary, *e.g.* reduce the maximum limit to prolong the time of operation of the electronic device.

It is obvious that the present invention is not limited solely to the above-presented embodiments but it can be modified within the scope of the appended claims.

Claims:

1. A method for determining the power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device, **wherein** the method comprising determining, for the power consumption, at least a first maximum value and a second maximum value which is higher than the first maximum value, and performing, between the electronic device and the peripheral device, setting of the maximum for the power consumption of the peripheral device to a value which is between said first and second maximum values.

2. The method according to claim 1, **wherein** said first maximum limit is used as a default value for the power consumption, wherein the power consumption of the peripheral device is set, at the startup stage, to be substantially not higher than said first maximum limit.

3. The method according to claim 1, **wherein** said second maximum limit is used as the highest allowable limit for the power consumption.

4. The method according to claim 1, **wherein** messages are transferred between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value substantially between said first maximum limit and said second maximum limit.

5. The method according to claim 1, **wherein** at least one content is stored in the peripheral device, to be used in connection with the electronic device, wherein at the stage of storing the content, the power consumption set for the peripheral device is a value corresponding to said second maximum limit, and at the stage of using the content, the power consumption set for the peripheral device is a value corresponding to said first maximum limit.

6. The method according to the claim 1, **wherein** at least one clock signal is generated in the peripheral device and that the power

consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

7. The method according to the claim 1, **wherein** the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling the bus width of the peripheral device.

8. The method according to the claim 1, **wherein** the peripheral device is provided with two or more storage blocks (2) is controlled by controlling the number of storage blocksprocessed by the peripheral device substantially simultaneously.

9. A system comprising an electronic device with means for connecting a peripheral device and means for supplying power to the peripheral device, and which system comprises means for determining the power consumption, **wherein** at least a first maximum value and a second maximum value which is higher than the first maximum value are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum of the power consumption of the peripheral device to a value which is between said first maximum value and second maximum value.

10. The system according to claim 9, comprising means for transferring messages between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value substantially between said first maximum limit and said second maximum limit.

11. The system according to claim 9, **wherein** the peripheral device comprises means for generating at least one clock signal, and that the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

12. The system according to claim 9, **wherein** the peripheral device comprises at least one bus, and that the system comprises means for

controlling the power consumption of the peripheral device by adjusting the bus width of the peripheral device.

13. The method according to the claim 9, **wherein** the peripheral device is provided with two or more storage blocks, and that the means for controlling the power consumption of the peripheral device comprise means for adjusting the number of storage blocks processed by the peripheral device substantially simultaneously.

14. The system according to the claim 9, **wherein** the electronic device is a portable electronic device .

15. The system according to claim 14, comprising means for performing mobile station functions.

16. An electronic device provided with means for connecting a peripheral device and means for supplying power to the peripheral device, and means for determining the power consumption, **wherein** at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum of the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value.

17. The electronic device according to claim 16, comprising means for transmitting messages from the peripheral device and for receiving messages from the peripheral device, to set the power consumption of the peripheral device to a value substantially between said first maximum limit and said second maximum limit.

18. The electronic device according to claim 16, **wherein** it is a portable electronic device.

19. The electronic device according to claim 18, comprising means for performing mobile station functions.

20. A peripheral device provided with means for connecting the peripheral device to an electronic device, from which the power required for using the peripheral device is arranged to be supplied to the peripheral device, **wherein** at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the peripheral device comprises means for setting the maximum of the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value.

21. The peripheral device according to claim 20, **wherein** at least one content is stored in the peripheral device to be used in connection with the electronic device.

22. The peripheral device according to claim 20, comprising means for generating at least one clock signal and means for controlling the power consumption of the peripheral device by controlling the frequency of said at least one clock signal.

23. The peripheral device according to claim 20, comprising at least one bus and means for controlling the power consumption of the peripheral device by controlling the bus width of the peripheral device.

24. The peripheral device according to the claim 20, **wherein** the peripheral device is provided with two or more storage blocks, and that the means for controlling the power consumption of the peripheral device comprise means for controlling the number of storage blocks processed by the peripheral device substantially simultaneously.

25. The peripheral device according to the claim 20, **wherein** said first maximum value and said second maximum value are stored in the peripheral device.

26. The peripheral device according to the claim 20, **wherein** it is a MultiMediaCard™ peripheral device.

Abstract

The present invention relates to a method and a system for determining the power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device. At least a first maximum value and a second maximum value, higher than the first maximum value, are determined for the power consumption. Between the electronic device and the peripheral device, a maximum for the power consumption of the peripheral device is set to a value which is between said first and second maximum values. The invention also relates to an electronic device and a peripheral device, in which the method is applied.

Fig. 1

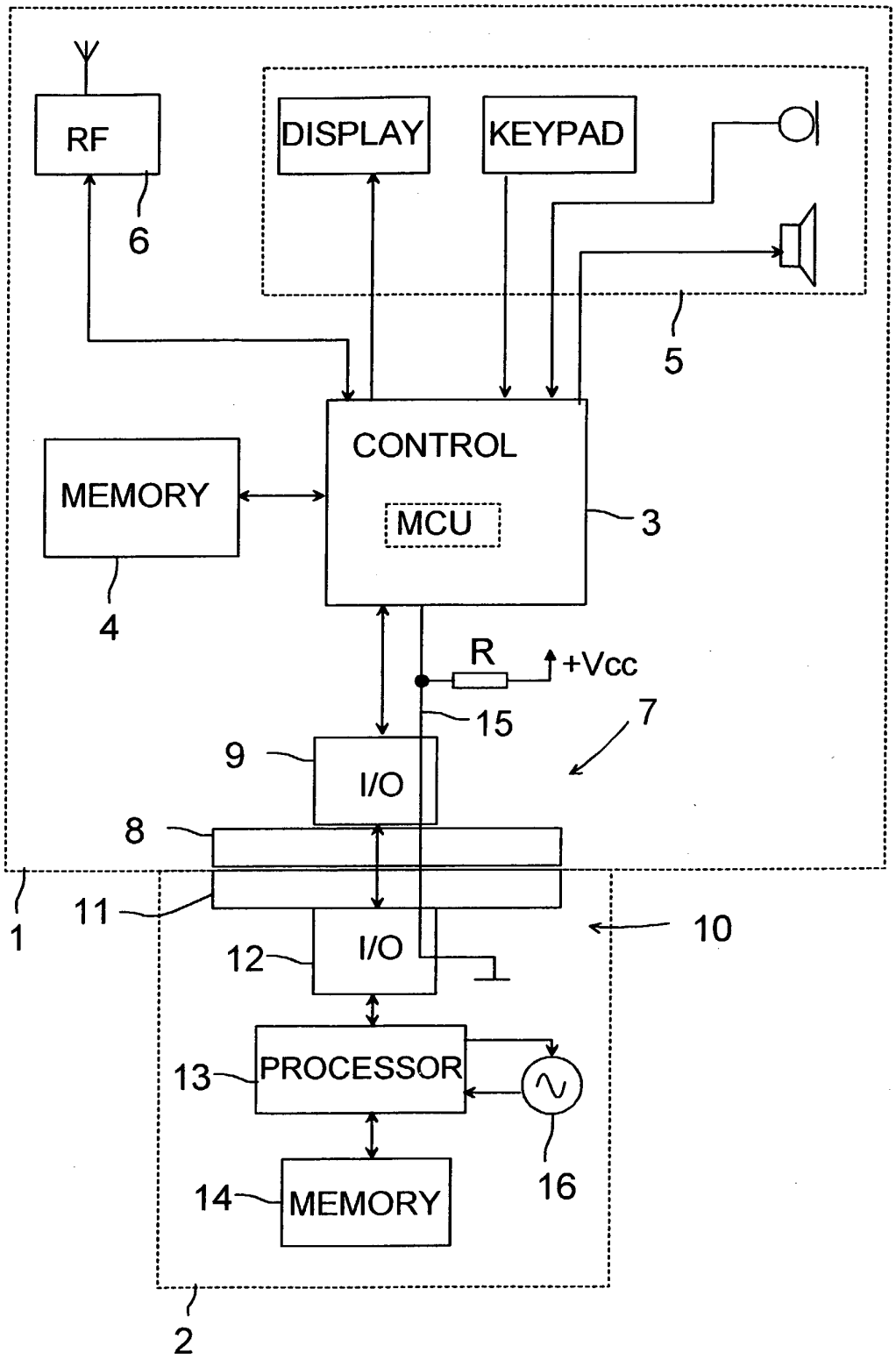
RF
6
DISPLAY
KEYPAD
5
CONTROL
MCU
3
MEMORY
4
R
+Vcc
15
7
9
I/O
8
1
11
10
12
I/O
13
PROCESSOR
16
14
MEMORY
2

Fig 1

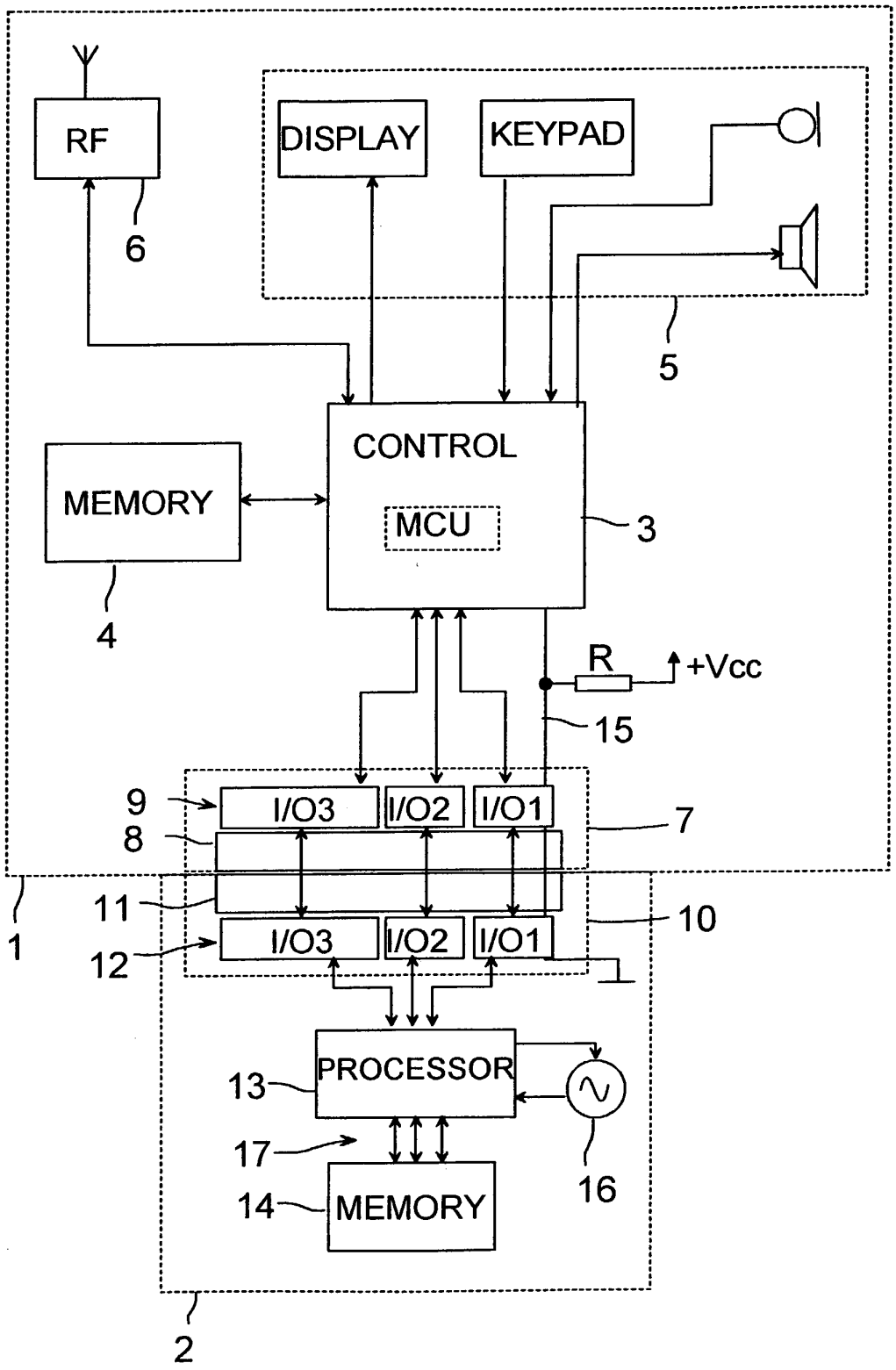
RF
6
DISPLAY
KEYPAD
5
CONTROL
MCU
3
MEMORY
4
R
+Vcc
15
9
8
I/O3
I/O2
I/O1
7
11
12
I/O3
I/O2
I/O1
10
1
PROCESSOR
13
17
14
MEMORY
16
2

Fig 2

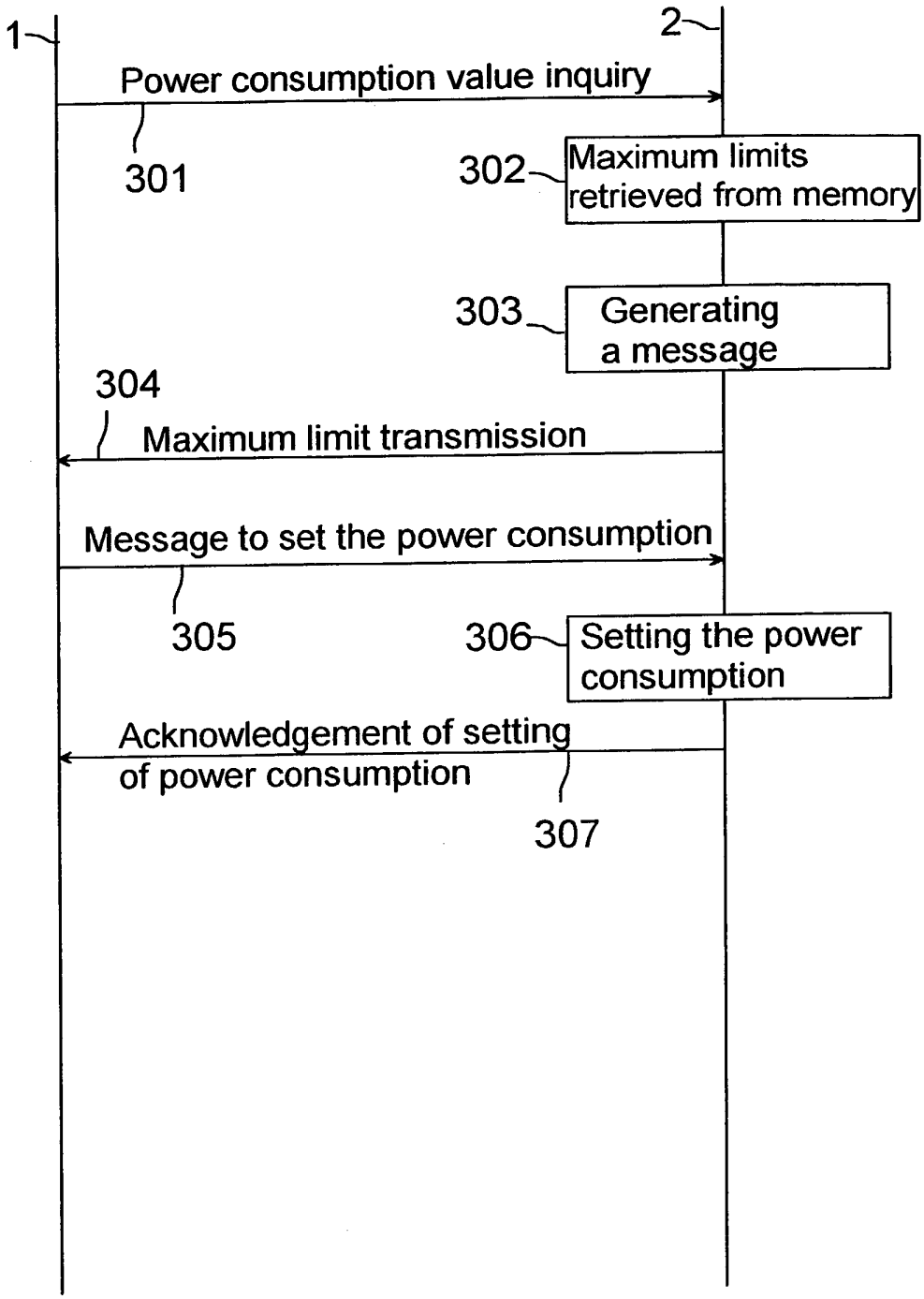
1
2
Power consumption value inquiry
301
302
Maximum limits retrieved from memory
303
Generating a message
304
Maximum limit transmission
Message to set the power consumption
305
306
Setting the power consumption
Acknowledgement of setting of power consumption
307

Fig 3

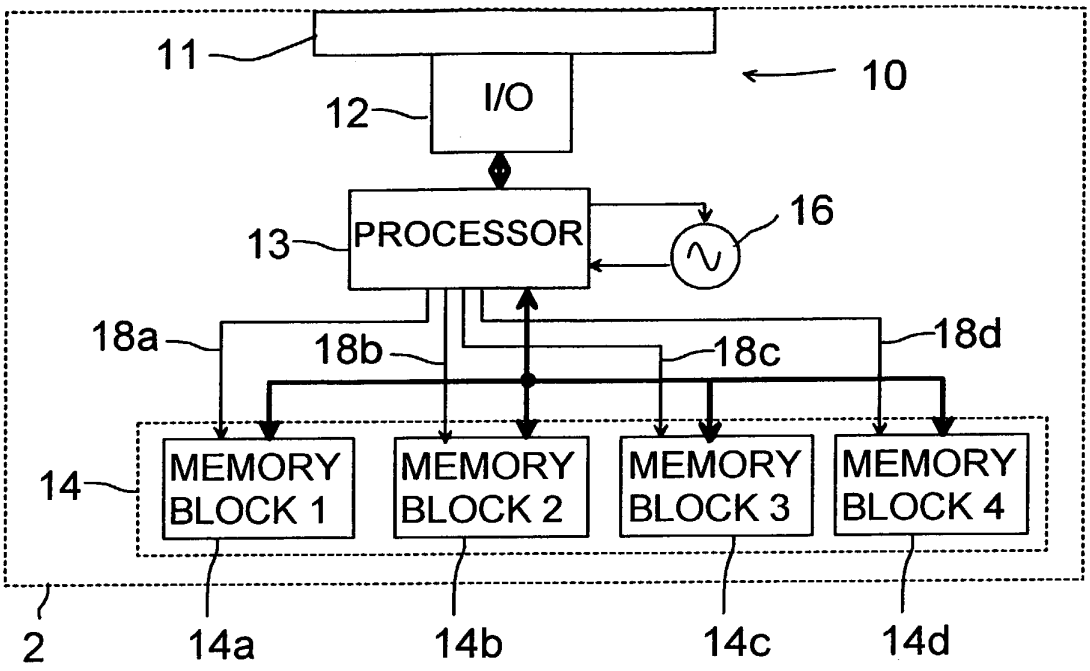
11
10
I/O
12
PROCESSOR
13
16
18a
18b
18c
18d
14
MEMORY BLOCK 1
MEMORY BLOCK 2
MEMORY BLOCK 3
MEMORY BLOCK 4
2
14a
14b
14c
14d

Fig 4

COMBINED DECLARATION AND POWER OF ATTORNEY

(Docket Number)

As a below named inventor, I hereby declare that:

- my residence, post office address and citizenship are as stated below next to my name;
- I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE;
- the specification of which is attached hereto unless the following box is checked: ☐. If the box is checked,

  the application was filed on ,
  as U.S. Application Number ,
  or PCT International Application Number ,
  and was amended on (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application			Priority Not Claimed
20020594 (Application Number)	Finland (Country)	27/03/2002 (Day/Month/Year Filed)	☐
(Application Number)	(Country)	(Day/Month/Year Filed)	☐

To the extent permitted by rule or law, I hereby incorporate by reference the Prior Foreign Application(s) listed above.

I hereby claim the benefits under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

(Provisional Application Number)	(Day/Month/Year Filed)
(Provisional Application Number)	(Day/Month/Year Filed)

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose information which is material to patentability, as defined in 37 CFR §1.56, which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application Number)	(Day/Month/Year Filed)	(Status--patented, pending, abandoned)
(Application Number)	(Day/Month/Year Filed)	(Status--patented, pending, abandoned)

The undersigned hereby authorizes the U.S. firm of **Ware, Fressola, Van Der Sluys & Adolphson LLP** to accept and follow instructions from the Finnish firm of **Tampereen Patenttitoimisto Oy** as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. firm and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. firm will be so notified by the undersigned or his successors and assigns. I hereby appoint the attorney(s) and/or agent(s) assigned to the customer number listed below, as may from time to time be amended, belonging to the firm of **Ware, Fressola, Van Der Sluys & Adolphson LLP**, to prosecute this application and to transact all business in the USPTO:

Customer Number

4955

* 04955 *
04955
PATENT TRADEMARK OFFICE

Address all telephone calls to: Ware, Fressola, Van Der Sluys & Adolphson LLP at (203) 261-1234. **Address all correspondence to:**

Customer Number

4955

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PATENT TRADEMARK OFFICE

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Kimmo MYLLY Full name of sole or first inventor (given name, middle initial, FAMILY NAME(S) IN UPPER CASE)	
K. Myl Inventor's Signature	16.1.2003 Date
Tampere, Finland Residence	Finland Citizenship
Post Office Address: Niemenkuja 8 As 1, FIN-39160 JULKUJÄRVI, Finland.	

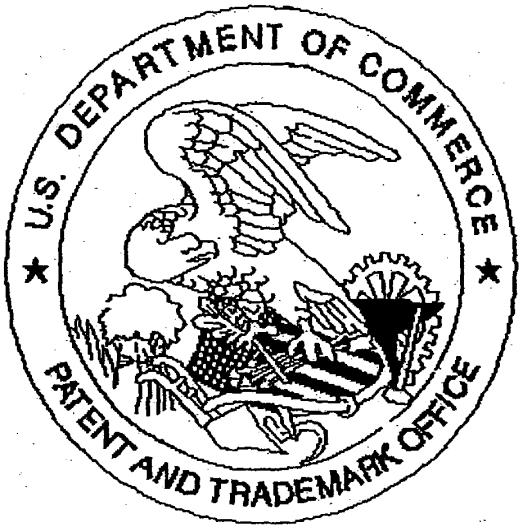
Full name of second inventor (given name, middle initial, FAMILY NAME(S) IN UPPER CASE)	
Inventor's Signature	Date
Residence	Citizenship
Post Office Address:	

Full name of third inventor (given name, middle initial, FAMILY NAME(S) IN UPPER CASE)	
Inventor's Signature	Date
Residence	Citizenship
Post Office Address:	

☐ Additional inventors are being named on separately numbered sheets attached hereto.

United States Patent & Trademark Office

Office of Initial Patent Examination -- Scanning Division



Application deficiencies found during scanning:

☑ Page(s) 15/15 of Transmittal were not present for scanning. (Document title)

☐ Page(s)_____ of _____ were not present for scanning. (Document title)

☐ ***Scanned copy is best available.***

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 915-005.48

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	26	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	26 minus 20=	* 6
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	108
X42=		OR	X84=	84
+140=		OR	+280=	0
TOTAL		OR	TOTAL	942

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

04/02/2003 STEJMEL1 00000052 10401338

02 FC:1001		750.00 OP
03 FC:1202		108.00 OP
04 FC:1201	34.00 CH	50.00 OP

PTO-1556
(5/87)

Kingston Exhibit 1004 - 61

*U.S. Government Printing Office: 2002 — 489-267/69033

CLAIMS ONLY

SERIAL NO. 10/401,338

FILING DATE 3-26-03

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	/					
2		/				
3		/				
4		/				
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TOTAL DEP.						
TOTAL CLAIMS						

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100						
TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

* MAY BE USED FOR ADDITIONAL CLAIMS OR AMENDMENTS

FORM PTO-2022 (1-98)

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

#3

Practitioner's Docket No. 915-005.48

PATENT 4-19-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kimmo Mylly
Serial No.: Group No.:
Filed: Herewith Examiner:
For: A METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE

Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF CERTIFIED COPY

Attached please find the certified copy of the foreign application from which priority is claimed for this case, along with the certified translation of Tuulikki Tulivirta, Certified Translator:

Country:	Finland
Application Number:	20020594
Filing Date:	March 27, 2002

WARNING: **"When a document that is required by statute to be certified must be filed, a copy, including a photocopy or facsimile transmission of the certification is not acceptable." 37 C.F.R. 1.4(f) (emphasis added).**

Reg. No.: 31,391

Francis J Maguire
SIGNATURE OF PRACTITIONER
Francis J. Maguire
(type or print name of practitioner)

Tel. No.: (203) 261-1234

Customer No. 004955

Ware, Fressola, Van Der Sluys & Adolphson LLP
755 Main Street, P.O. Box 224
P.O. Address

Monroe, Connecticut 06468

NOTE: ***The claim to priority need be in no special form and may be made by the attorney or agent, if the foreign application is referred to in the oath or declaration, as required by § 1.63.***

CERTIFICATE OF MAILING (37 CFR 1.10)

I hereby certify that this correspondence is, on the date shown below, is being deposited with the United States Postal Service on the date shown below is being deposited with the United States Postal Service with sufficient postage as Express Mail No. EV137073922US in an envelope addressed to the: Box Patent Application, U.S. Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202.

Date: March 26, 2003

Margery B. Hood
(Type or print name of person mailing paper)

Margery B. Hood
(Signature of person mailing paper)

CERTIFICATE

I, Tuulikki Tulivirta, hereby certify that, to the best of my knowledge and belief, the following is a true translation, for which I accept responsibility, of Finnish Patent Application No. 20020594 filed on 27 March 2002.

Tampere, 11 March 2003

VIRALLINEN KÄÄNTÄJÄ
TUULIKKI
TULIVIRTA
CERTIFIED TRANSLATOR

Tuulikki Tulivirta
Certified Translator (Act 1148/88)

Tampereen Patenttitoimisto Oy
Hermiankatu 12 B
FIN-33720 TAMPERE
Finland

A method and a system for determining the power consumption in connection with an electronic device, and an electronic device

The present invention relates to a method for determining the power consumption in an electronic device, to which a peripheral device is connected, which is supplied with power from the electronic device. The invention also relates to a system which comprises an electronic device provided with means for connecting a peripheral device and means for supplying power to the peripheral device, and which system comprises means for determining the power consumption. Furthermore, the invention relates to an electronic device provided with means for connecting a peripheral device, means for supplying power to the peripheral device, and means for determining the power consumption of the peripheral device. Moreover, the invention relates to a peripheral device provided with means for connecting the peripheral device to an electronic device, from which the power needed for using the peripheral device is arranged to be supplied to the peripheral device.

At present, several such electronic devices are in use, to which it is possible to connect various peripheral devices, *e.g.* to expand the properties of the electronic device and to produce auxiliary functions. For example, it is possible to connect peripheral devices, such as connection cards (*e.g.* PCMCIA cards), to laptop computers to connect the laptop computer to a local area network, a landline or wireless telephone network, *etc.* Furthermore, peripheral devices can be used to expand the memory of the laptop computer, to connect an external fixed disk, a CDROM station, or the like.

The MultiMediaCard™ Association is, among other things, developing a standard for memory expansion boards (MultiMediaCard™; MultiMediaCard™ is a trademark of Infineon Technologies AG). These memory expansion boards can be used in various portable electronic devices, such as wireless communication devices and communicator type devices, to expand the memory capacity.

Because the peripheral devices can be connected to a variety of devices, the power consumption of the peripheral device should not exceed the maximum power that can be supplied from the electronic device to the peripheral device. Otherwise, the operation of the peripheral device and/or the electronic device may be disturbed and the electronic device may even be overheated. On the other hand, the power consumption requirements of different peripheral devices may be very different, wherein manufacturers of electronic devices should provide for the maximum power consumption in the power supply of the peripheral device connection. Solutions are known, such as Nokia Communicator 9110/9210, in which the power supply of the peripheral device connection of the electronic device is provided with a relatively efficient regulator, for example in the order of 150 mA/3 V. Such an efficient regulator is a relatively bulky component, which may cause placement problems, particularly in portable electronic devices. The provision for the maximum power consumption will be unnecessary in such electronic devices, whose users do not use, in connection with the electronic device, such a peripheral device whose power consumption is close to the maximum power consumption of the peripheral device designed for the electronic device. On the other hand, another user of a similar electronic device may use such a peripheral device whose power consumption is in the order of the maximum power consumption of the peripheral device designed for the electronic device.

In some electronic devices and peripheral devices to be connected to them, the operating voltage is selected at the stage when the peripheral device is turned on, *e.g.* when the electronic device is turned on or when the peripheral device is connected. Thus, signalling will be performed between the electronic device and the peripheral device, for the electronic device to determine the level of the operating voltage required by the peripheral device and to select an operating voltage suitable for the peripheral device to the operating voltage line(s) of the peripheral device.

In said MultiMediaCard Association, a maximum limit has been proposed for the power consumption of memory cards of the MultiMediaCard™ type. Thus, in electronic devices supporting this standard, the

provision is made to supply a defined maximum power to the peripheral device. Moreover, the power consumption of memory cards of the MultiMediaCard™ type should thus not exceed the defined maximum limit. Such an arrangement is difficult, for example, for the reason that the power consumption of new memory cards to be developed is limited to this maximum value, wherein it may be an impediment for the implementation of such memory cards whose power consumption cannot be made smaller than the selected maximum limit. If the maximum limit is set so high that the power consumption of other memory cards to be developed later on is also very likely to be smaller than this, it will mean that relatively efficient and large regulators must be used in electronic devices.

The power consumption of the peripheral device is normally proportional to the clock frequency used in the peripheral device, wherein an increase in the clock frequency will increase the power consumption. In a corresponding manner, to decrease the power consumption, the clock frequency of the peripheral device can be decreased, if this is possible in view of the other functions of the peripheral device. However, the operating rate of the peripheral device will thus decrease, which is not necessarily desirable. Also, the bus width used in the peripheral device has an effect on how much power is consumed in the peripheral device.

It is an aim of the present invention to provide an improved method and system for determining the power consumption to be suitable in each situation. It is another aim of the invention to provide an electronic device and a peripheral device for applying the method. The invention is based on the idea of determining at least a first and a second maximum value for the power consumption, wherein the electronic device and the peripheral device set the power consumption to a value between these first and second maximum values. Thus, in different operating situations, for example the peripheral device can adjust its power consumption to be suitable for the situation. The method according to the present invention is primarily characterized in determining, for the power consumption, at least a first maximum value and a second maximum value which is higher than the first maximum value,

and setting, between the electronic device and the peripheral device, the maximum for the power consumption of the peripheral device to a value which is substantially between said first and second maximum values. The system according to the invention is primarily characterized in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum for the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value. The electronic device according to the invention is primarily characterized in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum for the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value. Furthermore, the peripheral device according to the invention is primarily characterized in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum for the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value.

The present invention shows remarkable advantages over solutions of prior art. By the method according to the invention, it is possible to avoid the use of an unnecessarily large regulator in an electronic device, which saves costs, and wherein the size of the electronic device can, in some cases, be reduced and, on the other hand, problems of heating caused by high power consumption can be avoided. Also the power consumption can be reduced, which is advantageous particularly in portable devices. By means of the invention, the peripheral device connection can also be provided with flexibility, because the power consumption of the peripheral device can be adjusted and set to a value suitable for each situation of use. Also, the clock frequency and bus width of the peripheral device can be changed in the system

according to an advantageous embodiment of the invention. Furthermore, the invention makes it possible that new peripheral devices to be developed will function in connection with electronic devices made earlier, and existing peripheral devices will function in connection with new electronic devices to be developed. With the solution according to the invention, it is also possible to achieve an improvement in the user-friendliness of the electronic device, for example, in a situation in which the peripheral device cannot fully operate on a lower level of power consumption but it can, however, inform the electronic device about this. Thus, the electronic device can take care of the shutdown (turning off) of the peripheral device in the appropriate way and notify the user of this.

In the following, the invention will be described in more detail with reference to the appended drawings, in which

Fig. 1 shows the system according to a preferred embodiment of the invention in a reduced block chart,

Fig. 2 shows a system according to a second preferred embodiment of the invention in a reduced manner,

Fig. 3 shows signalling in the method according to a preferred embodiment of the invention in a reduced manner, and

Fig. 4 shows a peripheral device according to yet another preferred embodiment of the invention in a reduced block chart.

In the system according to an advantageous embodiment of the invention, shown in Fig. 1, the electronic device 1 is exemplified by a wireless communication device. In this example, the peripheral device 2 is a memory card, such as a memory card complying with the Multi-MediaCard™ standard. However, it will be obvious that the present invention is not limited solely to such electronic devices and peripheral devices, but the invention can also be applied in connection with other electronic devices and peripheral devices. The peripheral device 2 can

be, for example, an interface card or also another device. The electronic device 1 contains a control block 3 comprising one or more processors, such as a micro controller unit (MCU). Furthermore, the electronic device 1 comprises a memory 4, a user interface 5 and means 6 for performing mobile station functions, such as GSM and/or UMTS mobile communication means. The user interface 5 preferably comprises a display, a keypad and audio means in a way known as such. For the connection of the peripheral device 2, the electronic device 1 is provided with connecting means 7 which comprise at least one connector 8 as well as the necessary I/O blocks 9, for example to connect the buses of the peripheral device 2 and the electronic device 1 to each other.

The peripheral device is also provided with corresponding connecting means 10 for connecting the peripheral device 2 to the electronic device 1. The connecting means 10 of the peripheral device comprise at least one connector 11 which can be connected to the connector 8 of the electronic device 1, and an I/O block 12. The power supply to the peripheral device 2 is arranged from the electronic device 1 via the connectors 8, 11. The I/O blocks are used for communication between the electronic device 1 and the peripheral device 2. This can take place as parallel data transmission or serial data transmission. For example, said peripheral device according to the MultiMediaCard™ specifications applies serial data transmission. However, in view of the present invention, it is not significant, in which format the data transmission between the electronic device 1 and the peripheral device 2 is carried out.

The peripheral device 2 also comprises a processor 13 or the like for controlling the functions of the peripheral device 2. Furthermore, the peripheral device comprises a memory 14, such as a read/write memory (RAM), *e.g.* for the storage of data, as well as a read-only memory (ROM, NVRAM) for the storage of the program code. The processor is responsible, for example, for controlling the I/O blocks in the data transmission between the peripheral device 2 and the electronic device 1. At least a first maximum value and a second maximum value for power consumption, which are used in the method according to the

present invention, are also stored in the memory 14 of the peripheral device. Furthermore, the peripheral device comprises means for generating one or more clock signals required for the operation of the processor, such as a clock generator 16.

The following is a description of the operation of the method according to a preferred embodiment of the invention in a system shown in Fig. 1. For example, information on whether a peripheral device 2 is placed in the connector 8 of the connecting means of the electronic device, is transmitted via the I/O blocks to the electronic device 1. This can be implemented, for example, by providing the I/O block 9, 12 with a detection line 15 whose state is changed when the peripheral device 2 is placed in the connector 8. In this advantageous embodiment of the invention, the detection line 15 is implemented so that the detection line 15 is set in the logical 1 state by means of a pull-up resistance R in the electronic device 1. In the system of Fig. 1, the change of state is achieved in such a way that the peripheral device 2 earths the detection line 15, wherein the state of the detection line 15 is changed to the logical 0 state. This change of state is detected in the electronic device 1, for example, in such a way that the change of state causes an interrupt in the control block 3, wherein a corresponding interrupt service program is run and the running of the initializing functions of the peripheral device are started. After the operating voltages have been coupled to the peripheral device, the processor 13 of the peripheral device 2 will start to run its own initializing operations. For example, the power consumption of the peripheral device 2 is set to a default value which, in this advantageous embodiment, is a power consumption value according to the first maximum limit. In this context, it is assumed that the first maximum limit is lower than the second maximum limit. The processor also sets the frequency of the clock generator 16 to correspond to this power consumption value. Typically, the frequency of the clock generator is set to a minimum value. In all peripheral devices 2, it is not necessarily possible to control the frequency of the clock generator 16, wherein the clock generator 16 cannot be used for controlling the power consumption.

In the operations of initializing the peripheral device, performed by the electronic device 1, the type of the peripheral device 2 is preferably examined, which may affect the type of initialization operations to be performed. However, this description will only discuss the operations which are essential in view of the invention. The signalling to be performed in this method according to the advantageous embodiment of the invention is illustrated in a reduced manner in the appended Fig. 3. The determination of the type of the peripheral device 2 will be followed by determining the first and second maximum limits for power consumption which have been stored on the card. Thus, a maximum limit reading message is preferably transmitted from the electronic device 1 to the peripheral device 2. This is illustrated by arrow 301 in the chart of Fig. 3. The message is received in the peripheral device 2 and its content is preferably examined in a processor 13. On the basis of the message, the processor 13 reads the first maximum limit and the second maximum limit from the memory 14 (block 302 in Fig. 3). If there are more than two maximum limits, the number of the maximum limits is preferably stored in the memory means, wherein the processor 13 reads the values of all the maximum limits from the memory 14. After this, the processor 13 generates a reply message (block 303) containing the requested information, such as the first and second maximum limits and, if necessary, also the number of the maximum limits. In the case of several maximum limits, also the values of the other maximum limits are preferably included in the message. The message is transmitted via the I/O blocks 9, 12 to the electronic device (arrow 304), in which the control block reads the information of the received message and, if necessary, stores them in the memory 4 of the electronic device.

After the maximum limits of power consumption supported by the peripheral device are known in the electronic device 1, it is possible to start to adjust the power consumption of the peripheral device, if necessary. Let us assume that the electronic device 1 is capable of supplying the power corresponding to the second maximum limit to the peripheral device 2. Thus, a power control message is transmitted from the electronic device 1 to the peripheral device 2 (arrow 305). This power control message indicates the power consumption value which is to be set as the maximum value for the peripheral device 2, for example said

second maximum limit. The processor 13 of the peripheral device examines the type of the received message, and after determining that it is a power control message, reads the maximum value for power consumption indicated in the message (block 306). Next, the processor 13 of the peripheral device sets, for example the operating frequency of the clock generator 16 to a value corresponding to this maximum value for power consumption, for example to the highest possible frequency. In some embodiments, the bus widths within the processor can also be changed according to the maximum limit used for power consumption. Furthermore, the peripheral device 2 preferably informs the electronic device 1 that the power consumption has been limited to the requested value (arrow 307).

If the electronic device 1 cannot supply the peripheral device 2 with the power of the second maximum limit, or if, for another reason, the electronic device 1 tends to set the maximum value for power consumption lower than the second maximum limit, it is possible to perform signalling, by which the electronic device 1 and the peripheral device try to find such a maximum limit for power consumption which is suitable in the situation. This can be carried out, for example, in such a way that the electronic device 1 selects, between the first and second maximum limits, a value which is a maximum value in view of the electronic device 1. Information about this limit is transferred to the peripheral device 2, in which the suggested value is examined 13, and if it is found acceptable, this information is transferred to the electronic device 1. If the peripheral device 2 cannot set its own power consumption to such a level which corresponds to the suggested maximum value, the peripheral device 2 will suggest a lower value between the first and second maximum values. If this value is possible in view of the electronic device 1, the electronic device 1 will transmit this information to the peripheral device 2, in which the power consumption is set to this value. If the value suggested by the peripheral device 2 is not suitable, the electronic device 1 advantageously selects another, preferably lower value which, however, is at least equal to the first maximum limit, and reports it to the peripheral device 2. The above-presented steps are iterated, until such a power consumption value is found which is suitable for both the electronic device 1 and the peripheral device 2. In

some cases, it may occur that the only suitable value is the first maximum value, wherein the power consumption does not need to be adjusted, because this value is the default value.

There may also be a need to change the value of the power consumption during the operation of the electronic device 1 and the peripheral device 2 connected to the same. For example, if the peripheral device is a transceiver card, such as a mobile station card or a modem card, there may be a need to significantly change the power consumption limit of the peripheral device 2, for example, for the time of a transmission. Thus, at the stage when *e.g.* the peripheral device 2 detects a need to change the power consumption, it transmits a message to the electronic device 1 and proposes a new power consumption value which is, however, in the range between the first and second maximum values. An exchange of messages is performed between the electronic device 1 and the peripheral device 2 by applying the above-described principles, to control the power consumption of the peripheral device according to the need. When the need for power consumption is changed again, a new adjustment of the power consumption can be made.

The need to change the power consumption of the peripheral device may also develop in the electronic device 1. For example, when the operation of the electronic device 1 shifts to a power saving mode, or when the charge of a battery (not shown) in the electronic device is reduced, the electronic device 1 may control the peripheral device 2 to shift to a less power consuming state.

The peripheral device according to the invention can also be connected to such an electronic device 1 which does not have a possibility to adjust the power consumption. Thus, the peripheral device 2 sets a default value, *i.e.* preferably the first maximum limit, as the power consumption value. Consequently, the peripheral device according to the invention can also be connected to such an electronic device 1 in which the steps of the method according to the invention are not carried out to control the power consumption of the peripheral device 2.

Above, the use of more than two different maximum limits were mentioned as the maximum values for power consumption. In this context, it is assumed that the other maximum limits are between the first and second maximum limits. These different maximum limits are feasible, for example, in such applications, in which different bus widths can be selected in the peripheral device. For example, in the system of Fig. 2, the bus width of the connection between the peripheral device and the electronic device can be selected to be any of the three values: 8, 16 or 32 bits. At the same time, this bus width selected for the connection is, in this advantageous embodiment, also used in the internal bus 17 of the peripheral device 2. Typically, the power consumption is the higher, the wider the bus used. Thus, the presumption is preferably that the bus width at the start-up stage is 8 bits, but the electronic device 1 and the peripheral device 2 may negotiate on the use of another bus width, *i.e.* on the change of the maximum limit for power consumption. This can be implemented by applying the principles described above. However, it will be obvious that said bus widths are only some non-restricting examples of bus widths.

The frequency of the clock generator 16 of the peripheral device is not necessarily adjustable in a stepless manner, but it is possible to select a value for the frequency from some predetermined values. Thus, the maximum limits for power consumption corresponding to these different frequencies can be stored as said maximum limits in the peripheral device, or if only the first maximum limit (lowest power consumption) and the second maximum limit (highest power consumption) are stored, it is possible to perform the exchange of messages between the electronic device 1 and the peripheral device, as described above in this description, to adjust the suitable power consumption limit.

Consequently, the power consumption of the peripheral device 2 can be adjusted *e.g.* by changing the clock frequency and/or the bus width, but it is obvious that other methods for adjusting the power consumption are also known and are applicable in connection with the invention. The power consumption can also be controlled by controlling the operating voltage, if the operating voltage of the peripheral device 2 does not need to be a given constant value. Peripheral devices are known,

in which the operating voltage can be selected to be, for example, either 3 V, 3.3 V, or 5 V. Yet another example to be mentioned in this context of the possibilities to control the power consumption of the peripheral device is to control the current consumption of the peripheral device.

In an advantageous embodiment of the invention, at least a part of the memory of the peripheral device 2 is divided into two or more memory blocks, to form so-called storage banks. Thus, in the peripheral device, one or more of these memory blocks can be selected for use, *e.g.* on the basis of the maximum power consumption value defined for the peripheral device 2. With higher power consumption values, it is typically possible to take more memory blocks into use than with lower power consumption values. Figure 4 shows an example of the structure of such a peripheral device. In the peripheral device 2 shown in Fig. 4, the memory 14 is provided with four memory blocks 14a, 14b, 14c, 14d, but it will be obvious that in practical applications, the number of storage banks can, within the scope of the invention, also be other than four. To take the memory blocks 14a–14d into use and to remove them from service, connection lines 18a–18d are preferably provided from the processor 13, to couple *e.g.* the operating voltage to the desired memory blocks 14a–14d, or the coupling lines are used to switch each memory block 14a–14d either to an active mode or to a power-saving mode. Also the above-presented method can be used to control the power consumption of the peripheral device 2 instead of or in addition to the methods for controlling the power consumption as presented above in this description.

In the electronic device 1, the power control can be performed, for example, by providing the electronic device 1 with a power source whose output voltage can be changed. Thus, in the electronic device 1, the operating voltage to be supplied to the peripheral device is selected to be the voltage value corresponding to the power consumption at the time.

The method according to the invention can also be applied in the implementation of various contents for use in connection with electronic

devices 1, for example in the following way. As the peripheral device 2, it is possible to use a memory card, such as a card complying with the definitions of the MultiMediaCard™ standard, in which contents can be stored. In this context, contents refer to data files, application programs, electronic books, audiovisual information, such as music, videos, *etc.* For example, a content provider stores such contents on the memory card. Thus, the memory card 2 is connected to an electronic device provided with means for transferring the content to the memory card 2. Thus, before starting the storage, the electronic device and the memory card 2 set the power consumption of the memory card preferably to a value corresponding to the second maximum limit. This is possible, because in such an electronic device 1 used for storing contents, the power consumption of the memory card has hardly any significance, but the electronic device 1 can supply the memory card 2 with the sufficient power. The storage can thus be performed at a maximum rate, because the clock frequency and/or bus width of the memory card can be set to the maximum. Also, the checkup of the content stored on the memory card 2, to detect possible storage defects, can be performed at a maximum rate. Thanks to the maximum storage and/or checkup rate, the content production rate of the electronic device 1 can be increased when compared with methods of prior art.

In a corresponding manner, at the stage when the content stored on the memory card 2 is to be used in an electronic device 1, the power consumption of the memory card 2 can be set to a level which is suitable for the electronic device 1, for example to the lowest possible power consumption. Thus, when applying the method of the invention, the content production rate does not need to be limited according to the maximum power consumption value possible in the use of the content.

Because the method according to the invention can be used for the power control of the peripheral device, the peripheral device 2 can be connected to a variety of electronic devices. In some electronic devices, it is only possible to supply the peripheral device with the power (voltage and current) corresponding to the minimum power consumption, wherein the electronic device 1 does not need a large regu-

lator, and the size of the electronic device does not need to be increased because of the need of space for a large regulator. On the other hand, power consumption does not need to be restricted in peripheral devices 2 to be developed, because the suitable power consumption value can be negotiated by the electronic device and the peripheral device. Thus, if the peripheral device is connected to such an electronic device, in which a relatively high power can be supplied to the peripheral device connection, the peripheral device can be used as efficiently as possible (with a high clock frequency / large bus width). At the stage of initialization, even such a peripheral device will operate with a lower power consumption, until a suitable power consumption value has been selected. In the system according to the invention, it is possible to provide for the use of peripheral devices which will be developed in the future and may require even high power in electronic devices. However, it is not necessary to consider cards with a high power consumption in the design of all electronic devices.

It will be obvious that the steps to be taken in the setting of the power consumption can also be implemented in another way than the above-presented handshake in the form of messages. For example, the connection means 7, 10 can be provided with connection lines which are used to set the power consumption of the peripheral device. Furthermore, the invention can be applied in such a way that certain alternative (allowable) values are defined for said maximum limits, wherein the first maximum limit and the second maximum limit for each peripheral device is selected from the set of these alternative limits.

It should also be mentioned that the peripheral device 2 does not need to be a card-format peripheral device, but the peripheral device 2 used can also be another device which can be connected to the electronic device 1. One non-restrictive example to be mentioned of such a peripheral device is a camera which is connected, for example, to a wireless communication device, a computer, or the like. Thus, by controlling the power consumption, it is possible to affect the functional properties of the camera. For example, the rate of updating the images of the camera on the display of the electronic device may be lower with a lower power consumption than with a higher power consumption.

Thus, the electronic device 1 may preferably set the power consumption of the camera used as the peripheral device 2 on the basis of how high a power can be supplied by the electronic device 1 to the peripheral device. In an advantageous embodiment of the invention, also the user of the electronic device 1 can set a maximum limit for the power consumption, wherein the user can, if necessary, *e.g.* reduce the maximum limit to prolong the time of operation of the electronic device.

It is obvious that the present invention is not limited solely to the above-presented embodiments but it can be modified within the scope of the appended claims.

Claims:

1. A method for determining the power consumption in an electronic device (1), to which a peripheral device (2) is connected, to which the power is supplied from the electronic device (1), **characterized** in determining, for the power consumption, at least a first maximum value and a second maximum value which is higher than the first maximum value, and setting, between the electronic device (1) and the peripheral device (2), the maximum for the power consumption of the peripheral device (2) to a value which is substantially between said first and second maximum values.

2. The method according to claim 1, **characterized** in that said first maximum limit is used as a default value for the power consumption, wherein the power consumption of the peripheral device (2) is set, at the startup stage, to be substantially not higher than said first maximum limit.

3. The method according to claim 1 or 2, **characterized** in that said second maximum limit is used as the highest allowable limit for the power consumption.

4. The method according to claim 1, 2, or 3, **characterized** in that messages are transferred between the electronic device (1) and the peripheral device (2) for setting the power consumption of the peripheral device to a value substantially between said first maximum limit and said second maximum limit.

5. The method according to any of the claims 1 to 4, **characterized** in that at least one content is stored in the peripheral device (2), to be used in connection with the electronic device (1), wherein at the stage of storing the content, the power consumption set for the peripheral device (1) is a value corresponding to said second maximum limit, and at the stage of using the content, the power consumption set for the peripheral device (2) is a value corresponding to said first maximum limit.

6. The method according to any of the claims 1 to 5, **characterized** in that at least one clock signal is generated in the peripheral device (2) and that the power consumption of the peripheral device (2) is controlled by adjusting the frequency of at least one clock signal.

7. The method according to any of the claims 1 to 6, **characterized** in that the peripheral device (2) comprises at least one bus and that the power consumption of the peripheral device (2) is controlled by controlling the bus width of the peripheral device (2).

8. The method according to any of the claims 1 to 7, **characterized** in that the peripheral device (2) is provided with two or more storage blocks (14a–14d), wherein the power consumption of the peripheral device (2) is controlled by controlling the number of storage blocks (14a–14d) processed by the peripheral device (2) substantially simultaneously.

9. A system comprising an electronic device (1) with means (7) for connecting a peripheral device (2) and means (8) for supplying power to the peripheral device (2), and which system comprises means (7, 10, 14) for determining the power consumption, **characterized** in that at least a first maximum value and a second maximum value which is higher than the first maximum value are defined for the power consumption, and that the means for determining the power consumption comprise means 3, 13, 16, 17) for setting the maximum of the power consumption of the peripheral device (2) to a value which is between said first maximum value and second maximum value.

10. The system according to claim 9, **characterized** in that it comprises means (7, 10) for transferring messages between the electronic device (1) and the peripheral device (2) for setting the power consumption of the peripheral device to a value substantially between said first maximum limit and said second maximum limit.

11. The system according to claim 9 or 10, **characterized** in that the peripheral device (2) comprises means (16) for generating at least one clock signal, and that the system comprises means (7, 10, 13) for

controlling the power consumption of the peripheral device (2) by adjusting the frequency of said at least one clock signal.

12. The system according to claim 9, 10, or 11, **characterized** in that the peripheral device (2) comprises at least one bus, and that the system comprises means (7, 10, 13) for controlling the power consumption of the peripheral device (2) by adjusting the bus width of the peripheral device (2).

13. The method according to any of the claims 9 to 12, **characterized** in that the peripheral device (2) is provided with two or more storage blocks (14a–14d), and that the means (7, 10, 13) for controlling the power consumption of the peripheral device (2) comprise means (13, 18a–18d) for adjusting the number of storage blocks (14a–14d) processed by the peripheral device (2) substantially simultaneously.

14. The system according to any of the claims 9 to 13, **characterized** in that the electronic device (1) is a portable electronic device (1).

15. The system according to claim 14, **characterized** in that it comprises means (6) for performing mobile station functions.

16. An electronic device (1) provided with means (7) for connecting a peripheral device (2) and means (8) for supplying power to the peripheral device (2), and means (7) for determining the power consumption, **characterized** in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means (3) for setting the maximum of the power consumption of the peripheral device (2) to a value which is between said first maximum value and said second maximum value.

17. The electronic device (1) according to claim 16, **characterized** in that it comprises means (7) for transmitting messages from the peripheral device (2) and for receiving messages from the peripheral device (2), to set the power consumption of the peripheral device to a value

substantially between said first maximum limit and said second maximum limit.

18. The electronic device (1) according to claim 16 or 17, **characterized** in that it is a portable electronic device (1).

19. The electronic device (1) according to claim 18, **characterized** in that it comprises means for performing mobile station functions.

20. A peripheral device (2) provided with means (10) for connecting the peripheral device (2) to an electronic device (1), from which the power required for using the peripheral device (2) is arranged to be supplied to the peripheral device (2), **characterized** in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the peripheral device comprises means (13, 16, 17) for setting the maximum of the power consumption of the peripheral device (2) to a value which is between said first maximum value and said second maximum value.

21. The peripheral device (2) according to claim 20, **characterized** in that at least one content is stored in the peripheral device (2) to be used in connection with the electronic device (1).

22. The peripheral device (2) according to claim 20 or 21, **characterized** in that the peripheral device (2) comprises means (16) for generating at least one clock signal and means (13) for controlling the power consumption of the peripheral device (2) by controlling the frequency of said at least one clock signal.

23. The peripheral device (2) according to claim 20, 21, or 22, **characterized** in that the peripheral device (2) comprises at least one bus and means (13) for controlling the power consumption of the peripheral device (2) by controlling the bus width of the peripheral device (2).

24. The peripheral device (2) according to any of the claims 20 to 23, **characterized** in that the peripheral device (2) is provided with two or

more storage blocks (14a–14d), and that the means (7, 10, 13) for controlling the power consumption of the peripheral device (2) comprise means (13, 18a–18d) for controlling the number of storage blocks (14a–14d) processed by the peripheral device (2) substantially simultaneously.

25. The peripheral device (2) according to any of the claims 20 to 24, **characterized** in that it is a MultiMediaCard™ peripheral device.

Abstract

The present invention relates to a method and a system for determining the power consumption in an electronic device (1), to which a peripheral device (2) is connected, to which the power is supplied from the electronic device (1). At least a first maximum value and a second maximum value, higher than the first maximum value, are determined for the power consumption. Between the electronic device (1) and the peripheral device (2), a maximum for the power consumption of the peripheral device (2) is set to a value which is substantially between said first and second maximum values. The invention also relates to an electronic device (1) and a peripheral device (2), in which the method is applied.

Fig. 1

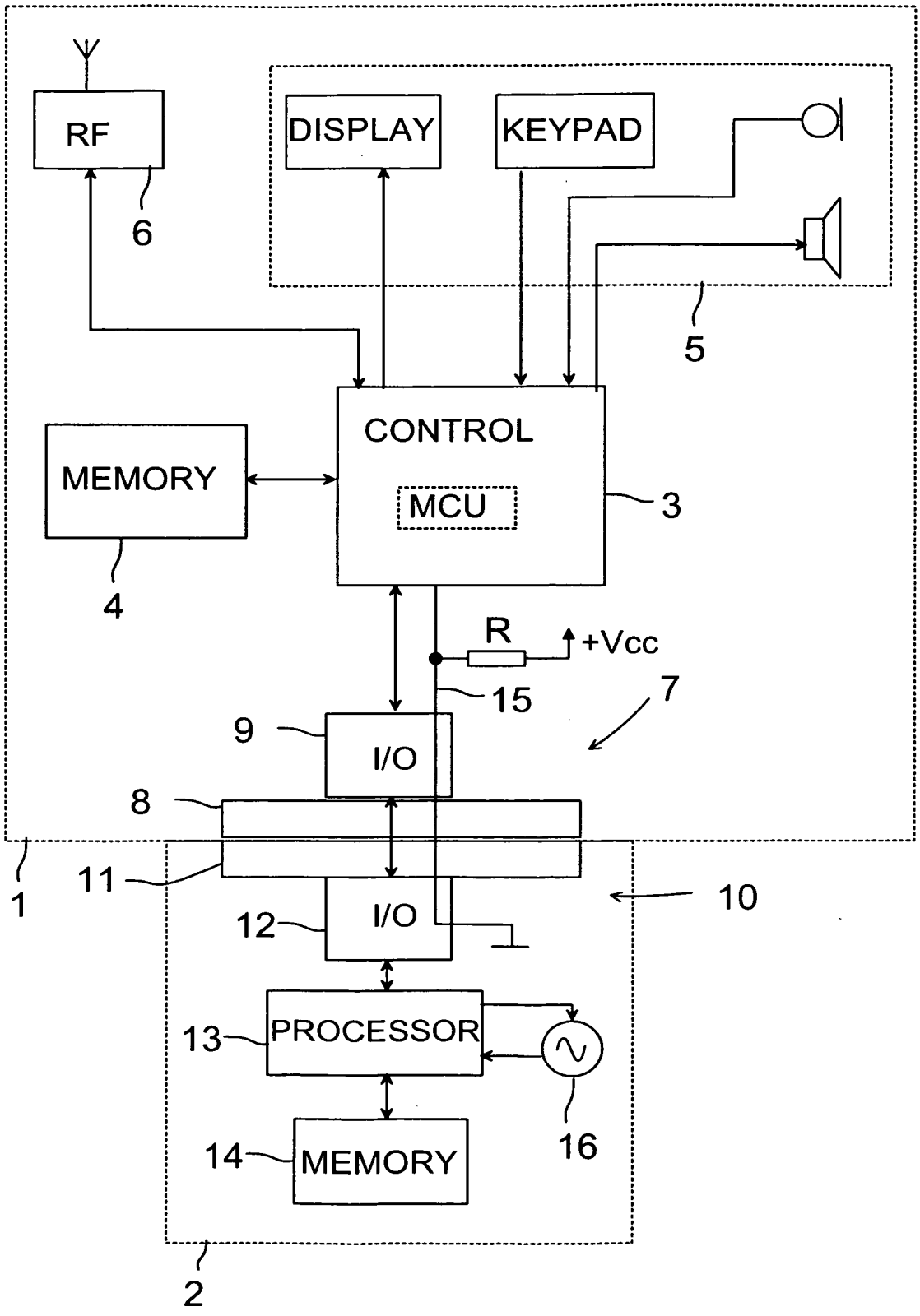
RF
6
DISPLAY
KEYPAD
5
CONTROL
MCU
3
MEMORY
4
R
+Vcc
15
7
9
I/O
8
1
11
10
12
I/O
13
PROCESSOR
16
14
MEMORY
2

Fig 1

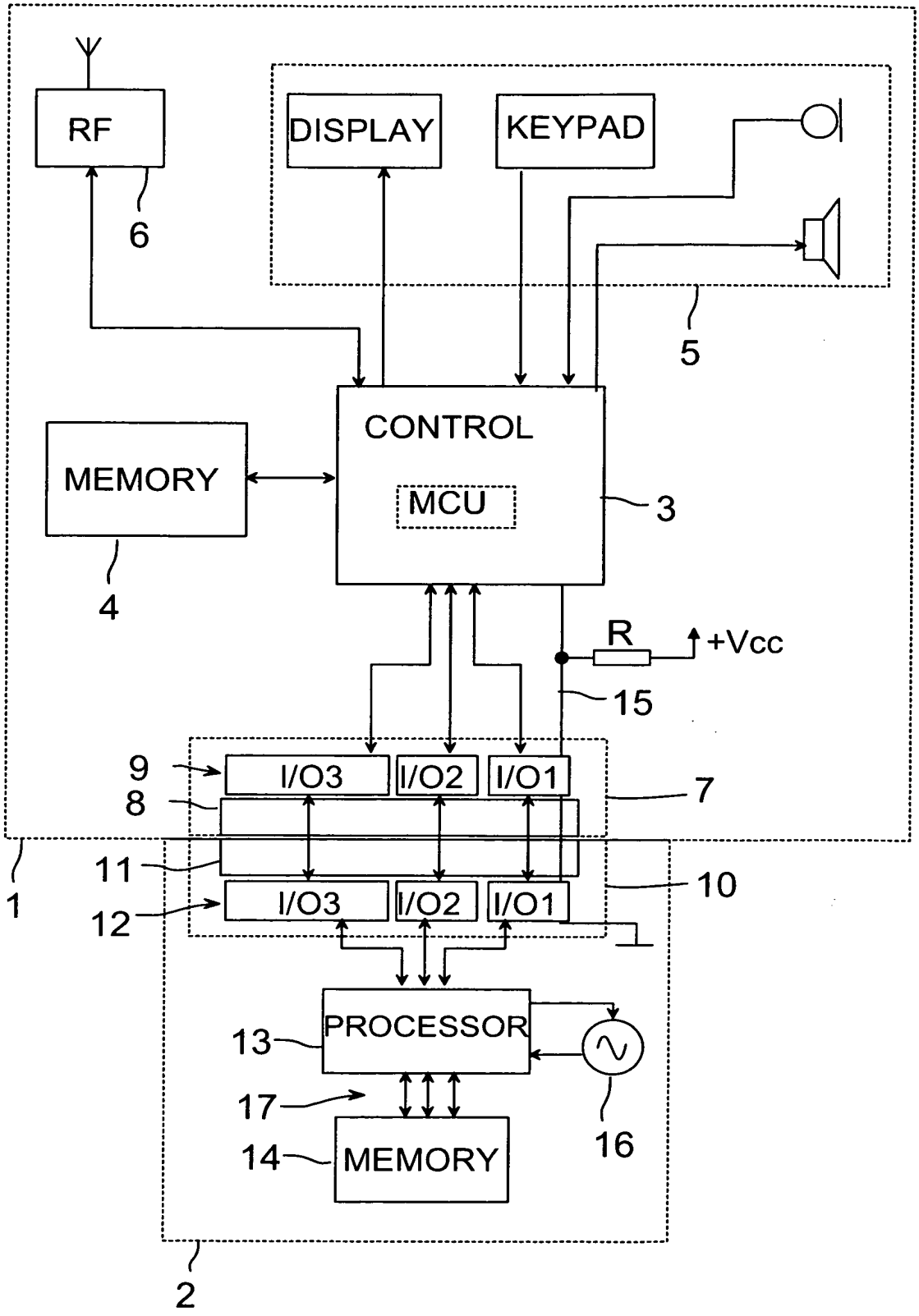

Fig 2

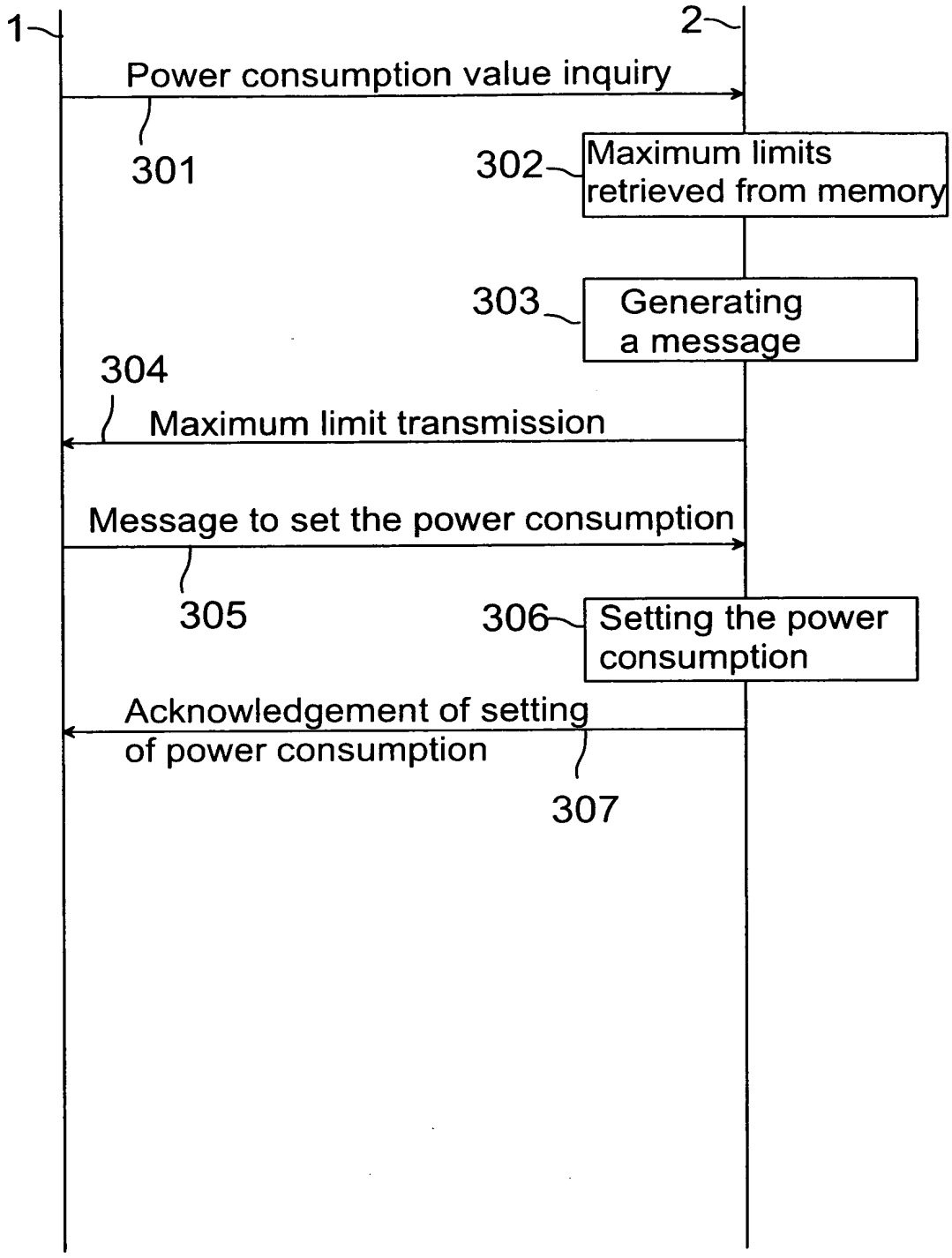
1
2
Power consumption value inquiry
301
302
Maximum limits retrieved from memory
303
Generating a message
304
Maximum limit transmission
Message to set the power consumption
305
306
Setting the power consumption
Acknowledgement of setting of power consumption
307

Fig 3

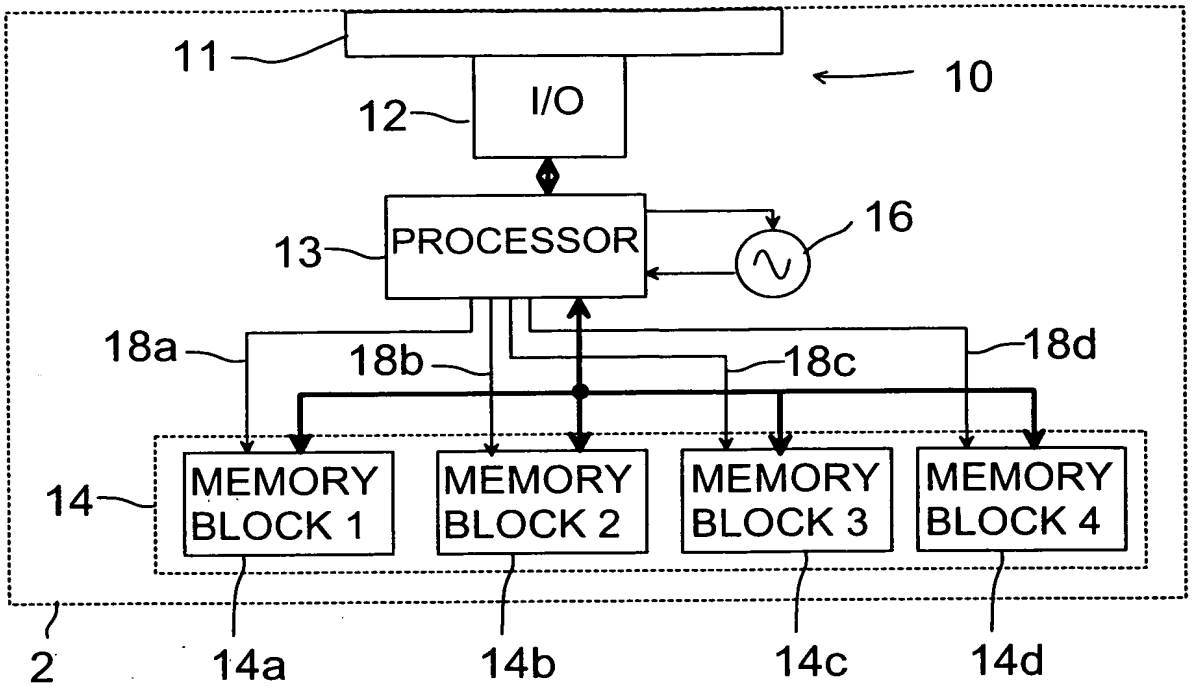
11
10
12
I/O
13
PROCESSOR
16
18a
18b
18c
18d
14
MEMORY BLOCK 1
MEMORY BLOCK 2
MEMORY BLOCK 3
MEMORY BLOCK 4
2
14a
14b
14c
14d

Fig 4

TRANSLATION FROM THE FINNISH ORIGINAL

NATIONAL BOARD OF PATENTS AND REGISTRATION

OFFICIAL ACTION

17 February 2003

Tampereen Patenttitoimisto Oy
Hermiankatu 12 B
33720 Tampere

Patent application No.	20020594
Class:	G01R AV
Applicant:	Nokia Corporation
Attorney:	Tampereen Patenttitoimisto Oy
Attorney's reference:	TP101235/TPu
Term	17 August 2003

The number and class of the patent application must be mentioned in your letter to the National Board of Patents and Registration

The independent claims 1, 9, 16 and 20 present an arrangement to be used for determining the power consumption of an electronic device, whereby a first maximum value and a second maximum value which is higher than the first maximum value, and setting, between the electronic device and the peripheral device, the maximum for the power consumption of the peripheral device to a value which is substantially between said first and second maximum values.

Publication WO 02/07494 (Sierra Wireless Inc., 31 January 2002, abstract and claim 1) discloses an arrangement, in which the power consumption of a portable computer and a PCMCIA card connected to it is limited to a value such that provides a current output which is between the values of two standard outputs. Because the arrangement presented in claims 1, 9, 16 and 20 is thus, in its essential parts, previously known from the publication WO 02/07494, the claims can thus not be accepted (Patent Act, Paragraph 2). Other claims present technical solutions which are known as such, for example, from US patent publications 5,606,704 (G06F 1/32, Pierce *et al.*, 25 February 1997), 5,613,130 (G06F 1/26, Teng *et al.*, 18 March 1997) and 5,737,616 (G06F 1/26, Watanabe, 7 April 1998).

The abstract in Swedish is missing.

(signed)
Annikki Visapää

Examining Engineer
Telephone: (09) 6939 5359

Enclosures:
Search report and copies of the references

Your response to the remarks is to be filed by the above mentioned due date. Upon failure to file a response with the Patent Office by the above-indicated due date or upon failure to take measures to correct the deficiencies stated in the present Official Action, the application is deemed to be withdrawn (Patent Act, 15 §). An application that is deemed to be withdrawn will be accepted under revival if you file your response or take measures to correct the stated defects within four months from the due date and, within the same term, pay the confirmed fee for revival of the application. If your response is filed at the Patent Office in due time, but the stated defects are not corrected in a manner that the application could be accepted, it is rejected, unless the Patent Office has a cause to issue a new Official Action (Patent Act, 16 §). A new specification, corrections made therein, and new claims shall always be filed in duplicate and thus Section 19 of the Patent Decree has to be taken into account.

The fee is based on Decree 1027/2001, with amendments, on the services payable to the National Board of Patents and Registration, issued by the Ministry of Trade and Industry.

TRANSLATION FROM THE FINNISH ORIGINAL

NATIONAL BOARD OF PATENTS AND REGISTRATION
Patent and Innovation Department

SEARCH REPORT

APPLICATION NO.	CLASSIFICATION
20020594	G01R 31/00

MATERIAL SEARCHED

Classes searched in the record of patent publications (FI, SE, NO, DK, DE; CH; EP; WO, GB, US):
G01R

Data searches and other material
Epodoc, WPI

REFERENCES

Category *)	Identification data of the publication	Relates to claims
X, Y	WO 02/07494 (Sierra Wireless Inc., 31 Jan. 2002), claim 1	1, 9, 16, 20
Y	US-5,606,704 (G06F 1/32, Pierce *et al.*, 25 Feb. 1997), the whole publication	1-25
Y	US-5,613,130 (G06F 1/26, Teng *et al.*, 18 Mar. 1997), the whole publication	1-25
Y	US-5,737,616 (G06F 1/26, Watanabe, 7 April 1998), the whole publication	1-25

*) X Publication of particular relevance in view of patentability when the publication is taken alone
Y Publication of particular relevance in view of patentability when the publication is combined with one or more such publications
A Publication defining the general state of art, not considered relevant in view of patentability

Date	Examiner
17 February 2003	Annikki Visapää

PATENTTI- JA REKISTERIHALLITUS VÄLIPÄÄTÖS

17.02.2003

Tampereen Patenttitoimisto Oy

Hermiankatu 12 B

33720 Tampere

Patenttihakemus nro:	20020594
Luokka:	G01R AV
Hakija:	Nokia Corporation
Asiamies:	Tampereen Patenttitoimisto Oy
Asiamiehen viite:	TP101235/TPu
Määräpäivä:	17.08.2003

Patenttihakemuksen numero ja luokka on mainittava kirjelmässänne PRH:lle

Itsenäisissä patenttivaatimuksissa 1, 9, 16 ja 20 esitetään elektroniikkalaitteen tehonkulutuksen määrittämisessä käytettävä järjestely, jossa määritetään tehonkulutukselle ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo ja elektroniikkalaitteen ja oheislaitteen välillä suoritetaan oheislaitteen tehonkulutuksen maksimin asettaminen arvoon, joka on olennaisesti ensimmäisen ja toisen maksimiarvon välissä.

Julkaisusta WO-02/07494 (Sierra Wireless Inc., 31.1.02, tiivistelmä ja vaatimus 1) tunnetaan järjestely, jossa kannettavan tietokoneen ja siihen liitetetyn PCMCIA-kortin tehonkulutusta rajoitetaan arvoon, jolla saadaan ulostuloteho, joka on kahden standardiulostulotehon arvon välissä. Koska patenttivaatimuksissa 1, 9, 16 ja 20 esitetty järjestely on näin ollen olennaisilta osiltaan ennestään tunnettu julkaisusta WO-02/07494, ei patenttivaatimuksia voida hyväksyä (PL 2 §). Muissa vaatimuksissa on esitetty teknisiä ratkaisuja, jotka ovat sinänsä tunnettuja esimerkiksi US-patenttijulkaisuista 5606704 (G06F 1/32, Pierce et. al., 25.2.97), 5613130 (G06F 1/26, Teng et al., 18.3.97) ja 5737616 (G06F 1/26, Watanabe, 7.4.98).

Ruotsinkielinen tiivistelmä puuttuu.

Annikki Visapää

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Puhelin: (09) 6939 5359

Liitteenä tutkimusraportti ja viitejulkaisukopiot

Lausumanne huomautusten johdosta on annettava viimeistään yllämainittuna määräpäivänä. Jollette ole antanut lausumaanne virastoon viimeistään mainittuna määräpäivänä tai ryhtynyt toimenpiteisiin tässä välipäätöksessä esitettyjen puutteellisuuksien korjaamiseksi, jätetään hakemus sillensä (patenttilain 15 §). Sillensä jätetty hakemus otetaan uudelleen käsiteltäväksi, jos Te neljän kuukauden kuluessa määräpäivästä annatte lausumanne tai ryhdytte toimenpiteisiin esitettyjen puutteellisuuksien korjaamiseksi ja samassa ajassa suoritatte vahvistetun uudelleenkäsittelymaksun. Jos lausumanne on annettu virastoon oikeassa ajassa, mutta esitettyjä puutteellisuuksia ei ole siten korjattu, että hakemus voitaisiin hyväksyä, se hylätään, mikäli virastolla ei ole aihetta antaa Teille uutta välipäätöstä (patenttilain 16 §). Uusi keksinnön selitys, siihen tehdyt lisäykset ja uudet patenttivaatimukset on aina jätettävä kahtena kappaleena ja tällöin on otettava huomioon patenttiasetuksen 19 §.

Maksu perustuu kauppa- ja teollisuusministeriön antamaan asetukseen 1027/2001 Patentti- ja rekisterihallituksen maksullisista suoritteista muutoksineen.

PATENTTI- JA REKISTERIHALLITUS **TUTKIMUSRAPORTTI**
Patentti- ja innovaatiolinja

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X,Y	WO-02/07494 (Sierra Wireless Inc., 31.1.02), vaatimus 1	1, 9, 16, 20
Y	US-5606704 (G06 F 1/32, Pierce et.al, 25.2.97), koko julkaisu	1-25
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Y	US-5737616 (G06F 1/26, Watanabe, 7.4.98), koko julkaisu	1-25

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Menetelmä ja järjestelmä tehonkulutuksen määrittämiseksi elektroniikkalaitteen yhteydessä ja elektroniikkalaite

Nyt esillä oleva keksintö kohdistuu menetelmään tehonkulutuksen määrittämiseksi elektroniikkalaitteessa, johon liitetään oheislaite, jolle teho syötetään elektroniikkalaitteesta. Keksintö kohdistuu lisäksi järjestelmään, joka käsittää elektroniikkalaitteen, jossa on välineet oheislaitteen liittämiseksi ja välineet tehon syöttämiseksi oheislaitteelle, ja joka järjestelmä käsittää välineet tehonkulutuksen määrittämiseksi. Keksintö kohdistuu vielä elektroniikkalaitteeseen, jossa on välineet oheislaitteen liittämiseksi, välineet tehon syöttämiseksi oheislaitteelle, ja välineet oheislaitteen tehonkulutuksen määrittämiseksi. Keksintö kohdistuu vielä oheislaitteeseen, jossa on välineet oheislaitteen liittämiseksi elektroniikkalaitteeseen, josta oheislaitteen käyttämisessä tarvittava teho on järjestetty syötettäväksi oheislaitteelle.

Nykyisin käytössä on useita sellaisia elektroniikkalaitteita, joihin voidaan liittää erilaisia oheislaitteita mm. elektroniikkalaitteen ominaisuuksien laajentamiseksi ja lisätoimintojen aikaansaamiseksi. Esimerkiksi kannettaviin tietokoneisiin voidaan liittää oheislaitteita, kuten liitäntäkortteja (esim. PCMCIA-kortteja), joilla kannettava tietokone on liitettävissä lähiverkkoon, langalliseen tai langattomaan puhelinverkkoon, jne. Lisäksi oheislaitteiden avulla voidaan kannettavan tietokoneen muistia laajentaa, liittää ulkoinen kiintolevy, CDROM-asema tai vastaava.

MultiMediaCard™ Association on mm. kehittämässä standardia lisämuistikortteja varten (MultiMediaCard™; MultiMediaCard™ on Infineon Technologies AG:n tavaramerkki). Tällaisia lisämuistikortteja voidaan käyttää erilaisissa kannettavissa elektroniikkalaitteissa, kuten langattomissa viestimissä ja kommunikaattori-tyyppisissä laitteissa muistimäärän lisäämiseksi.

Oheislaitteiden liitettävyys erilaisiin laitteisiin aiheuttaa mm. sen, että oheislaitteen tehonkulutus ei saisi ylittää elektroniikkalaitteesta oheislaitteelle syötettävissä olevaa maksimitehoa. Muussa tapauksessa oheislaitteen ja/tai elektroniikkalaitteen toiminta saattaa häiriintyä ja

elektroniikkalaite voi jopa ylikuumentua. Toisaalta eri oheislaitteiden tehonkulutusvaatimukset voivat olla hyvinkin erilaiset, jolloin elektroniikkalaitteiden valmistajien tulisi varautua oheislaiteliitännän tehonsyötössä mahdollisimman suureen tehonkulutukseen. Tunnetaankin ratkaisuja, kuten Nokia Communicator 9110/9210, joissa elektroniikkalaitteen oheislaiteliitännän tehonsyöttö on järjestetty suhteellisen tehokkaalla regulaattorilla, esim. luokkaa 150 mA/3 V. Tällainen tehokas regulaattori on suhteellisen tilaa vievä komponentti, mikä erityisesti kannettavissa elektroniikkalaitteissa voi aiheuttaa sijoitteluongelmia. Mahdollisimman suureen tehonkulutukseen varautuminen on sellaisten elektroniikkalaitteiden osalta tarpeetonta, joiden käyttäjä ei käytä elektroniikkalaitteen yhteydessä sellaista oheislaitetta, jonka tehonkulutus on lähellä elektroniikkalaitteelle suunniteltua oheislaitteen maksimitehonkulutusta. Toisaalta joku toinen käyttäjä saattaa käyttää samanlaisessa elektroniikkalaitteessa sellaista oheislaitetta, jonka tehonkulutus on elektroniikkalaitteelle suunniteltua oheislaitteen maksimitehonkulutuksen suuruusluokkaa.

Joissakin elektroniikkalaitteissa ja niihin liitettävissä oheislaitteissa suoritetaan käyttöjännitteen valinta siinä vaiheessa kun oheislaite käynnistetään, esim. käynnistettäessä elektroniikkalaite tai oheislaitteen liittämisen yhteydessä. Tällöin elektroniikkalaitteen ja oheislaitteen välillä suoritetaan signalointia, jonka perusteella elektroniikkalaite päättelee oheislaitteen tarvitseman käyttöjännitteen suuruuden ja valitsee oheislaitteen käyttöjännitelinjaan (-linjoihin) oheislaitteelle sopivan käyttöjännitteen.

Mainitussa MultiMediaCard Association –järjestössä on ehdotettu maksimirajan asettamista MultiMediaCard™-tyyppisten muistikorttien tehonkulutukselle. Tällöin tätä standardia tukevissa elektroniikkalaitteissa varaudutaan siihen, että oheislaitteeseen voidaan syöttää määritetty maksimiteho. Lisäksi MultiMediaCard™-tyyppisten muistikorttien tehonkulutus ei tällöin saisi olla suurempi kuin määritetty maksimiraja. Tällainen järjestely on hankala mm. siitä syystä, että kehitettävien uusien muistikorttien tehonkulutus on rajoitettu tähän maksimiarvoon, joten se voi olla esteenä sellaisten muistikorttien toteuttamiselle, joiden tehonkulutusta ei voida saada valittua maksimirajaa pienemmäksi. Mi-

käli maksimiraja asetetaan niin korkeaksi, että suurella todennäköisyydellä myös myöhemmin kehitettävien muistikorttien tehonkulutus on lälä pienempi, merkitsee se sitä, että elektroniikkalaitteissa on käytettävä suhteellisen tehokkaita ja kookkaita regulaattoreita.

Oheislaitteen tehonkulutus on yleensä verrannollinen oheislaitteessa käytettävään kellotaajuuteen, joten kellotaajuuden kasvattaminen nostaa tehonkulutusta. Vastaavasti tehonkulutuksen pienentämiseksi voidaan oheislaitteen kellotaajuutta pienentää, mikäli se oheislaitteen muun toiminnan kannalta on mahdollista. Tällöin kuitenkin oheislaitteen toimintanopeus pienenee, mikä ei välttämättä ole toivottavaa. Myös oheislaitteessa käytössä olevalla väyläleveydellä on vaikutusta siihen, kuinka paljon tehoa oheislaitteessa kuluu.

Nyt esillä olevan keksinnön eräänä tarkoituksena on aikaansaada parannettu menetelmä ja järjestelmä tehonkulutuksen määrittämiseksi kulloiseenkin tilanteeseen sopivaksi. Lisäksi keksinnön tarkoituksena on aikaansaada elektroniikkalaite ja oheislaite, joissa menetelmää sovelletaan. Keksintö perustuu siihen ajatukseen, että määritetään tehonkulutukselle ainakin ensimmäinen ja toinen maksimiarvo, jolloin elektroniikkalaite ja oheislaite suorittavat tehonkulutuksen asettamisen johonkin arvoon näiden ensimmäisen ja toisen maksimiarvon välissä. Tällöin esimerkiksi oheislaite voi erilaisissa toimintatilanteissa säätää tehonkulutustaan tilanteeseen sopivaksi. Nyt esillä olevan keksinnön mukaiselle menetelmälle on pääasiassa tunnusomaista se, että määritetään tehonkulutukselle ainakin ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo, ja että elektroniikkalaitteen ja oheislaitteen välillä suoritetaan oheislaitteen tehonkulutuksen maksimin asettaminen arvoon, joka on olennaisesti mainittujen ensimmäisen ja toisen maksimiarvon välissä. Keksinnön mukaiselle järjestelmälle on pääasiassa tunnusomaista se, että tehonkulutukselle on määritetty ainakin ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo, ja että välineet tehonkulutuksen määrittämiseksi käsittävät välineet oheislaitteen tehonkulutuksen maksimin asettamisen arvoon, joka on mainittujen ensimmäisen maksimiarvon ja toisen maksimiarvon välissä. Keksinnön mukaiselle elektroniikkalaitteelle on pääasiassa tunnusomaista se, että

tehonkulutukselle on määritetty ainakin ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo, ja että välineet tehonkulutuksen määrittämiseksi käsittävät välineet oheislaitteen tehonkulutuksen maksimin asettamisen arvoon, joka on mainittujen ensimmäisen maksimiarvon ja toisen maksimiarvon välissä. Keksinnön mukaiselle oheislaitteelle on vielä pääasiassa tunnusomaista se, että tehonkulutukselle on määritetty ainakin ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo, ja että välineet tehonkulutuksen määrittämiseksi käsittävät välineet oheislaitteen tehonkulutuksen maksimin asettamisen arvoon, joka on mainittujen ensimmäisen maksimiarvon ja toisen maksimiarvon välissä.

Nyt esillä olevalla keksinnöllä saavutetaan merkittäviä etuja tunnetun tekniikan mukaisiin ratkaisuihin verrattuna. Keksinnön mukaisella menetelmällä voidaan elektroniikkalaitteessa välttyä tarpeettoman suuren regulaattorin käyttämiseltä, mikä säästää kustannuksia, ja jolloin elektroniikkalaitteen kokoa voidaan joissakin tapauksissa pienentää ja toisaalta suuren tehonkulutuksen aiheuttamilta lämpenemisongelmilta välttyä. Myös virrankulutusta voidaan pienentää, mistä on etua erityisesti kannettavissa laitteissa. Keksinnöllä voidaan oheislaiteliitäntään aikaansaada myös joustavuutta, koska oheislaitteen tehonkulutusta voidaan säätää ja asettaa se kulloisenkin käyttötilanteen kannalta sopivaan arvoon. Myös oheislaitteen kellotaajuutta ja väyläleveyttä voidaan keksinnön erään edullisen suoritusmuodon mukaisessa järjestelmässä muuttaa. Keksintö mahdollistaa vielä sen, että kehitettävät uudet oheislaitteet toimivat aikaisemmin valmistettujen elektroniikkalaitteiden yhteydessä ja olemassa olevat oheislaitteet toimivat kehitettävien uusien elektroniikkalaitteiden yhteydessä. Keksinnön mukaisella ratkaisulla voidaan myös saada parannusta elektroniikkalaitteen käyttäjäystävällisyyteen mm. tilanteessa, jossa oheislaite ei voi toimia täysin alemmalla tehonkulutustasolla, mutta voi kuitenkin antaa tästä informaation elektroniikkalaitteelle. Tällöin elektroniikkalaite voi huolehtia oheislaitteen alasajosta (sammuttamisesta) asianmukaisesti ja muodostaa tästä ilmoituksen käyttäjälle.

Keksintöä selostetaan seuraavassa tarkemmin viitaten samalla oheisiin piirustuksiin, joissa

kuva 1 esittää keksinnön eräan edullisen suoritusmuodon mukaista järjestelmää pelkistettynä lohkokaaviona,

kuva 2 esittää keksinnön erään toisen edullisen suoritusmuodon mukaista järjestelmää pelkistetysti,

kuva 3 esittää pelkistetysti keksinnön eraän edullisen suoritusmuodon mukaisessa menetelmässä suoritettavaa signalointia, ja

kuva 4 esittää pelkistetysti keksinnön vielä erään edullisen suoritusmuodon mukaista oheislaitetta pelkistettynä lohkokaaviona.

Kuvan 1 mukaisessa keksinnön edullisen suoritusmuodon mukaisessa järjestelmässä käytetään esimerkkinä elektroniikkalaitteesta 1 langatonta viestintälaitetta. Oheislaitteena 2 on tässä esimerkissä muistikortti, kuten MultiMediaCard™-standardin mukainen muistikortti. On kuitenkin selvää, että nyt esillä olevaa keksintöä ei ole rajoitettu ainoastaan tällaisiin elektroniikkalaitteisiin ja oheislaitteisiin, vaan keksintöä voidaan sovellaa myös muiden elektroniikkalaitteiden sekä oheislaitteiden yhteydessä. Oheislaite 2 voi olla esimerkiksi liitäntäkortti tai myös jokin muu laite. Elektroniikkalaite 1 käsittää ohjauslohkon 3, jossa on yksi tai useampi suoritin, kuten mikro-ohjain (MCU). Lisäksi elektroniikkalaite 1 käsittää muistia 4, käyttöliittymän 5 sekä välineet 6 matkaviestintoimintojen suorittamiseksi, kuten GSM- ja/tai UMTS-matkaviestinvälineet. Käyttöliittymä 5 käsittää edullisesti näytön, näppäimistön ja audiovälineet sinansä tunnetusti. Oheislaitteen 2 liittämiseksi on elektroniikkalaitteeseen 1 muodostettu liitäntävälineet 7, jotka käsittävät ainakin yhden liittimen 8 sekä tarvittavat I/O-lohkot 9 mm. oheislaitteen 2 ja elektroniikkalaitteen 1 väylien kytkemiseksi toisiinsa.

Oheislaitteessa on myös vastaavat liitäntävälineet 10, jolla oheislaite 2 liitetään elektroniikkalaitteen 1 yhteyteen. Oheislaitteen liitäntävälineet 10 käsittävät ainakin yhden liittimen 11, joka on yhdistettävissä elektroniikkalaitteen 1 liittimeen 8 ja I/O-lohko 12. Tehonsyöttö oheislaitteelle

2 järjestetään elektroniikkalaitteesta 1 liittimien 8, 11 kautta. I/O-lohkojen kautta suoritetaan elektroniikkalaitteen 1 ja oheislaitteen 2 välinen kommunikointi. Tämä voidaan suorittaa rinnakkaismuotoisena tiedonsiirtona tai sarjamuotoisena tiedonsiirtona. Esimerkiksi mainitussa MultiMediaCard™-määritysten mukaisessa oheislaitteessa käytetään sarjamuotoista tiedonsiirtoa. Nyt esillä olevan keksinnön kannalta ei kuitenkaan ole merkitystä sillä, missä muodossa tiedonsiirto elektroniikkalaitteen 1 ja oheislaitteen 2 välillä toteutetaan.

Oheislaitteessa 2 on myös suoritin 13 tai vastaava oheislaitteen 2 toimintojen ohjaamiseksi. Oheislaite käsittää myös muistia 14, kuten luku/kirjoitusmuistia (RAM) mm. tietojen tallentamiseksi, sekä lukumuistia (ROM, NVRAM) suorittimen ohjelmakoodin tallennusta varten. Suoritin huolehtii mm. I/O-lohkojen ohjaamiseksi tiedonsiirrossa oheislaitteen 2 ja elektroniikkalaitteen 1 välillä. Oheislaitteen muistiin 14 on tallennettu myös ainakin tehonkulutuksen ensimmäinen maksimiarvo sekä toinen maksimiarvo, joita käytetään nyt esillä olevan keksinnön mukaisessa menetelmässä. Lisäksi oheislaite käsittää välineet suorittimen toiminnassa tarvittavan yhden tai useamman kellosignaalin muodostamiseksi, kuten kellogeneraattorin 16.

Seuraavaksi selostetaan keksinnön erään edullisen suoritusmuodon mukaisen menetelmän toimintaa kuvan 1 mukaisessa järjestelmässä. I/O-lohkojen kautta välitetään elektroniikkalaitteelle 1 mm. tieto siitä, onko elektroniikkalaitteen liitäntävälineiden liittimeen 8 asetettu oheislaitetta 2. Tämä voidaan toteuttaa esimerkiksi siten, että I/O-lohkossa 9, 12 on tunnistuslinja 15, jonka tila muuttuu, kun oheislaite 2 asetetaan liittimeen 8. Tunnistuslinja 15 on toteutettu keksinnön tässä edullisessa suoritusmuodossa siten, että tunnistuslinja 15 on elektroniikkalaitteessa 1 asetettu loogiseen 1-tilaan ylösvetovastuksella R. Tilanmuutos aikaansaadaan kuvan 1 mukaisessa järjestelmässä siten, että oheislaite 2 maadoittaa tunnistuslinjan 15, jolloin tunnistuslinjan 15 tila muuttuu loogiseksi 0-tilaksi. Tämä tilanmuutos havaitaan elektroniikkalaitteessa 1 esimerkiksi siten, että tilanmuutos aiheuttaa keskeytyksen ohjauslohkossa 3, jolloin suoritetaan vastaava keskeytyspalveluohjelma ja aloitetaan oheislaitteen alustustoimintojen suorittaminen. Sen jälkeen kun oheislaitteelle on kytketty käyttöjännitteet, aloittaa

oheislaitteen 2 suoritin 13 omien alustustoimintojensa suorittamisen. Oheislaitteen 2 tehonkulutus mm. asetetaan olelusarvoonsa, joka tässä edullisessa suoritusmuodossa on ensimmäisen maksimirajan mukainen tehonkulutusarvo. Tässä oletetaan, että ensimmäinen maksimiraja on pienempi kuin toinen maksimiraja. Suoritin asettaa myös kellogeneraattorin 16 taajuuden vastaamaan tätä tehonkulutusarvoa. Tyypillisesti kellogeneraattorin taajuus asetetaan minimiarvoon. Kaikissa oheislaitteissa 2 ei välttämättä ole mahdollista säätää kellogeneraattorin 16 taajuutta, jolloin kellogeneraattoria 16 ei voida käyttää tehonkulutuksen säätämisessä.

Elektroniikkalaitteen 1 suorittamissa oheislaitteen alustustoiminnoissa tutkitaan edullisesti oheislaitteen 2 tyyppi, mikä voi vaikuttaa siihen, minkälaisia alustustoimintoja suoritetaan. Tässä selityksessä rajoitutaan kuitenkin vain keksinnön kannalta olennaisten toimintojen kuvaamiseen. Keksinnön tämän edullisen suoritusmuodon mukaisessa menetelmässä suoritettavaa signalointia on kuvattu pelkistetysti oheisessa kuvassa 3. Sen jälkeen kun oheislaitteen 2 tyyppi on selvitetty, aloitetaan kortille tallennettujen tehonkulutuksen ensimmäisen ja toisen maksimirajan selvittäminen. Tällöin elektroniikkalaitteesta 1 lähetetään edullisesti maksimirajojen lukusanoma oheislaitteelle 2. Tätä esittaa nuoli 301 kuvan 3 kaaviossa. Oheislaitteessa 2 vastaanotetaan sanoma ja tutkitaan sen sisältö edullisesti suorittimessa 13. Sanoman perusteella suoritin 13 lukee muistista 14 ensimmäisen maksimirajan ja toisen maksimirajan (lohko 302 kuvassa 3). Mikäli maksimirajoja on useampia kuin 2, on muistivälineisiin edullisesti tallennettu tieto maksimirajojen lukumäärästä, jolloin suoritin 13 lukee kaikkien maksimirajojen arvot muistista 14. Tämän jälkeen suoritin 13 muodostaa vastaussanoman (lohko 303), joka sisältää kysytyt tiedot, kuten ensimmäisen ja toisen maksimirajan ja tarvittaessa myös tiedon maksimirajojen lukumäärästä. Useampien maksimirajojen tapauksessa sanomaan edullisesti liitetään muidenkin maksimirajojen arvot. Sanoma lähetetään I/O-lohkojen 9, 12 kautta elektroniikkalaitteelle (nuoli 304), jossa ohjauslohko lukee vastaanotetun sanoman tiedot ja tarvittaessa tallentaa ne elektroniikkalaitteen muistiin 4.

Sen jälkeen kun elektroniikkalaitteessa 1 on tiedossa oheislaitteen tukemat tehonkulutuksen maksimirajat, voidaan aloittaa oheislaitteen tehonkulutuksen säätäminen tarvittaessa. Oletetaan, että elektroniikkalaite 1 pystyy syöttämään oheislaitteelle 2 tolsta maksimirajaa vastaavan tehon. Tällöin elektroniikkalaitteesta 1 lähetetään tehonsäätösanoma oheislaitteelle 2 (nuoli 305). Tässä tehonsäätösanomassa ilmoitetaan se tehonkulutusarvo, joka halutaan asettaa oheislaitteen 2 maksimiarvoksi, esimerkiksi mainittu toinen maksimiraja. Oheislaitteen suoritin 13 tutkii vastaanotetun sanoman tyypin, ja havaittuaan kyseessä olevan tehonsäätösanoma, lukee sanomassa ilmoitetun tehonkulutuksen maksimiarvon (lohko 306). Tämän jälkeen oheislaitteen suoritin 13 asettaa esimerkiksi kellogeneraattorin 16 toiminlalaajuuden arvoon, joka vastaa tätä tehonkulutuksen maksimiarvoa, esimerkiksi suurimpaan mahdolliseen taajuuteen. Myös suorittimen sisäisiä väyläleveyksiä voidaan joissakin sovelluksissa muuttaa sen mukaan, minkälainen tehonkulutuksen maksimiraja on käytössä. Oheislaite 2 edullisesti ilmoittaa vielä elektroniikkalaitteelle 1, että tehonkulutus on rajoitettu pyydettyyn arvoon (nuoli 307).

Mikäli elektroniikkalaite 1 ei pysty tuottamaan oheislaitteelle 2 toisen maksimirajan mukaista tehoa, tai muusta syystä elektroniikkalaite 1 pyrkii asettamaan tehonkulutuksen maksimiarvon pienemmäksi kuin toinen maksimiraja, voidaan suorittaa signalointi, jolla elektroniikkalaite 1 ja oheislaite pyrkivät löytämään tilanteeseen sopivan tehonkulutuksen maksimirajan. Tämä voidaan toteuttaa esimerkiksi siten, että elektroniikkalaite 1 valitsee ensimmäisen ja toisen maksimirajan välistä sellaisen arvon, joka elektroniikkalaitteen 1 kannalta on maksimiarvo. Tieto tästä rajasta välitetään oheislaitteelle 2, jossa tutkitaan 13 ehdotettu arvo, ja jos se voidaan hyväksyä, välitetään siitä tieto elektroniikkalaitteelle 1. Jos oheislaite 2 ei voi asettaa omaa tehonkulutustaan sellaiseksi, joka vastaa ehdotettua maksimiarvoa, ehdottaa oheislaite 2 jotakin pienempää arvoa ensimmäisen ja toisen maksimiarvon välistä. Jos tämä arvo on elektroniikkalaitteen 1 kannalta mahdollinen, ilmoittaa elektroniikkalaite 1 tästä oheislaitteelle 2, jolla tehonkulutus asetetaan tähän arvoon. Mikäli oheislaitteen 2 ehdottama arvo ei ole sopiva, valitaan edullisesti elektroniikkalaitteessa 1 jokin muu, sopivimmin pienempi arvo, joka kuitenkin on vähintään yhtä suuri kuin ensimmäinen

maksimiraja, ja ilmoitetaan se oheislaitteelle 2. Edellä esitettyjä vaiheita toistetaan, kunnes on löydetty sellainen tehonkulutusarvo, joka sopii elektroniikkalaitteelle 1 ja oheislaitteelle 2. Joissakin tapauksissa saattaa käydä niin, että ainoa sopiva arvo on ensimmäinen maksimiarvo, jolloin tehonkulutusta ei tarvitse säätää, koska tämä arvo on oletusarvona.

Tehonkulutuksen arvoa voi olla tarve muuttaa myös elektroniikkalaitteen 1 ja siihen liitetyn oheislaitteen 2 toiminnan aikana. Esimerkiksi, jos oheislaitteena on lähetin/vastaanotinkortti, kuten matkaviestinkortti tai modeemikortti, saattaa oheislaitteen 2 tehonkulutusrajaa olla tarve muuttua merkittävästi esimerkiksi lähetyksen ajaksi. Tällöin siinä vaiheessa kun esim. oheislaite 2 havaitsee tarpeen muuttaa tehonkulutusta, lähettää se sanoman elektroniikkalaitteelle 1 ja ehdottaa uutta tehonkulutusarvoa, joka kuitenkin on ensimmäisen ja toisen maksimiarvon välissä. Elektroniikkalaitteen 1 ja oheislaitteen 2 välillä suoritetaan sanomien vaihtoa esim. edellä kuvattuja periaatteita soveltaen oheislaitteen tehonkulutuksen säätämiseksi tarvetta vastaavaksi. Tehonkulutustarpeen jälleen muuttuessa voidaan suorittaa uusi tehonkulutuksen säätö.

Oheislaitteen tehonkulutuksen muuttamistarve voi syntyä myös elektroniikkalaitteessa 1. Esimerkiksi elektroniikkalaitteen 1 toiminnan siirtyessä tehonsäästötilaan, tai elektroniikkalaitteen 1 akun (ei esitetty) varauksen pienentyessä, voi elektroniikkalaite 1 ohjata oheislaitetta 2 siirtymään vähemmän tehoa kuluttavaan tilaan.

Keksinnön mukainen oheislaite voidaan liittää myös sellaiseen elektroniikkalaitteeseen 1, jossa ei ole mahdollisuutta säätää tehonkulutusta. Tällöin tehonkulutusarvoksi asetetaan oheislaitteessa 2 oletusarvo, siis sopivimmin ensimmäinen maksimiraja. Keksinnön mukainen oheislaite voidaan siis liittää sellaiseenkin elektroniikkalaitteeseen 1, jossa ei ole toteutettu keksinnön mukaisen menetelmän vaiheita oheislaitteen 2 tehonkulutuksen säätämiseksi.

Edellä oli mainittu useamman kuin kahden eri maksimirajan käyttäminen tehonkulutuksen maksimiarvoina. Tässä oletetaan, että muut mak-

simirajat ovat ensimmäisen ja toisen maksimirajan välissä. Nämä erilaiset maksimirajat voivat tulla kyseeseen esimerkiksi sellaisissa sovelluksissa, joissa oheislaitteessa on mahdollista valita erilaisia väyläleveyksiä. Esimerkiksi kuvan 2 mukaisessa järjestelmässä on oheislaitteen ja elektroniikkalaitteen välisen liitännän väyläleveys valittavissa joksikin kolmesta arvosta: 8, 16 tai 32 bittiä. Samalla tämä liitännälle valittu väyläleveys tulee tässä edullisessa suoritusmuodossa käyttöön myös oheislaitteen 2 sisäisessä väylässä 17. Tyypillisesti tehonkulutus on sitä suurempi mitä leveämpää väylää käytetään. Tällöin oletuksena on sopivimmin se, että käynnistysvaiheessa väyläleveys on 8 bittiä, mutta elektroniikkalaite 1 ja oheislaite 2 voivat neuvotella muun väyläleveyden käyttämisestä, siis tehonkulutuksen maksimirajan muuttamisesta. Tämä voidaan toteuttaa edellä esitettyjä periaatteita soveltamalla. On kuitenkin selvää, että mainitut väyläleveydet ovat vain eräitä ei rajoittavia esimerkkejä väyläleveyksistä.

Oheislaitteen kellogeneraattorin 16 taajuus ei välttämättä ole portaattomasti säädettävissä, vaan taajuudelle voidaan valita jokin arvo joistakin määrätyistä arvoista. Näitä eri taajuuksia vastaavat tehonkulutuksen maksimirajat voidaan tällöin tallentaa oheislaitteelle mainituiksi maksimirajoiksi, tai mikäli tallennetaan vain ensimmäinen maksimiraja (pienin tehonkulutus) ja toinen maksimiraja (suurin tehonkulutus), voidaan elektroniikkalaitteen 1 ja oheislaitteen välillä suorittaa aikaisemmin tässä selityksessä esitetty sanomien vaihto sopivan tehonkulutusrajan säätämiseksi.

Oheislaitteen 2 tehonkulutusta voidaan siis säätää mm. kellotaajuutta ja/tai väyläleveyttä muuttamalla, mutta on selvää, että muitakin tehonkulutuksen säätökeinoja tunnetaan ja joita keksinnön yhteydessä voidaan soveltaa. Myös käyttöjännitteen säätämisellä voidaan tehonkulutusta säätää, mikäli oheislaitteen 2 käyttöjännitteen ei tarvitse olla tietty vakioarvo. Tunnetaan oheislaitteita, joissa käyttöjännitteeksi voidaan valita esimerkiksi joko 3 V, 3,3 V, tai 5 V. Vielä eräänä esimerkkinä oheislaitteen tehonkulutuksen säätämismahdollisuuksista mainittakoon tässä yhteydessä oheislaitteen virrankulutuksen säätäminen.

Keksinnön eräässä edullisessa suoritusmuodossa on ainakin osa oheislaitteen 2 muistista jaettu kahteen tai useampaan muistilohkoon ns. muistipankkien muodostamiseksi. Tällöin oheislaitteessa voidaan näistä muistilohkoista valita käyttöön yksi tai useampi mm. sen perusteella, mikä on oheislaitteelle 2 määritetty maksimitehonkulutusarvo. Suuremmilla tehonkulutusarvoilla voidaan tyypillisesti ottaa käyttöön useampia muistilohkoja kuin pienemmillä tehonkulutusarvoilla. Kuvassa 4 on esitetty eräs esimerkki tällaisen oheislaitteen rakenteesta. Kuvassa 4 esitetyssä oheislaitteessa 2 muistiin 14 on muodostettu neljä muistilohkoa 14a, 14b, 14c, 14d, mutta on selvää, että käytännön sovelluksissa muistipankkien lukumäärä voi olla keksinnön puitteissa myös muu kuin neljä. Muistilohkojen 14a—14d käyttöön ottamiseksi ja käytöstä poistamiseksi on edullisesti suorittimesta 13 muodostettu kytkentälinjat 18a—18d, joilla voidaan esim. kytkeä käyttöjännite haluttuihin muistilohkoihin 14a—14d, tai kytkentälinjoilla ohjataan kukin muistilohko 14a—14d joko aktiiviseen tilaan tai tehonsäästötilaan. Myös edellä esitetyllä menetelmällä voidaan oheislaitteen 2 tehonkulutusta säätää aikaisemmin tässä selityksessä esitettyjen tehonkulutuksen säätömenetelmien sijasta tai niiden lisäksi.

Elektroniikkalaitteessa 1 tehonsäätö voidaan suorittaa esimerkiksi siten, että elektroniikkalaitteessa 1 on teholähde, jonka lähtöjännitettä voidaan muuttaa. Tällöin elektroniikkalaitteessa 1 valitaan oheislaitteelle johdettavaksi käyttöjännitteeksi kulloistakin tehonkulutusta vastaava jännitearvo.

Keksinnön mukaista menetelmää voidaan soveltaa myös esimerkiksi erilaisten sisältöjen toteuttamisessa elektroniikkalaitteiden 1 yhteydessä käytettäväksi esim. seuraavasti. Oheislaitteena 2 voidaan käyttää muistikorttia, kuten MultiMediaCard™-standardin määritysten mukaista korttia, johon sisältöjä voidaan tallentaa. Sisällöillä tässä yhteydessä tarkoitetaan tietojoukkoja, sovellusohjelmia, elektronisia kirjoja, audiovisualista informaatiota, kuten musiikkia, videoita, jne. Esimerkiksi sisällön tuottaja tallentaa tällaisia sisältöjä muistikortille. Tällöin muistikortti 2 liitetään elektroniikkalaitteeseen, jossa on välineet sisällön siirtämiseksi muistikortille 2. Tällöin ennen tallennuksen aloittamista elektroniikkalaite ja muistikortti 2 suorittavat muistikortin tehonkulutuksen

asettamiseksi edullisesti toista maksimirajaa vastaavaan arvoon. Tämä on mahdollista, koska tällaisessa sisällön tallentamisessa käytettävässä elektroniikkalaitteessa 1 ei muistikortin tehonkulutuksella ole juurikaan merkitystä, vaan elektroniikkalaite 1 voi tuottaa riittävän tehon muistikortille 2. Tallennus voidaan tällöin suorittaa mahdollisimman suurella nopeudella, koska muistikortin kellotaajuus ja/tai väyläleveys saadaan asetettua suurimmaksi mahdolliseksi. Myös muistikortille 2 tallennetun sisällön varmistaminen mahdollisten tallennusvirheiden havaitsemiseksi voidaan myös suorittaa suurimmalla mahdollisella nopeudella. Suuri tallennus- ja/tai tarkistusnopeus aikaansaa sen, että elektroniikkalaitteella 1 saadaan sisältöjen tuotantonopeutta kasvatettua verrattuna tunnetun tekniikan mukaisiin menetelmiin.

Vastaavasti siinä vaiheessa kun muistikortille 2 tallennettua sisältöä halutaan käyttää jossakin elektroniikkalaitteessa 1, voidaan muistikortille 2 tehonkulutus asettaa sellaiseksi, joka elektroniikkalaitteen 1 kannalta on sopiva, esimerkiksi alin mahdollinen tehonkulutus. Tällöin keksinnön mukaista menetelmää sovellettaessa ei sisältöjen tuotantonopeutta tarvitse rajoittaa sen mukaan, mikä on sisällön käyttämisessä mahdollinen maksimi tehonkulutusarvo.

Koska keksinnön mukaisella menetelmällä voidaan suorittaa oheislaitteen tehonsäätö, voidaan oheislaite 2 liittää useisiin erilaisiin elektroniikkalaitteisiin. Joissakin elektroniikkalaitteissa on oheislaitteelle syötettävissä vain minimitehonkulutusta vastaava teho (jännite ja virta), jolloin elektroniikkalaitteessa 1 ei tarvita suurikokoista regulaattoria ja elektroniikkalaitteen kokoa ei tarvitse kasvattaa suurikokoisen regulaattorin tilantarpeen johdosta. Toisaalta kehitettävissä oheislaitteissa 2 ei tarvitse rajoittaa tehonkulutusta, koska elektroniikkalaite ja oheislaite voivat neuvotella sopivan tehonkulutusarvon. Tällöin jos oheislaite liitetään sellaiseen elektroniikkalaitteeseen, jossa oheislaitelliitäntään voidaan syöttää suhteellisen suuri teho, voidaan oheislaitetta käyttää mahdollisimman tehokkaasti (suurella kellotaajuudella/väyläleveydellä). Alustusvaiheessa tällainenkin oheislaite toimii pienemmällä tehonkulutuksella, kunnes sopiva tehonkulutuksen arvo on valittu. Keksinnön mukaisessa järjestelmässä voidaan varautua tulevaisuudessa kehitettävien mahdollisesti suurtakin tehoa vaativien oheislaitteiden käyttämi-

seen elektroniikkalaitteissa. Kuitenkaan ei kaikkien elektroniikkalaitteiden suunnittelussa tarvitse ottaa huomioon paljon tehoa kuluttavia kortteja.

On selvää, että tehonkulutuksen asettamisessa suoritettavat vaiheet voidaan toteuttaa muullakin tavalla kuin edellä esitetty sanomien muodossa tapahtuva kättely. Liitäntävälineissä 7, 10 voi olla esimerkiksi liitäntälinjoja, joita käyttämällä voidaan tehonkulutus asettaa oheislaitteelle. Lisäksi keksintöä voidaan soveltaa siten, että mainituille maksimirajoille on määritelty liellyjä vaihtoehtoisia (sallittuja) arvoja, jolloin kullakin oheislaitteella on ensimmäinen maksimiraja ja toinen maksimiraja valittu näiden vaihtoehtoisien rajojen joukosta.

Lisäksi mainittakoon, että oheislaitteen 2 ei tarvitse olla korttimuotoinen oheislaite, vaan oheislaitteena 2 voidaan käyttää muutakin laitetta, joka on liitettävissä elektroniikkalaitteeseen 1. Eräänä ei rajoittavana esimerkkinä tällaisesta oheislaitteesta mainittakoon kamera, joka liitetään esimerkiksi langattomaan viestimeen, tietokoneeseen, tms. Tällöin tehonkulutusta säätämällä voidaan vaikuttaa kameran toiminnallisiin ominaisuuksiin. Esimerkiksi pienemmällä tehonkulutuksella kameran kuvien päivitysnopeus elektroniikkalaitteen näytöllä voi olla pienempi kuin suuremmalla tehonkulutuksella. Tällöin elektroniikkalaite 1 voi asettaa oheislaitteena 2 käytettävän kameran tehonkulutuksen edullisesti sen perusteella, kuinka suuren tehon elektroniikkalaite 1 pystyy syöttämään oheislaitteelle. Keksinnön eräässä edullisessa suoritusmuodossa myös elektroniikkalaitteen 1 käyttäjä voi asettaa tehonkulutuksen maksimirajan, jolloin käyttäjä voi halutessaan esim. pienentää maksimirajaa kannettavan elektroniikkalaitteen käyttöajan pidentämiseksi.

On selvää, että nyt esillä olevaa keksintöä ei ole rajoitettu ainoastaan edellä esitettyihin suoritusmuotoihin, vaan sitä voidaan muunnella oheisten patenttivaatimusten puitteissa.

Patenttivaatimukset:

1. Menetelmä tehonkulutuksen määrittämiseksi elektroniikkalaitteessa (1), johon liitetään oheislaite (2), jolle teho syötetään elektroniikkalaitteesta (1), **tunnettu** siitä, että määritetään tehonkulutukselle ainakin ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo, ja että elektroniikkalaitteen (1) ja oheislaitteen (2) välillä suoritetaan oheislaitteen (2) tehonkulutuksen maksimin asettaminen arvoon, joka on olennaisesti mainittujen ensimmäisen ja toisen maksimiarvon välissä.

2. Patenttivaatimuksen 1 mukainen menetelmä, **tunnettu** siitä, että mainittua ensimmäistä maksimirajaa käytetään tehonkulutuksen oletusarvona, jolloin oheislaitteen (2) tehonkulutus asetetaan käynnistysvaiheessa korkeintaan olennaisesti samaksi kuin mainittu ensimmäinen maksimiraja.

3. Patenttivaatimuksen 1 tai 2 mukainen menetelmä, **tunnettu** siitä, että mainittua toista maksimirajaa käytetään tehonkulutuksen suurimpana sallittuna arvona.

4. Patenttivaatimuksen 1, 2 tai 3 mukainen menetelmä, **tunnettu** siitä, että elektroniikkalaitteen (1) ja oheislaitteen (2) välillä siirretään sanomia oheislaitteen tehonkulutuksen asettamiseksi johonkin arvoon olennaisesti mainittujen ensimmäisen maksimirajan ja toisen maksimirajan välissä.

5. Jonkin patenttivaatimuksen 1—4 mukainen menetelmä, **tunnettu** siitä, että oheislaitteelle (2) tallennetaan ainakin yksi sisältö käytettäväksi elektroniikkalaitteen (1) yhteydessä, jolloin sisällön tallennusvaiheessa oheislaitteen (2) tehonkulutukseksi asetetaan mainittua toista maksimirajaa vastaava arvo, ja sisällön käyttövaiheessa oheislaitteen (2) tehonkulutukseksi asetetaan mainittua ensimmäistä maksimirajaa vastaava arvo.

6. Jonkin patenttivaatimuksen 1—5 mukainen menetelmä, **tunnettu** siitä, että oheislaitteessa (2) muodostetaan ainakin yksi kellosignaali, ja

että oheislaitteen (2) tehonkulutuksen säätäminen suoritetaan mainitun ainakin yhden kellosignaalin taajuutta säätämällä.

7. Jonkin patenttivaatimuksen 1—6 mukainen menetelmä, **tunnettu** siitä, että oheislaitteessa (2) on ainakin yksi väylä, ja että oheislaitteen (2) tehonkulutuksen säätäminen suoritetaan oheislaitteen (2) väyläleveyttä säätämällä.

8. Jonkin patenttivaatimuksen 1-7 mukainen menetelmä, **tunnettu** siitä, että oheislaitteelle (2) on muodostettu kaksi tai useampia muistilohkoja (14a—14d), jolloin oheislaitteen (2) tehonkulutuksen säätäminen suoritetaan oheislaitteen (2) olennaisesti samanaikaisesti käsittelemien muistilohkojen (14a—14d) määrää säätämällä.

9. Järjestelmä, joka käsittää elektroniikkalaitteen (1), jossa on välineet (7) oheislaitteen (2) liittämiseksi ja välineet (8) tehon syöttämiseksi oheislaitteelle (2), ja joka järjestelmä käsittää välineet (7, 10, 14) tehonkulutuksen määrittämiseksi, **tunnettu** siitä, että tehonkulutukselle on määritetty ainakin ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo, ja että välineet tehonkulutuksen määrittämiseksi käsittävät välineet (3, 13, 16, 17) oheislaitteen (2) tehonkulutuksen maksimin asettamisen arvoon, joka on mainittujen ensimmäisen maksimiarvon ja toisen maksimiarvon välissä.

10. Patenttivaatimuksen 9 mukainen järjestelmä, **tunnettu** siitä, että se käsittää välineet (7, 10) sanomien siirtämiseksi elektroniikkalaitteen (1) ja oheislaitteen (2) välillä oheislaitteen tehonkulutuksen asettamiseksi johonkin arvoon olennaisesti mainittujen ensimmäisen maksimirajan ja toisen maksimirajan välissä.

11. Patenttivaatimuksen 9 tai 10 mukainen järjestelmä, **tunnettu** siitä, että oheislaitteessa (2) on välineet (16) ainakin yhden kellosignaalin muodostamiseksi, ja että järjestelmä käsittää välineet (7, 10, 13) oheislaitteen (2) tehonkulutuksen säätämiseksi mainitun ainakin yhden kellosignaalin taajuutta säätämällä.

12. Patenttivaatimuksen 9, 10 tai 11 mukainen järjestelmä, **tunnettu** siitä, että oheislaitteessa (2) on ainakin yksi väylä, ja että järjestelmä käsittää välineet (7, 10, 13) oheislaitteen (2) tehonkulutuksen säätämiseksi suoritetaan oheislaitteen (2) väyläleveyttä säätämällä.

13. Jonkin patenttivaatimuksen 9-12 mukainen järjestelmä, **tunnettu** siitä, että oheislaitteelle (2) on muodostettu kaksi tai useampia muistilohkoja (14a—14d), ja että välineet (7, 10, 13) oheislaitteen (2) tehonkulutuksen säätämiseksi käsittävät välineet (13, 18a—18d) oheislaitteen (2) olennaisesti samanaikaisesti käsittelemien muistilohkojen (14a—14d) määrän säätämiseksi.

14. Jonkin patenttivaatimuksen 9—13 mukainen järjestelmä, **tunnettu** siitä, että elektroniikkalaite (1) on kannettava elektroniikkalaite (1).

15. Patenttivaatimuksen 14 mukainen järjestelmä, **tunnettu** siitä, että se käsittää välineet (6) matkaviestintoimintojen suorittamiseksi.

16. Elektroniikkalaite (1), jossa on välineet (7) oheislaitteen (2) liittämiseksi ja välineet (8) tehon syöttämiseksi oheislaitteelle (2), ja välineet (7) tehonkulutuksen määrittämiseksi, **tunnettu** siitä, että tehonkulutukselle on määritetty ainakin ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo, ja että välineet tehonkulutuksen määrittämiseksi käsittävät välineet (3) oheislaitteen (2) tehonkulutuksen maksimin asettamisen arvoon, joka on mainittujen ensimmäisen maksimiarvon ja toisen maksimiarvon välissä.

17. Patenttivaatimuksen 16 mukainen elektroniikkalaite (1), **tunnettu** siitä, että se käsittää välineet (7) sanomien lähettämiseksi oheislaitteelta (2) ja vastaanottamiseksi oheislaitteelta (2) oheislaitteen tehonkulutuksen asettamiseksi johonkin arvoon olennaisesti mainittujen ensimmäisen maksimirajan ja toisen maksimirajan välissä.

18. Patenttivaatimuksen 16 tai 17 mukainen elektroniikkalaite (1), **tunnettu** siitä, että se on kannettava elektroniikkalaite (1).

19. Patenttivaatimuksen 18 mukainen elektroniikkalaite (1), **tunnettu** siitä, että se käsittää välineet matkaviestintoimintojen suorittamiseksi.

20. Oheislaite (2), jossa on välineet (10) oheislaitteen (2) liittämiseksi elektroniikkalaitteeseen (1), josta oheislaitteen (2) käyttämisessä tarvittava teho on järjestetty syötettäväksi oheislaitteelle (2), **tunnettu** siitä, että tehonkulutukselle on määritetty ainakin ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo, ja että oheislaite käsittää välineet (13, 16, 17) tehonkulutuksen maksimin asettamisen arvoon, joka on mainittujen ensimmäisen maksimiarvon ja toisen maksimiarvon välissä.

21. Patenttivaatimuksen 20 mukainen oheislaite (2), **tunnettu** siitä, että oheislaitteelle (2) on tallennettu ainakin yksi sisältö käytettäväksi elektroniikkalaitteen (1) yhteydessä.

22. Patenttivaatimuksen 20 tai 21 mukainen oheislaite (2), **tunnettu** siitä, että oheislaitteessa (2) on välineet (16) ainakin yhden kellosignaalin muodostamiseksi, ja välineet (13) oheislaitteen (2) tehonkulutuksen säätämiseksi mainitun ainakin yhden kellosignaalin taajuutta säätämällä.

23. Patenttivaatimuksen 20, 21 tai 22 mukainen oheislaite (2), **tunnettu** siitä, että oheislaitteessa (2) on ainakin yksi väylä, ja välineet (13) oheislaitteen (2) tehonkulutuksen säätämiseksi oheislaitteen (2) väyläleveyttä säätämällä.

24. Jonkin patenttivaatimuksen 20-23 mukainen oheislaite (2), **tunnettu** siitä, että oheislaitteelle (2) on muodostettu kaksi tai useampia muistilohkoja (14a—14d), ja että välineet (7, 10, 13) oheislaitteen (2) tehonkulutuksen säätämiseksi käsittävät välineet (13, 18a—18d) oheislaitteen (2) olennaisesti samanaikaisesti käsittelemien muistilohkojen (14a—14d) määrän säätämiseksi.

25. Jonkin patenttivaatimuksen 20—24 mukainen oheislaite (2), **tunnettu** siitä, että se on MultiMediaCard™ -oheislaite.

(57) Tiivistelmä

Nyt esillä oleva keksintö kohdistuu menetelmään ja järjestelmään tehonkulutuksen määrittämiseksi elektroniikkalaitteessa (1), johon liitetään oheislaite (2), jolle teho syötetään elektroniikkalaitteesta (1). Tehonkulutukselle määritetään ainakin ensimmäinen maksimiarvo ja ensimmäistä maksimiarvoa suurempi toinen maksimiarvo. Elektroniikkalaitteen (1) ja oheislaitteen (2) välillä suoritetaan oheislaitteen (2) tehonkulutuksen maksimin asettaminen arvoon, joka on olennaisesti mainittujen ensimmäisen ja toisen maksimiarvon välissä. Keksintö kohdistuu lisäksi elektroniikkalaitteeseen (1) ja oheislaitteeseen (2), joissa menetelmää sovelletaan.

Fig. 1

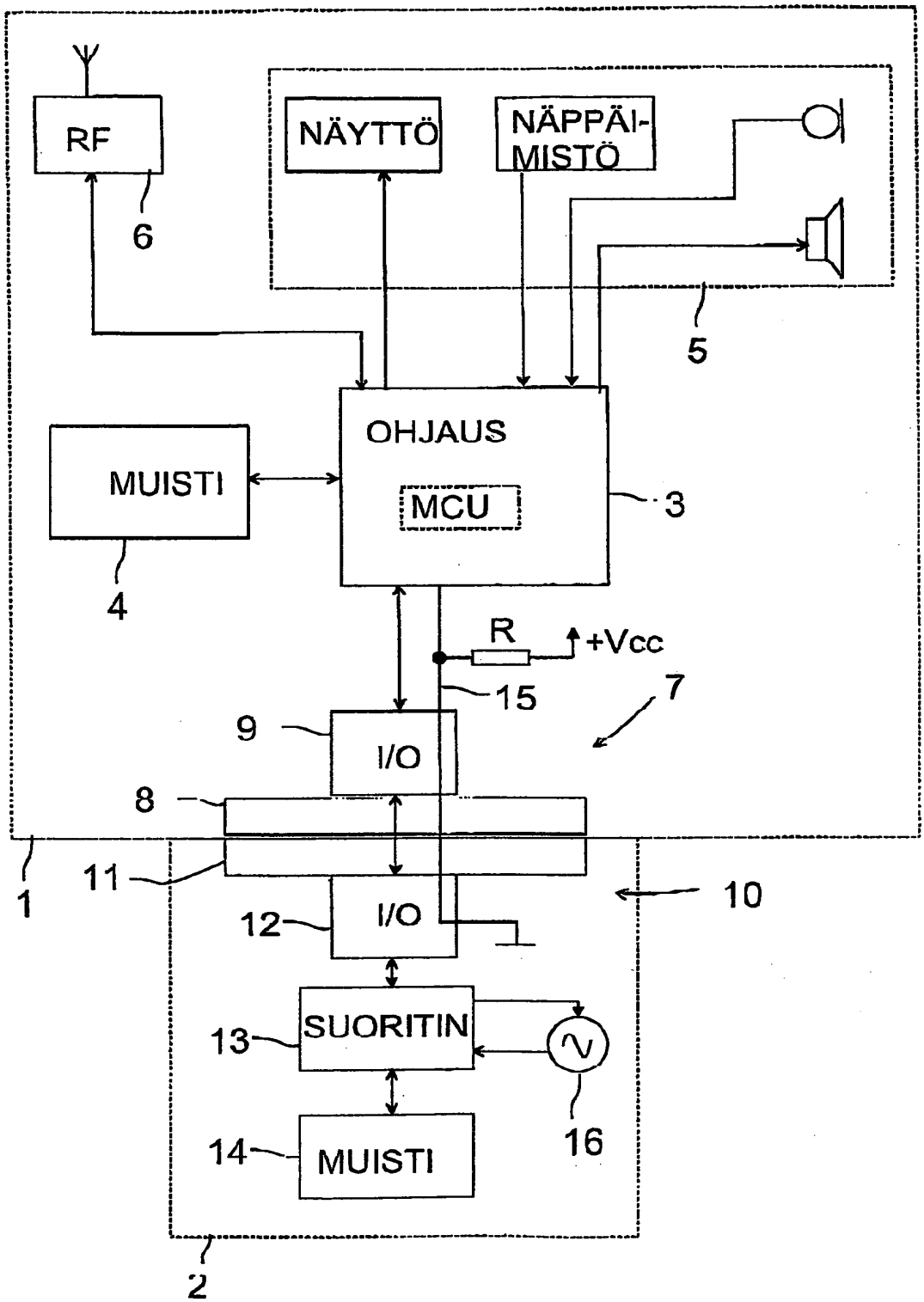


Fig 1

Kingston Exhibit 1004 - 113

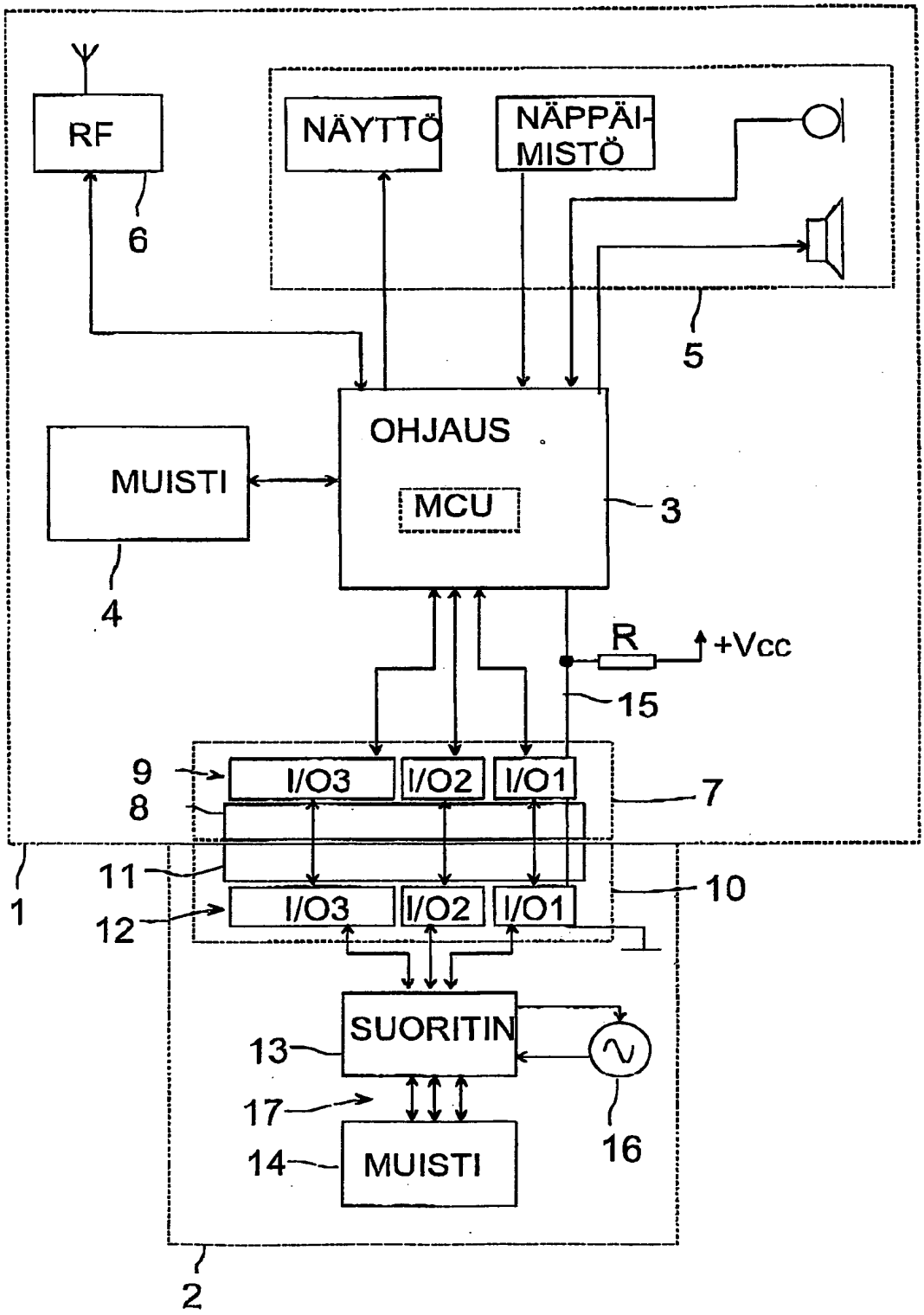
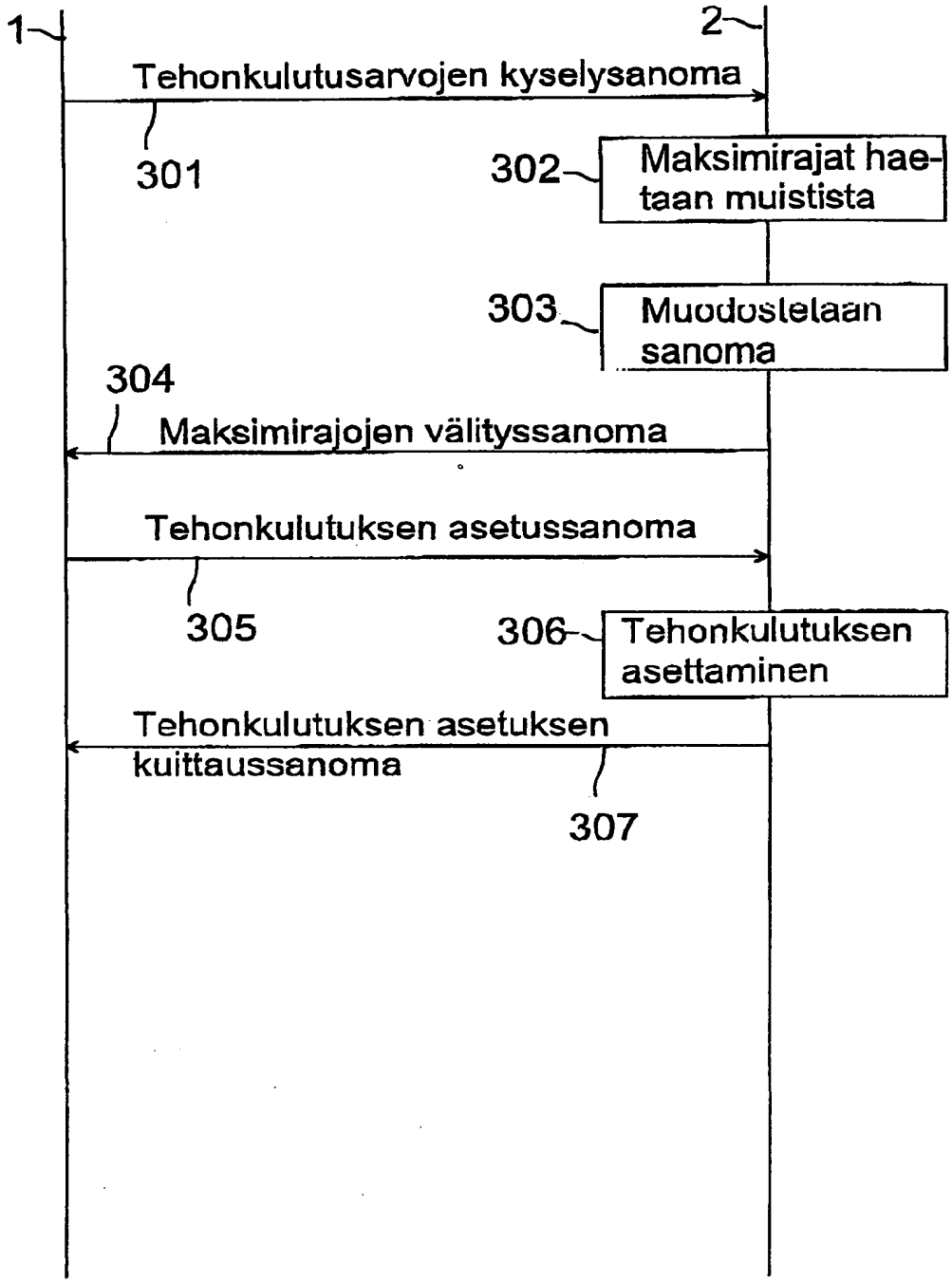

RF
6
NÄYTTÖ
NÄPPÄI-
MISTÖ
5
OHJAUS
MCU
3
MUISTI
4
R
+Vcc
15
9
8
I/O3
I/O2
I/O1
7
11
12
I/O3
I/O2
I/O1
10
1
SUORITIN
13
17
14
MUISTI
16
2

Fig 2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2
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303
Muodostelaan sanoma
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Tehonkulutuksen asetussanoma
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306
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Tehonkulutuksen asetuksen kuittaussanoma
307

Fig 3

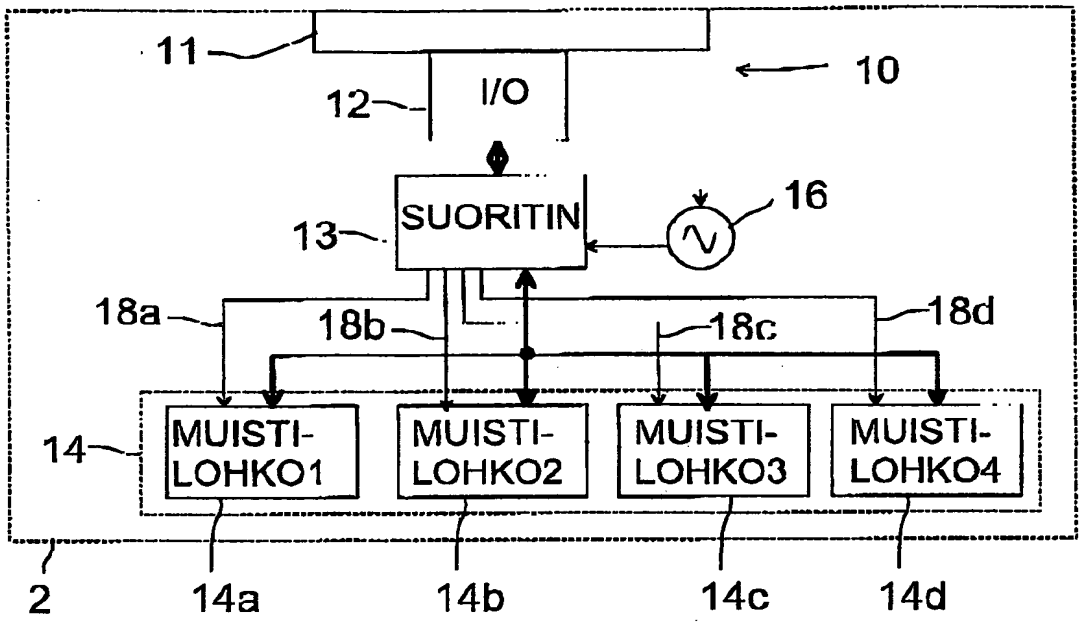

Fig 4

#2
6-19-03
cw

915-005.48

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of :

Kimmo Mylly :

Filed: Herewith :

For: A METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE

Assistant Commissioner for Patents
U.S. Patent and Trademark Office
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicant submits herewith references of which he is aware, which he believes may be material to the examination of this application and which he may have a duty to disclose in accordance with 37 CFR 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 CFR 1.56, it is not intended to constitute an admission that any document referred to herein is "prior art" for this invention unless specifically designated as such.

FILING OF PAPERS AND FEES BY "EXPRESS MAIL"
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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as "Express Mail" in an envelope with Mailing Label No. EV137073922US placed thereon prior to mailing and addressed to the U.S. Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202.

Margery B. Hood

Margery B. Hood
Dated: March 26, 2003

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement should not be construed to mean that a search has been made or that no other material information as defined under 37 CFR 1.56(a) exists.

Enclosed is a copy of the first Official Action with its English translation together with cited references.

Also enclosed is a Form PTO-1449 listing the cited references.

Respectfully submitted,

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FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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APPLICANT: K. Mylly	
FILING DATE: Herewith	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APROPRIATE
		5 6 0 6 7 0 4	2/25/97	Pierce et al			
		5 6 1 3 1 3 0	3/18/97	Teng et al			
		5 7 3 7 6 1 6	4/7/98	Watanabe			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		0 2 0 7 4 9 4	1/31/02	WO				

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

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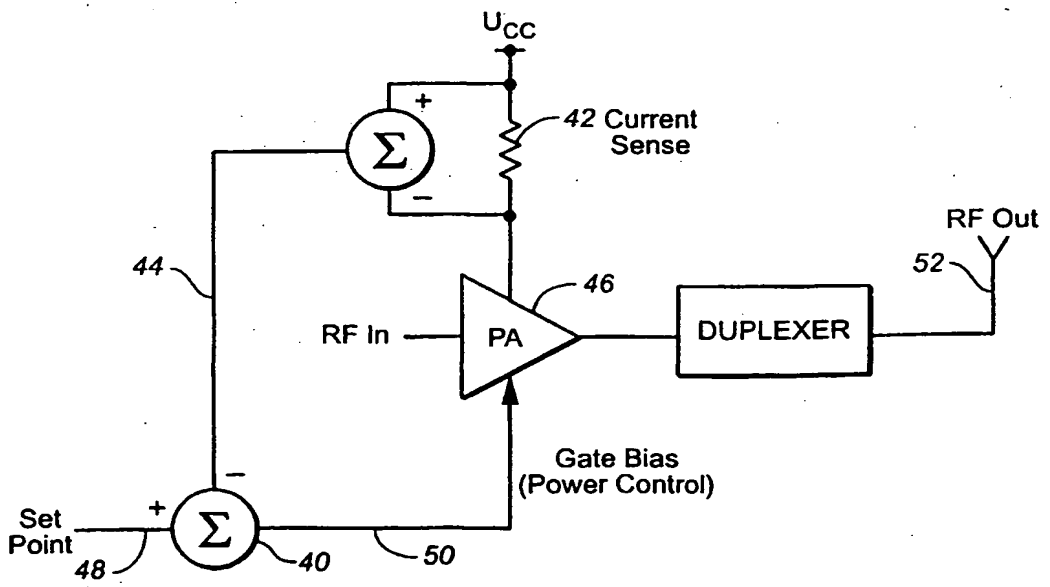
(54) Title: PERSONAL COMPUTER CARD RADIO MODEM USING NON-STANDARD POWER OUTPUT LEVEL



(57) Abstract: A hand-held, PCMCIA cellular radio modem card is described which uses a non-standard power output level. The non-standard power output is defined as the maximum RF power attainable such that the current drawn by the power amplifier does not exceed 400 mA. This definition permits the use of the wireless modem inside hand-held computing devices without the use of an additional battery pack extension.

WO 02/07494 A2

PERSONAL COMPUTER CARD RADIO MODEM USING NON-STANDARD POWER OUTPUT LEVEL

Background of the Invention

The present invention relates to personal computer (PC) card radio modems. Small hand-held personal computing devices can use Personal Computer Memory Card Interface Association (PCMCIA) radio modems to connect to a wireless network. PC card radio modems typically use battery power from the hand-held PC or from a battery pack extension.

A problem that exists in prior-art systems in which the wireless modem operates on a network such as the North American AMPS or CDPD network, is a battery pack extension is used to supplement the power supplied to the wireless modem. Typically, hand-held PCs use two AA batteries, which suffer from low capacity and a low peak current capability.

Six different standard RF power levels are required by the CDPD standard (CDPD R1.1 Part 409) and the AMPS standard (IS-19B) for a class III cellular device. With two AA batteries supplying the hand-held PC and the PCMCIA wireless card, it is difficult to achieve the highest RF power level; which, for a class III cellular device, is an output power of 28 dBm where 0 dBm is 1mW output power. Typically, prior art uses a battery pack extension on the PCMCIA card to achieve the highest RF power output. This is an undesirable solution as the esthetics of the complete product are poor.

It is desirable to have an improved system, which avoids some of the problems of the prior art.

Summary of the Invention

In one embodiment, the present invention relates to a PC card radio transceiver which uses a non-standard power output level. The non-standard power output level is limited by the peak sustainable current available from the battery inside the hand-held PC. In one embodiment, this current is limited to 600 mA. The non-standard RF power

obtainable, given a 600mA maximum limit, is typically between 24 dBm and 28 dBm (in one implementation, 26.5 dBm). The non-standard power output level has a nominal value less than the nominal value required by the standard, yet is still within the acceptable range (+2, -4dB) specified in the standard.

The advantage of the present invention is that the radio transceiver in the PC card can operate while attached to a hand-held PC without requiring a battery pack extension. The system allows the two AA batteries of the hand-held PC to produce an acceptable, high-level RF output power.

Implementation of a non-standard RF power level, which is based on a current restriction, requires the automatic leveling circuit (ALC) of the power amplifier to be a current leveling circuit as opposed to a power leveling circuit as in prior art systems. A current leveling circuit achieves the same effect as a power leveling circuit, given the load on the power amplifier remains constant. In practice, this is a reasonable assumption.

Brief Description of the Drawings

Fig. 1 is a block diagram illustrating a PCMCIA cellular modem attached to a hand-held PC.

Fig. 2 is a diagram illustrating the power amplifier, current leveling circuit, duplexer and antenna used in the PC card cellular radio transceiver of one embodiment of the present invention.

Fig. 3 is a diagram illustrating both the implemented and non-implemented standard power output levels as well as the non-standard power output level of one embodiment of the present invention.

Fig. 4 is a block diagram illustrating one embodiment of the current leveling system of the present invention.

Fig. 5 is a schematic illustrating one embodiment of the current leveling circuit for one embodiment of the present invention.

Detailed Description of the Preferred Embodiment

Fig. 1 is a block diagram that illustrates a hand-held personal computer 20 and PC card 22. In one embodiment, the PC card is a cellular modem with a built-in radio transceiver.

The hand-held PC 20 sends signals to be transmitted to the PC card cellular modem 22. Additionally, the hand-held PC supplies power for the operation of the PC card cellular modem 22. Typically, two AA batteries in the hand-held PC power both the hand-held PC and the PC card cellular modem 22. Since relatively small batteries are used, the maximum current which can be drawn by the PC card cellular modem 22 is limited to less than what is needed to meet the nominal output power requirements of IS-19B and CDPD Part 409 standards given present power amplifier and duplexer technologies. In one embodiment, the PC card cellular modem 22 should not draw more than 600 mA of current.

Fig. 2 is a simplified diagram of the elements in the PC card cellular modem of one embodiment of the present invention. A current leveling circuit 32 controls the current supplied to power amplifier 30 and hence indirectly controls the output power of amplifier 30. In a PC card cellular modem, the current supplied to the power amplifier makes up a large percentage of the total current consumed by the device. The output of the power amplifier 30 is sent to a duplexer 34, then out the antenna 36.

In the present invention, the current leveling circuit 32 limits the current used by the power amplifier 30 at the highest power output level. This highest power output level is the non-standard power output level described below.

In one embodiment, the current leveling circuit 32 limits the current drawn by the power amplifier 30 to 400 mA when it is transmitting at the highest output power level. The current consumption of the entire card is therefore limited to 600mA.

Fig. 3 illustrates the RF output levels for the standard and non-standard power outputs for CDPD standard R.1.1 Part 409 and AMPS standard IS-19B. There are six standard output power levels for a class III cellular device. The standard, nominal power

output levels range from 8 to 28 dBm in 4 dB steps. In one embodiment, the non-standard power output level is between the highest standard power level, which is not implemented (28 dBm), and the highest implemented power level (24 dBm). In one embodiment, by limiting the current draw by the power amplifier to 400 mA or less (the total PC card current draw to 600mA or less), the non-standard power output level is about 26.5 dBm. This level is below the nominal 28 dBm power level specified in the standard, yet still falls within the acceptable range of +2dB to –4dB from nominal specified in the standard.

Fig. 4 is a block diagram of a circuit to implement one embodiment of the present invention. A set point value 48 is sent to adder 40 and combined with a feedback value on line 44 from current-sensor 42 to produce a gate bias (power control) signal for power amplifier 46. The set point values are controlled by the micro-processor. Each set point value corresponds to a power output level for the power amplifier 46. The current leveling circuit limits the power output by the power amplifier. In a preferred embodiment, the maximum set point value is such that the current drawn by the power amplifier is less than 400 mA.

Fig. 5 illustrates details of one embodiment of the current leveling circuitry for operation with the PC card radio transceiver of the present invention.

Other modifications and implementations will occur to those skilled in the art, without departing from the spirit and scope of the present invention. Accordingly, the above description is not intended to limit the invention, which is to be limited only by the following claims.

Claims:

1. A PC radio card adapted to be connected to and powered by a hand-held personal computer, the PC radio card using a number of output power levels controlled by current supplied to power amplifier in the PC radio card, the output power levels including multiple implemented standard power output levels and a nonstandard battery-limited power output level, the nonstandard battery-limited power output level being greater than the multiple implemented standard power output levels but less than an unimplemented standard power output level.

2. The PC radio card of Claim 1 wherein the non-standard battery-limited power output level is such that the current drawn by the power amplifier is 400 mA or less.

3. The PC radio card of Claim 1 wherein the PC radio card includes a current control automatic leveling circuit, keeping the current supplied to the power amplifier less than 400 mA.

4. The PC radio card of Claim 1 wherein the PC radio card is powered by a hand-held personal computer using two AA batteries.

5. The PC radio card of Claim 1 wherein the non-standard battery-limited power output level is less than 28 dBm and more than 24 dBm, wherein an output of 0 dBm is calibrated to 1 mW of output power.

6. A PC radio card adapted to be connected to and powered by a hand held personal computer, the PC radio card using a number of output power levels set by current supplied to power amplifier in the PC radio card, the output power levels including multiple implemented standard power output levels and a nonstandard battery-

limited power output level, the nonstandard battery-limited power output level being such that the current drawn by the power amplifier is 400mA or less.

7. The PC radio card of Claim 6 wherein the non-standard battery-limited power output level is greater than the implemented standard but less than an unimplemented standard power output level.

8. The PC radio card of Claim 6 wherein the PC radio card is powered by a hand-held personal computer using two AA batteries.

9. The PC radio card of Claim 6 wherein the PC radio card has a current controlled automatic leveling circuit to limit the current supplied to the power amplifier.

10. The PC radio card of Claim 6 wherein the non-standard battery-limited power output level is less than 28 dBm and more than 24 dBm when 0 dBm is calibrated to one mW of output power.

11. A system including:

a battery-powered hand held personal computer; and

a PC radio card connected to and powered by the hand held personal computer, the PC radio card using a number of output power levels set by current supplied to power amplifier in the PC radio card, the output power levels including multiple implemented standard power output levels and a nonstandard battery-limited power output level, the nonstandard battery-limited power output level being greater than the multiple implemented standard power output levels but less than an unimplemented standard power output level.

12. The system of Claim 11 wherein the nonstandard battery-limited power level is such that the current drawn by the power amplifier is 400 mA or less.

13. The system of Claim 11 wherein the hand-held personal computer is powered two AA batteries

14. The system of Claim 11 wherein the nonstandard battery-limited power level limits the current supplied by the hand-held personal computer to the PC radio card to less than a given amount.

15. The system of Claim 11 further comprising a current controlled automatic leveling curcuit in the PC radio card to limit the current supplied to the power amplifier.

16. A PC card transceiver including:

an antenna;

an amplifier operably connected to the antenna:

a current controller operably connected to the amplifier to set the power output of the transceiver, the current controller adapted to produce a number of standard transceiver power output levels and a nonstandard transceiver output power level, the nonstandard transceiver output power level being such that the amplifier current is at a level that makes efficient use of the PC card transceiver batteries.

17. The PC card of Claim 16, further comprising a duplexer operatively positioned between the amplifier and the antenna.

18. The PC card of Claim 16 wherein the non-standard battery-limited power output level is greater than the implemented standard but less than an unimplemented standard power output level.

19. The PC card transceiver of Claim 16 wherein the amplifier is limited to 400 mA of current draw.

20. The PC card transceiver of Claim 16 wherein the PC card transceiver is adapted to be powered by a hand-held personal computer.

FIG._1

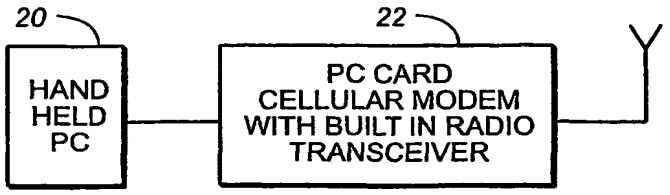
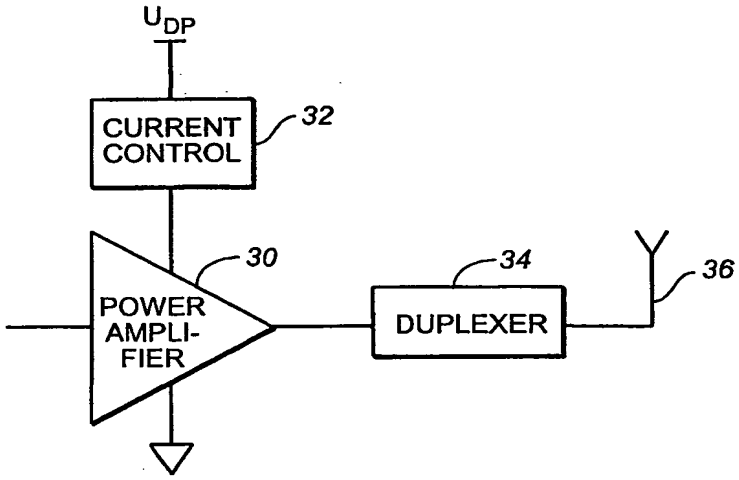


FIG._2



STANDARD POWER OUTPUT LEVELS		NON-STANDARD POWER OUTPUT LEVEL
Not Implememted	0 + 28 dBm 1 + 28 dBm 2 + 28 dBm	Maximun RF outpout power such that the power drawn by the PC card is less than 600mA. ~ 26.5 dBm
Implememted	3 + 24 dBm 4 + 20 dBm 5 + 16 dBm 6 + 12 dBm 7 + .8 dBm	

FIG._3

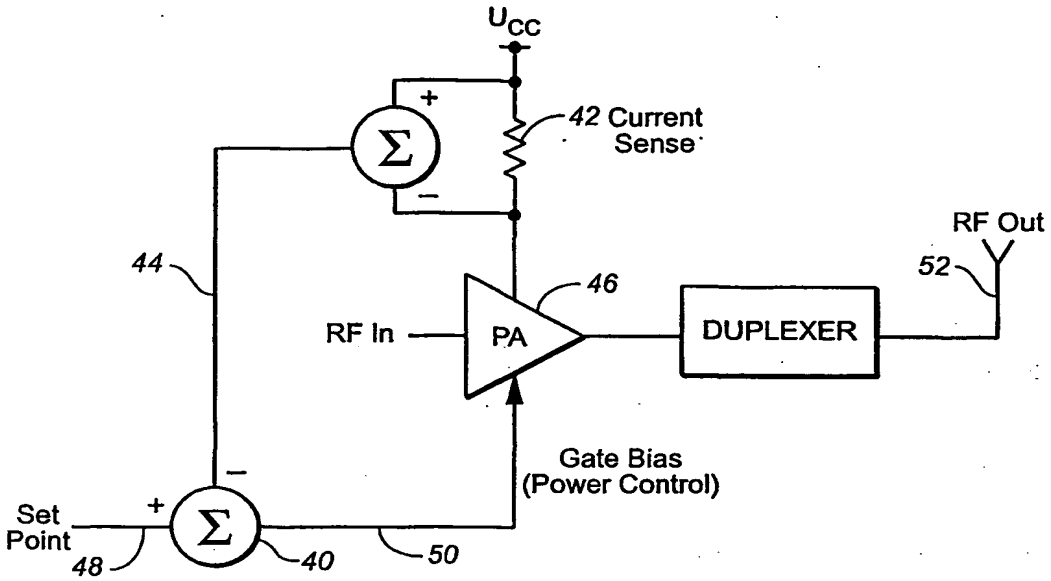

U_{CC}
+
Σ
−
42 Current Sense
RF Out
52
44
46
RF In
PA
DUPLEXER
Gate Bias (Power Control)
−
+
Set Point
48
Σ
40
50

FIG._4

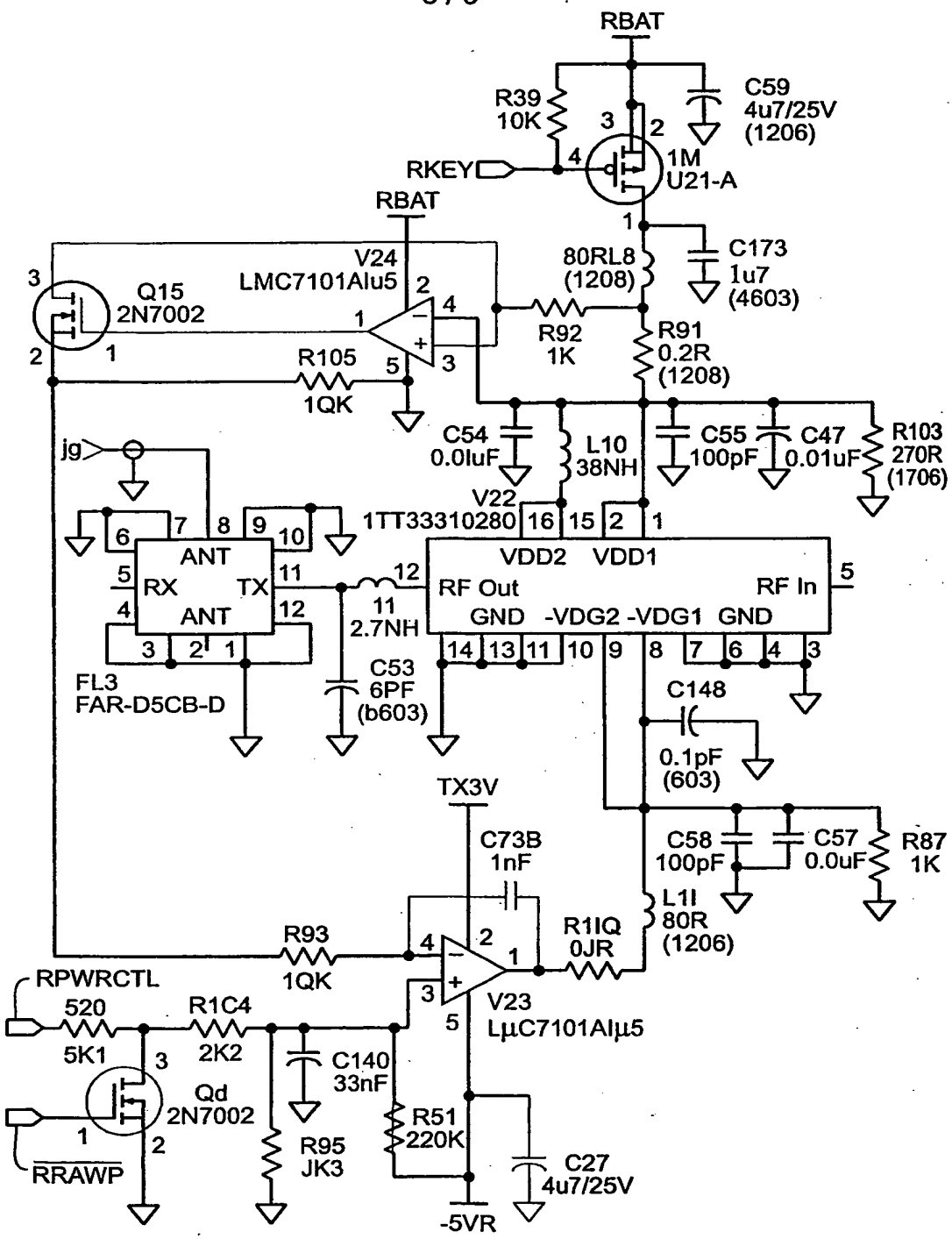


FIG._5 Schematic for Current Control ALC

2185 #4 SP

915-005.48 8-6-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of :

Kimmo Mylly :

Serial No. 10/401,338 :

Filed: March 26, 2003 : Group Art Unit: 2185

For: A METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE

Assistant Commissioner for Patents
U.S. Patent and Trademark Office
Washington, DC 20231

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Marilyn O'Connell

Marilyn O'Connell

July 24, 2003

Date

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement should not be construed to mean that a search has been made or that no other material information as defined under 37 CFR 1.56(a) exists.

The enclosed references have been cited in an International Search Report dated June 27, 2003 in a corresponding PCT application. A copy of the International Search Report is also enclosed for the convenience of the Examiner. Also enclosed is a Form PTO-1449 listing the cited references.

Respectfully submitted,

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Attorney for the Applicant
Registration No. 31,391

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July 15, 2003
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(37 CFR 1.98(b))

ATTY. DOCKET NO.	SERIAL NO.
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APPLICANT	
K. Mylly	
FILING DATE	GROUP
March 26, 2003	2185

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		4841440	6/20/89	Yonezu et al			
		5758108	5/26/98	Nakamura			
		5737616	4/7/98	Watanabe			
		5884086	3/16/99	Amoni et al			
		5758171	5/26/98	Ramamurthy et al			
		6178514	1/23/01	Wood			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		9841987	9/24/98	WO				
		2235797	3/13/91	GB				
		0207494	1/31/02	WO				

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)

EXAMINER	DATE CONSIDERED

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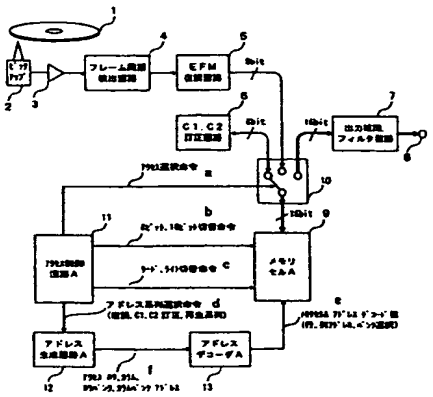
添付公開書類
国際調査報告書

(54)Title: **DEVICE AND METHOD FOR REPRODUCING DIGITAL SIGNAL USING VARIABLE BUS-WIDTH MEMORY AND DEVICE AND METHOD FOR RECORDING DIGITAL SIGNAL**

(54)発明の名称 バス幅可変メモリを用いたディジタル信号再生装置、再生方法及び記録装置、記録方法



2 ... pickup
4 ... frame synchronization detecting circuit
5 ... EFM demodulating circuit
6 ... C1 and C2 correcting circuit
7 ... output interpolation filter circuit
9 ... memory cell A
11 ... access control circuit A
12 ... address generating circuit A
13 ... address decoder A
a ... access selecting instruction
b ... 8 bit/16 bit switching instruction
c ... read/write switching instruction
d ... address sequence selecting instruction (demodulation, C1/C2 correction, and reproducing sequence)
e ... address decoding value of memory cell A (selection of row/column address and bank)
f ... access row/column, row/column bank address

(57) Abstract

Digital data are stored in a memory means in prescribed arranging order and, when a data arrangement to be corrected for an error contained in the arrangement or a data arrangement to be produced is read out, the control of the access to the memory means is made easier, the number of accesses to the memory means is reduced and a data transfer speed is increased to thereby reduce the power consumption when using a semiconductor chip containing the memory means. The memory means which can switch the access bit width between (n) bits and (n x m) bits (n and m: natural numbers), a bus width switching means which can switch the memory access bit width between the (n) and (n x m) bits, and a control means which controls the access are provided. Since the control means controls the access so that the bus width can be switched to the (n x m) bit width at the time of reading out the data arrangement to be reproduced from the memory means, the number of accesses is reduced and the transferring speed of reproduced data is improved. When the memory means which can be changed in access bit width, a means required for the execution of processing, etc., are provided on the same semiconductor chip, the memory means is customized so that the access bit width can be variably set in accordance with each required means.

（５７）要約

メモリ手段に対し、ディジタルデータを所定の配列順に記憶し、配列中の誤り訂正を行うデータ配列、再生データ配列の読み出しを行う際に、メモリ手段へのアクセス制御を容易に、アクセス回数の減少を実現すると共に、データの転送速度の向上を実現し、メモリ手段を含む半導体チップで実現した際の消費電力低減を実現する。

アクセスビット幅をｎビット、ｎ×ｍビット（ｎ、ｍは自然数）と切替可能なメモリ手段を設け、メモリ手段に対してアクセスビット幅をｎビット、ｎ×ｍビットと切替え可能なバス幅切替手段と、アクセスを制御する制御手段を設け、制御手段は再生データ配列をメモリ手段から読みだす際には、ｎ×ｍビット幅のバス幅とするように制御することによりアクセス回数が減少、再生データの転送速度が向上する。

また、アクセスビット幅可変なメモリ手段と処理の実行に必要な手段等を同一の半導体チップに設ける際、メモリ手段は必要なそれぞれの手段に応じてアクセスビット幅を可変に設定できるようにカスタマイズされる。

明 細 書

バス幅可変メモリを用いたディジタル信号再生装置、再生方法及び記録装置、記録方法

技術分野

本発明はディジタル信号再生装置、再生方法及び記録装置、記録方法に関し、特に一時的にデータを記憶するメモリ手段に対するアクセスにより、ディジタル信号を所定の配列にならべ、ならべられた配列に対し、誤り訂正等所定の処理を実行するためのデータ系列の読み出し、及び所定の処理が終了したデータ系列の読み出しを行うことで、ディジタル信号に対する再生処理、或は記録処理を行うディジタル信号再生装置、再生方法及び記録装置、記録方法に関する。

背景技術

従来、この類のディジタル信号再生装置、再生方法の一例としてＣＤ（Compact Disc）が挙げられる。このＣＤは、「ＣＤ－オーディオからパソコンへ－ 真利藤雄 監修、林 謙二編著 コロナ社 ｐ１３～ｐ１４」に記載の技術のように、標本化された１６ビットオーディオデータに対し、上位、下位それぞれ８ビット（１シンボル）単位に分割し複数のシンボルデータで１フレームを構成した後、誤り訂正符号としてＣ２訂正符号付加、フレーム間でのインターリーブ、Ｃ１訂正符号付加、サブコード付加を行った後、１シンボル８ビット単位のデータを１４ビット単位のデータに変調するＥＦＭ（Eight to Fourteen Modulation）と呼ばれる変調が行われ、ディスクへの記録周波数を下げる為のマージン３ビットを付加する。最後にマージンビットを含む合計１７ビット単位のデ

ータを複数集めた物に対して同期信号を付加した後の信号をディスクに記録する。

再生の際にはディスクから読み取られた信号に対し、上記とは逆の順番で復調処理、Ｃ１、Ｃ２訂正符号の復号による誤り訂正処理、デインターリーブ処理を実行することにより元のオーディオデータに対する再生データが得られる。

再生装置におけるメモリ手段に対してはシンボル単位のアクセスを行い、復調データの書込み、誤り訂正を行う対象の復調データの読み出し、時系列的に連続した順番で再生データの読み出しを行う事により再生が行われる。

上記した従来技術は、再生データを得る為に、誤り訂正等所定の処理を行う論理回路と、データを一時的に記憶し読み書きが自由なメモリ（ＲＡＭ：Random Access Memory）が用いられる。この場合メモリに対しては、復調データ系列のフレーム書込み、Ｃ１訂正系列のフレーム読み出し、Ｃ２訂正系列のフレーム読み出し、再生データ系列のフレーム読み出しと、所定の各処理に応じたシンボル単位のメモリアクセスが必要である。

メモリアクセス時には、インターリーブ遅延を考慮して処理対象のデータ系列にアクセスしなければならず、メモリに対するアドレス制御、管理が複雑となり、アドレス制御を行う論理回路が複雑となる問題が有る。

また、メモリに対する全てのアクセスはシンボル単位で行われる為、全てのアクセスに対するメモリアドレスを指定しなければならずメモリアクセス回数が増加するという問題がある。

この場合、特に高速で論理回路とメモリが動作する場合の消費電力が大きくなるという問題、メモリアクセス回数増加の為、本来メモリが持

つアクセス性能を活かせなくなり、再生データを読み出す際のデータ転送レートが低下するという問題が有る。

更に上記した論理回路とメモリを同一の半導体チップ上に設けた場合も同様の問題が生ずる。

また、最近は大規模、安価で一定時間間隔でリフレッシュが必要なＤＲＡＭ（Dynamic Random Access Memory）を大規模な論理回路と共に同一の半導体チップ上に混載可能な半導体技術が開発された。このＤＲＡＭ混載技術を用いて上記した処理を論理回路とＤＲＡＭで実現した場合、アクセス回数を減少させないと、特に高速動作時の半導体チップ全体の消費電力が大きくなるという問題が有る。

一方、近年開発が進んでいるＤＶＤにおいて、そのディジタル信号処理は、大容量のメモリと大規模な論理回路が必要である。大容量メモリの点でＤＲＡＭが有利であり、高速でこの大容量メモリにアクセスしディジタル信号処理を行うためには、上記したＤＲＡＭ混載技術でＤＲＡＭと論理回路を同一の半導体チップ上に設けて実現する事が必須となる。この場合もメモリアクセス回数、高速動作の点で半導体チップ全体の消費電力の問題が顕著に現れる。

従って本発明の目的は、メモリにアクセスする際のアドレスを容易に制御でき、かつメモリアクセス回数を減少させると共に、転送データの転送速度を向上させる事が可能なディジタル信号再生装置、再生方法及び記録装置、記録方法を提供するものであり、同一の半導体チップ上に処理手段とメモリとを設けた際に、半導体チップ全体の消費電力の低減を実現すると共に、ディジタル信号処理を高速で処理し、データの高速転送を実現する半導体チップ上のディジタル信号処理システムを提供するものである。

発明の開示

上記問題を解決するための、少なくとも、記録媒体からの読取り信号を復調し、復調データをｎビット単位で出力する復調処理手段と、誤り訂正処理に対するデータ配列に対し、ｎビット単位で処理を行う誤り訂正処理手段と、再生データのデータ配列に対し、ｎ×ｍビット単位で処理を行う出力処理手段と、メモリ手段のデータバスに対し、上記手段のデータバスを選択的に接続する接続手段と、上記各処理手段それぞれの処理に必要なデータ配列のアクセスに必要なアドレスを生成する手段と、生成されたアドレスをメモリ手段上の実際のアドレスにデコードする手段と、メモリ手段、接続手段、アドレス生成手段に対する制御命令を生成する手段とを有し、メモリ手段は、アクセスビット幅がｎビットとｎ×ｍビットに切替えてアクセス可能なバス幅可変手段を有し、メモリ手段にアクセスを行う制御手段を設け、その制御手段は、上記ｎ×ｍビット単位で出力処理手段への転送データの読み出しを行う際に、ｎ×ｍビットのバス幅とすることで行う。

これにより、メモリのアクセス回数を減少させると共に、データの転送速度の向上が図れる。

また、これらアクセスビット幅が可変なメモリ手段と、接続手段、メモリの制御手段、処理手段を同一の半導体チップ上に設ける際には、可変なアクセスビット幅の種類（ｎビット幅とｎ×ｍビット幅）に対応したアクセスビット幅のカスタマイズが行われ、アクセスビット幅を可変に設定できるメモリ手段が半導体チップ上に設けられ、大容量のメモリ手段が半導体チップ上に必要な場合は一定時間でリフレッシュ動作の必要なダイナミックなメモリをメモリ手段として用いる。

ＤＲＡＭ混載技術により、論理回路及び同一の半導体チップ上に設けられるメモリは、ディジタル処理を行うのに必要なアクセスビット幅及

び記憶容量に応じて自由に構成することが可能となる。すなわち、所定の処理に必要なそれぞれの論理回路を処理効率の点から有利なように構成でき、それぞれの論理回路で必要なアクセスビット幅に合せてアクセスが可能なメモリが構成できるようになる。

図面の簡単な説明

第１図は、本発明による第１の実施形態の構成を示すブロック図である。

第２図は、第１図の実施形態におけるメモリセルＡのアクセス制御の過程を示すフローチャートである。

第３図は、出力補間、フィルタ処理までに必要な各処理のアクセス系列、メモリセルＡのアドレス制御方法を示す図である。

第４図は、８ビット、１６ビットとアクセスビット幅が可変なメモリセルＡの一構成例を示すブロック図である。

第５図は、第１図に示した実施形態における光ディスク１に記録されるデータのフレーム構造を示す図である。

第６図は、第１図に示した実施形態におけるで光ディスク１からの復調後のシンボルデータに対し、各処理におけるフレーム間遅延を示す図である。

第７図は、本発明による第２の実施形態の構成を示すブロック図である。

第８図は、第７図の実施形態におけるメモリセルＢのアクセス制御の過程を示すフローチャートである。

第９図は、第７図に示した実施形態でメモリセルＡから読みだされたデータで構成される１セクタの構成を示す図である。

第１０図は、第７図に示した実施形態で、インターフェイス回路への

データ転送までに必要な各処理のアクセス系列、メモリセルBのアドレス制御方法を示す図である。

第１１図は、本発明による第３の実施形態の構成を示すブロック図である。

第１２図は、８、３２ビットとアクセスビット幅が可変なメモリセルCの一構成例を示すブロック図である。

第１３図は、第１１図に示した実施形態で、インターフェイス回路へのデータ転送までに必要な各処理のアクセス系列、メモリセルCのアドレス制御方法を示す図である。

第１４図は、第１１図の実施形態におけるメモリセルCのアクセス制御の過程を示すフローチャートである。

第１５図は、本発明による第４の実施形態の構成を示すブロック図である。

第１６図は、第１５図の実施形態におけるメモリセルCのアクセス制御の過程を示すフローチャートである。

第１７図は、本発明の第５の実施形態の構成を示すブロック図である。

発明を実施するための最良の形態

以下、本発明の実施の形態を図面を用いて説明する。

第１図は本発明の第１の実施形態に関る再生装置及び再生方法の構成を示すブロック図である。同図において、参照数字１は記録する１６ビットディジタルオーディオ信号に対し、所定のフォーマットでエンコードを行ったディジタル信号を記録した光ディスク、２は光ディスク１に記録された信号を読み取るピックアップ、３はプリアンプ、４は光ディスク１から読みだされた信号より構成されるフレームの先頭を示す同期信号の検出を行うフレーム同期検出回路、５は変調されて記録された光

ディスク１からの読み出し信号を元の８ビット、１シンボル単位のデータに復調するＥＦＭ復調回路、６はディスク読み出し時に発生したエラーに対し信号中に付加された訂正符号の復号を行い信号内に存在するシンボル単位のエラー訂正を行うＣ１，Ｃ２訂正回路、７は１６ビット、２シンボル単位で処理を行い、訂正不能と判断された際には再生データの補間を実行、フィルタ処理を行う出力補間、フィルタ回路、８は出力端子、９はアクセスビット幅を８ビット、１６ビットと可変にアクセスでき、８ビット単位でアクセスするメモリバンクを２面持つメモリセルＡ、１０はメモリセルＡにアクセスする対象を制御し、８ビットアクセスの場合は、メモリセルＡの１６ビットデータバスの下位８ビットとアクセスする対象の８ビットデータバスをダイレクトに接続し、１６ビットアクセスの場合はメモリセルＡの１６ビットデータバスをそのままダイレクトに接続するセレクタＡ、１１はメモリセルＡのアクセス対象の選択を制御するアクセス選択命令、メモリのリード、ライト切替命令、８ビット、１６ビット切替命令、メモリセルＡにアクセスする際のアドレス系列（復調系、Ｃ１、Ｃ２訂正系、再生系）選択命令をそれぞれ生成するアクセス制御回路Ａ、１２はアドレス系列選択命令に従い、アクセスを行うアドレスを生成するアドレス生成回路Ａ、１３は生成されたアドレスをメモリセルＡのアドレスにデコードするアドレスデコーダＡである。

第１図において、光ディスク１に記録されている再生されるべきディジタルオーディオ信号がピックアップ２から読みだされ、読みだされた信号中に含まれるフレーム同期信号検出を４のフレーム同期検出回路４で行う。

ここで第５図により光ディスク１に記憶されるディジタル信号の処理単位であるフレームの構造、第６図により再生データを得る為に必要な

処理について説明する。

第５図に示すように、光ディスク１に記録する単位であるフレーム５０１の構成は、フレームの先頭を示す同期信号５０２と、そのフレームについての再生時間情報などを記録したサブコード５０３、フレームデータ５０４により構成される。フレーム同期信号の検出、ＥＦＭ復調処理を行った後のサブコード、フレームデータは８ビットを１シンボルとした単位で構成され、フレームデータはデータ２４シンボル、Ｃ１、Ｃ２訂正符号各４シンボル、合計３２シンボルで構成される。元のオーディオ再生データを得る為には第６図に示すように復調処理を行ったフレームに対して、フレーム番号順に複数ならべたフレーム系列に対し（図中６０１）、Ｃ１訂正は奇数番号のシンボルデータを１フレーム分遅延した図中６０２に示す様なフレーム系列に対して行う。Ｃ２訂正はシンボル毎に４フレーム遅延が増加、最大１０８フレーム遅延までのフレーム系列（図中６０３）の３２－４＝２８シンボルに対して行い、再生データはＣ２訂正を終了したフレーム系列内の０～１１までのシンボル番号の系列６０４と、２フレーム分遅延したＣ２訂正フレーム系列内の１６～２７までのシンボル番号の系列６０５からなる。

以上のような各系列のフレームデータに対する各処理を第１図で行い、出力補間、フィルタ回路７への再生データ読み出しを２シンボル（１ワード）単位で容易に行う為のシンボルデータの配置、及びメモリアドレス制御の方法を第３図を用いて説明する。

第３図において、３０４、３０５は再生データの読み出し制御を容易にかつ、アクセス単位を１ワードとする事が可能なシンボル単位のデータの配置例であり、３０４は第（ｎ－３）フレーム目の０～１１シンボル目までの再生データ系列、３０５は第（ｎ－３）フレーム目の１６～２７シンボル目までの再生データ系列である。このような配置で再生デ

ータ系列を構成しようとすると、Ｃ２訂正系列は第６図で説明したＣ２訂正系列６０３と再生系列６０４、６０５で示した関係のフレーム遅延で与えられるので、再生データ系列中の０～１５シンボルと、２フレーム遅延した再生データ系列の１６～２７シンボルとなる。従ってこの場合の再生系列に対するＣ２訂正系列は、３０３の様に１列に並ぶ配置になる(第３図中、３０３は第(ｎ－１)フレーム目のＣ２訂正系列を示す)。Ｃ２訂正系列はＣ１訂正系列に対し最大フレーム遅延１０８フレームで、１シンボル毎に４フレーム遅延が増加するので、３０３のＣ２訂正系列に対し、Ｃ１訂正系列は３０２の様な配置になる。(図中３０２は(ｎ－１)フレーム目のＣ１訂正系列を示す)。更にＣ１訂正系列は、復調系列に対して奇数シンボル番号が１フレーム遅延されるので、復調系列は３０１の様な配置になる(図中３０１はｎフレーム目の復調系列を示す)。以上の各系列のシンボル配置をメモリでアクセス際のアドレス制御方法は、アドレス制御を容易に行う為、例えば横方向に１６シンボル、縦方向に４個の６４バイトをアドレス制御の１単位、１バンクとし(図中３０６)アドレス制御の際の基本単位としている。３０７は１バンクの縦方向のアドレスを示すカラムアドレス、３０８は横方向のアドレスを示すロウアドレスである。更にバンク単位のアドレス制御を行う為、カラムバンクアドレス３０９、ロウバンクアドレス３１０が与えられる。アクセスする際にはロウバンク、カラムバンクアドレスと、バンク内のロウ、カラムアドレスを指定してアドレス制御を行い、再生データ系の読み出しの際には、２シンボル構成のワード単位の最初のシンボルに対するアドレスを指定して、１ワード単位のアクセスを行う(図中３１１)。

第３図で説明したアドレス制御方法を用い、第１図の再生装置において再生データを得るまでの処理の流れを第２図のフローチャートを併せて用いて説明する。

第１図において、アクセス開始命令に従い光ディスク１から信号の読み出しが開始されると、１１のアクセス制御回路Ａは、１０のセレクタＡ、９のメモリセルＡ、１２のアドレス生成回路Ａそれぞれの制御対象に対し各制御命令を生成する。１０のセレクタＡはアクセス選択命令に従い５のＥＦＭ復調回路からの８ビットデータバスとメモリセルＡの１６ビットデータバスの下位８ビットに接続、９のメモリセルＡは８ビット、１６ビット切替命令に従い、シンボル単位の復調データをライトする為、アクセスビット幅を８ビットに設定、リード、ライト切替命令に従いライトを選択し、１２のアドレス生成回路Ａはアドレス系列選択命令に従い、復調系列のアドレスを生成するように設定される（ステップ２０１）。メモリセルＡへのアクセス準備が完了するとＥＦＭ復調処理が開始され、１２のアドレス生成回路Ａは第３図で説明したアドレスの指定方法に従い、復調系列のロウ、カラムアドレス、ロウバンク、カラムバンクアドレスを１シンボルライト毎に生成、１３のアドレスデコーダＡでメモリセルＡのアドレスにデコードされ１シンボル毎にメモリセルＡにライトされる（ステップ２０３）。

ここでアクセスビット幅が８、１６ビットと可変な１０のメモリセルＡについて説明する。第４図はメモリセルＡの構成例で、８ビット単位でアクセス可能な２つのメモリバンク４０１と４０２を持ち、行方向、列方向のアドレスを指定する事でメモリバンクへのアクセスが可能となっている。４０３はバンク切替用のセレクタでバンク選択信号に従い８ビット単位アクセスのメモリバンク選択が可能である。４０４は８ビット、１６ビット切替命令に従い、メモリバンク１の８ビットバスを上位８ビット、メモリバンク２の８ビットバスを下位８ビット、合計１６ビットデータをして扱う場合と、セレクタ４０３で選択されたメモリバンク１または２の８ビットデータを下位８ビットとし、リード時、上位８

ビットのデータとして“0”を加え16ビットデータとした物の選択を行うセレクタである。405はリード、ライト切替命令に従い、データの転送方向を決定するI／Oバッファである。このような構成でメモリセルAは構成され、アクセスビット幅の切替が可能になる。なお、物理的にバスを切り替える変わりに、物理的にはすべてのバスが接続されているがその時に使用するバス幅分のバスのみを有効にする構成としても構わない。

C2訂正可能な復調フレームのライトが終了したと判断されると（ステップ204）、アクセス制御回路Aは各制御対象に対しC1訂正系列のフレームをメモリセルAからリードする為の命令を生成する。セレクタAはC1、C2訂正回路にC1訂正系列のシンボルデータをリード可能な様にC1、C2訂正回路への8ビットデータバスとメモリセルAの16ビットデータバスの下位8ビットを接続、メモリセルAはリードを選択、アドレス生成回路AはC1訂正系列のアドレスを生成するように設定される（ステップ205）。C1訂正処理の為のメモリアクセス選択が終了すると、アドレス生成回路AはC1訂正系列のロウ、カラム、ロウバンク、カラムバンクアドレスを1シンボルリード毎に生成、アドレスデコーダAでメモリセルAのアドレスにデコードされ1シンボル毎にC1訂正系列データがメモリセルAからリードされ（ステップ206）、リードされたC1訂正系列のフレームに対して系列中に発生したエラーの訂正が実行される（ステップ207）。

C1訂正系列の処理が終了すると、アクセス制御回路Aは各制御対象に対してC2訂正系列のフレームをメモリセルAからリードする為の命令を生成する。アドレス生成回路AはC2訂正系列のアドレスを生成するように設定され（ステップ208）、C2訂正系列のロウ、カラム、ロウバンク、カラムバンクアドレスを1シンボルリード毎に生成、アド

レスデコーダＡでメモリセルＡのアドレスにデコードされ１シンボル毎にＣ２訂正系列データがメモリセルＡからリードされ（ステップ２０９）、リードされたＣ２訂正系列のフレームに対して系列中に発生したエラーの訂正が実行される（ステップ２１０）。

Ｃ２訂正系列の処理が終了すると、アクセス制御回路Ａは各制御対象に対して再生データ系列を１ワード（２シンボル）単位でメモリセルＡからリードする為の命令を生成する。セレクタＡは１ワード単位で処理を行う出力補間、フィルタ回路７への１６ビットデータバスとメモリセルＡの１６ビットデータバスを接続、出力補間、フィルタ回路７への１ワード単位のデータ転送を可能にし、メモリセルＡはアクセスビット幅を１６ビットに選択、アドレス生成回路Ａは再生データ系列のアドレスを生成するように設定（ステップ２１１）、リードの単位である２シンボルデータの中で最初にアクセスを行うのロウ、カラム、ロウバンク、カラムバンクアドレスを１ワードリード毎に生成し、アドレスデコーダＡでメモリセルＡのアドレスにデコードし再生データをリードする（ステップ２１２）。リードされた再生データは７の出力補間、フィルタ回路において、訂正不能の場合は補間処理が行われ、フィルタ処理後、出力端子８より出力される。再生を継続する場合には、ステップ２０１から処理を再開する（ステップ２１３）。

第１の実施形態の例において、光ディスク１から読み取られ、ディジタル化されたシリアルデータに対する復調方法が、シリアルデータに同期して送られてくるビットクロック１７個分のシリアルデータ（復調データ１４ビットとマージン３ビット単位でシリアル転送される）から８ビット単位のパラレルデータにＥＦＭ復調回路で変換される場合、シリアルデータの転送回数を示すビットクロック数と、出力補間、フィルタ回路へ１６ビット単位でデータ転送を行う際のメモリのアクセス回数と

の関係は、アクセスビット幅可変なメモリを用いた場合、誤り訂正符号等の冗長分を考慮し冗長度が１００％とすると、ビットクロック(１７＋１７)個に対して、８ビットで書き込まれたメモリから１６ビットのデータ量のデータ転送が１回で行われるので３４：１となり、また、冗長度が０の場合１７：１の関係となる。よって、一般的に冗長度は１００％より小、０％より大であるので、ビットクロック周波数１に対して、出力転送周波数Ｆｏは１／３４＜Ｆｏ＜１／１７となる。

これに対して、出力補間、フィルタ回路へのデータ転送が１回につき８ビット単位であれば、同じ１６ビットのデータ量を転送するのに２回の転送が必要となり、上記と同様の条件の場合、ビットクロック周波数１に対して、出力転送周波数Ｆｏは１／６８＜Ｆｏ＜１／３４となり、アクセスビット幅可変なメモリを用いた場合よりもデータの転送効率が低下する。

以上のように本発明の第１の実施の形態においては、光ディスクから読みだされた信号に対し同期信号の検出、復調処理後のシンボル単位のデータ書込みから、再生データの読み出しを行うまでの処理に対するアドレス制御を、まとまった複数シンボル単位で１バンクを構成、１バンク中のロウ、カラムアドレスと、バンクに対するロウ、カラムアドレスを指定してアクセス制御を行う事によりアドレス制御が容易となる。

また、アドレス制御を行う際の再生データ系列の配置を工夫する事により、２シンボル単位でアクセス、データリードが可能となり、再生データに対する出力処理を２シンボル単位で行う事ができる。

また、再生データ系列の読み出しの際のメモリセルＡのアクセスビット幅を１６ビット、リード単位を１ワード単位で行える為、メモリアクセス回数が減少し、再生装置全体の消費電力低減につながる。

また、以上説明した再生処理に必要なメモリセルＡ、各処理回路、制

御回路を同一の半導体チップ上に設けた場合でもメモリアクセス回数が減少し、半導体チップ全体の消費電力低減につながる。

第７図は本発明による再生装置及び再生方法の第２の実施の形態を示すブロック図であって、参照数字１はホストコンピュータで処理を行うディジタルデータが記録された光ディスク、１４はメモリセルＡから１ワード単位でリードされた再生データで構成されるセクタの先頭を検出するセクタ同期信号検出回路、１５は１セクタ内に含まれる訂正符号の復号によりセクタ中に発生したエラーの訂正を行うＰ，Ｑ訂正回路、１６はホストコンピュータと再生装置の間で２ワード（３２ビット）単位のデータ転送を行うインターフェイス回路、１７はアクセスビット幅が１ワード（１６ビット）、２ワード（３２ビット）と可変にアクセス可能で第４図に示したメモリセルＡの構造においてメモリバンク１、２を１６ビット単位でアクセスするメモリバンクに変更し、それ以外の部分を３２ビット化したメモリセルＢ、３１は１セクタ中に記録され光ディスク１でのセクタの存在する位置を示すセクタＩＤを検出、検出したセクタＩＤとホストコンピュータからのアクセス命令に含まれる転送開始セクタＩＤの一致を検出、一致検出結果を１９のアクセス制御回路Ｂに出力するセクタＩＤ検出回路、１８はメモリセルＢにアクセスする対象を制御する際に、１６ビットアクセスの場合は、メモリセルＢの３２ビットデータバスの下位１６ビットとアクセスする対象の１６ビットデータバスをダイレクトに接続し、３２ビットアクセスの場合はメモリセルＢの３２ビットデータバスをそのままダイレクトに接続するセレクタＢ、１９はメモリセルＢのアクセス選択命令、リード、ライト切替命令、１６ビット、３２ビットアクセスビット幅の切替命令、メモリセルＢのアドレス系列（セクタデータ系、Ｐ、Ｑ訂正系、ホスト転送系）の選択命令を生成するアクセス制御回路Ｂ、２０はアドレス系列選択命令に従い、

各系列の１ワード単位のデータに対するアドレスを生成するアドレス生成回路Ｂ、２１は生成されたアドレスをメモリセルＢのアドレスにデコードするアドレスデコーダＢであり、第１図と共通の部分については同一の参照数字をつけて説明を省略する。

同図において、インターフェイス回路１６がホストコンピュータからのアクセス命令を受付けると、ピックアップ２により光ディスク１に記録されている信号が読み取られ、第１図を用いて説明した動作に従い１ワード単位の再生データがメモリセルＡよりリードされセクタ同期検出回路１４に送られる。

ここで第９図を用いてメモリセルＡからリードされる１ワード単位の再生データで構成される1.セクタ構造を、第１０図を用いて２０のアドレス生成回路Ｂにおけるアドレス制御について説明する。

第９図において、メモリセルＡからリードされ構成される１セクタ９０１の構成はセクタの先頭を示す１２バイトのセクタ同期信号９０２と、セクタの存在する光ディスク上のアドレス等の情報を格納した４バイト（２ワード）のセクタＩＤ、ホストコンピュータに転送を行うべきユーザデータ９０４、セクタ中に発生したエラーの訂正を行う為の２８８バイトのＰ、Ｑ訂正符号で構成される。このような構成のセクタに対し、セクタ同期信号の検出を行った残りのデータ（９０６のワード単位の時系列通し番号０～１１６９）に対するアドレス制御は、第１０図に示すように、まず１ワード単位で時系列番号順に図の様にならべ、誤りの訂正を行う際には、Ｐ訂正系列１０Ａの縦方向の系列に対して行い、Ｑ訂正系列１０Ｂの斜め方向の系列に対して行う。ホストコンピュータにデータ転送する際にはワード単位の時系列通し番号２～１０３１を転送、転送の単位は１０Ｃに示すように２ワード（３２ビット）で行われる。これらの各処理のデータ系列に対してアドレス制御を行う際には、図中

１０Ｄのロウアドレス、１０Ｅのカラムアドレスを指定して行い、インターフェイス回路へデータの転送を行う際には、２ワード単位の最初に転送を行うワードデータに対するアドレスを指定し、アドレス制御を行う。

第７図において、第１０図に示したセクタデータのアドレス制御方法でメモリアクセス制御を実行、インターフェイス回路を介しホストコンピュータへ２ワード単位のデータ転送を行う様子を第８図のフローチャートを併せて用い説明する。

第７図、第８図において、インターフェイス回路１６にホストコンピュータからのアクセス命令が受付けられると、光ディスク１から信号の読み出しが開始され、メモリセルＡにおけるアクセスで各処理を行い、１ワード単位のセクタデータがリードされる（ステップ８０１）、１４のセクタ同期検出回路において、リードされたセクタデータに含まれるセクタ同期信号の検出後、１セクタ中に含まれるセクタＩＤの検出を３１のセクタＩＤ検出回路で行う（ステップ８１２）。ホストコンピュータのアクセス命令にはデータ転送を開始する転送開始セクタＩＤが含まれており、この転送開始セクタＩＤと検出セクタＩＤの一致を検出すると、１９のアクセス制御回路Ｂによる各制御対象に対する設定が開始され、一致しなければセクタＩＤの一致検出を継続する（ステップ８０２）。

セクタＩＤの一致検出に従い１９のアクセス制御回路Ｂは１８のセレクタＢ、１７のメモリセルＢ、２０のアドレス生成回路Ｂの各制御対象に対し、転送開始セクタＩＤからのセクタデータをメモリセルＢにライトする為の命令を生成、セレクタＢはアクセス選択命令に従いセクタ同期検出回路１４からの１ワードデータバスとメモリセルＢの２ワードデータバスの内下位１ワードとを接続、メモリセルＢは１６ビット、３２ビット切替命令に従い、ワード単位（１６ビット）で同期検出後のセク

タデータをライトする為、アクセスビット幅を１６ビットに設定、リード、ライト切替命令に従いライトを選択、アドレス生成回路Ｂはアドレス系列選択命令に従いセクタデータ系のアドレスを生成するように設定される（ステップ８０２）。メモリセルＢへのアクセス準備が完了するとセクタ同期信号の検出後のセクタデータが１ワード単位で送られ、アドレス生成回路Ｂは第１０図に示したセクタデータのアドレス制御方法に従いロウアドレス、カラムアドレスを１ワードライト毎に生成、２１のアドレスデコーダＢでメモリセルＢのアドレスにデコードされ１ワード毎にメモリセルＢにライトされる（ステップ８０３）。

メモリセルＢの記憶容量分まで１セクタ単位のセクタデータのライトが行われると（ステップ８０４）、アクセス制御回路Ｂは各制御対象にたいしてＰ訂正系列をメモリセルＢからリードする為の命令を生成する。セレクタＢはＰ，Ｑ訂正回路への１ワードデータバスとメモリセルＢの下位１ワードデータバスとを接続、メモリセルＢはリードを選択、アドレス生成回路ＢはＰ訂正系列のロウ、カラムアドレスを生成するように設定される（ステップ８０５）。Ｐ訂正系列に対するメモリアクセス選択が終了すると、アドレス生成回路Ｂは１ワードリード毎にＰ訂正系列のアドレスを生成、アドレスデコーダＢでメモリセルＢのアドレスにデコードされ１ワード毎にＰ訂正系列データがメモリセルＢからリードされる。リードされたＰ訂正系列に対して系列中に発生したエラーの訂正が実行される（ステップ８０６）。

Ｐ訂正系列の処理が終了すると、アクセス制御回路Ｂは各制御対象に対してＱ訂正系列をメモリセルＢからリードする為の命令を生成する。アドレス生成回路ＢはＱ訂正系列のアドレスを生成するように設定され（ステップ８０７）、Ｑ訂正系列のロウ、カラムアドレスを１ワードリード毎に生成、アドレスデコーダＢでメモリセルＢのアドレスにデコー

ドされ１ワード毎にＱ訂正系列データがメモリセルＢからリードされる。リードされたＱ訂正系列に対して系列中に発生したエラーの訂正が実行される（ステップ８０８）。

Ｑ訂正系列の訂正処理が終了すると、アクセス制御回路Ｂは各制御対象に対してホスト転送データ系列をメモリセルＢからリードする為の命令を生成する。セレクタＢはインターフェイス回路１６への２ワード幅データバス（３２ビット）とメモリセルＢの２ワードデータバスを接続し、メモリセルＢはアクセスビット幅を３２ビットに選択、アドレス生成回路Ｂはホスト転送データ系列のアドレスを生成するように設定され（ステップ８０９）、２ワード単位のホスト転送データ系列の最初の１ワードに対するロウ、カラムアドレスを２ワードリード毎に生成、２ワード単位のデータの最初のワードに対するロウ、カラムアドレスを指定する。アドレスデコーダＢは生成された２ワード単位の先頭アドレスをメモリセルＢのアドレスにデコードし、１回のアクセスにつき２ワード単位でリード、インターフェイス回路１６に転送（ステップ８１０）、インターフェイス回路は２ワード単位でホストコンピュータへデータの転送を行う。ホストコンピュータからの転送要求セクタ数に満たない場合（ステップ８１１）、ステップ８０２から処理を繰返し、要求セクタ数に達したのであれば、処理を終了する。

この第２の実施形態において、光ディスク１から読み取られ、ディジタル化されたシリアルデータに対する復調方法が、シリアルデータに同期して送られてくるビットクロック１７個分のシリアルデータ（復調データ１４ビットとマージン３ビット単位でシリアル転送される）から８ビット単位のパラレルデータにＥＦＭ復調回路で変換される場合、シリアルデータの転送回数を示すビットクロック数と、インターフェイス回路から３２ビット単位でデータ転送を行う際の転送回数との関係は、ア

クセスビット幅可変なメモリを用いた場合、誤り訂正符号等の冗長分を考慮し冗長度が１００％とすると、ビットクロック(１７＋１７)個に対して、８ビットで書き込まれたメモリから３２ビットのデータ量のデータ転送が１回で行われるので３４：１となり、また、冗長度が０の場合１７：１の関係となる。よって、一般的に冗長度は１００％より小、０％より大であるので、ビットクロック周波数１に対して、出力転送周波数Ｆｏは１／３４＜Ｆｏ＜１／１７となる。

これに対して、インターフェイス回路からのデータ転送が１回につき１６ビット単位であれば、同じ３２ビットのデータ量を転送するのに２回転送が必要となり、上記と同様の条件の場合、ビットクロック周波数１に対して、出力転送周波数Ｆｏは１／６８＜Ｆｏ＜１／３４となる。

更にインターフェイス回路からのデータ転送或は、メモリ手段からインターフェイス回路へのデータ転送が８ビット単位で行われるのであれば、３２ビットのデータ量を転送するのにインターフェイス回路からの転送或はメモリアクセスが４回必要となり、上記と同様の条件の場合、ビットクロック(１７＋１７)×４個につき３２ビットのデータ量の転送を行う事になるので(１３６～６８)：１の関係となり、ビットクロック周波数１に対して、出力転送周波数Ｆｏは１／１３６＜Ｆｏ＜１／６８となり、データ転送効率が著しく低下する。　従ってこの実施の形態においては、メモリセルＡからリードされた１ワード単位のデータで構成されるセクタに対する必要な処理を行い、インターフェイス回路を通じてホストコンピュータにデータ転送を行う際には、２ワード単位で行う事が可能となるので、ホストコンピュータへのデータの転送速度が向上する。

また、メモリセルＡ，メモリセルＢのアクセス回数が減少するので、上記した複数のセクタを一時的に記憶するのに必要な大容量のメモリセ

ルＢを含む、再生装置全体の消費電力低減につながる。

また、以上説明した再生処理に必要なメモリセルＡ、メモリセルＢ、各処理回路、制御回路を同一の半導体チップ上に設けた場合でも、ホストコンピュータにデータ転送を行う際には、２ワード単位で行う事が可能となりデータ転送速度が向上すると共に、メモリアクセス回数が減少し、半導体チップ全体の消費電力低減につながる。

第１１図は本発明によるの再生装置及び再生方法の第３の実施の形態を示すブロック図であって、参照数字１はホストコンピュータで処理を行うディジタルデータが記録され、第１図、第７図における光ディスクとは異なる変調方式、エンコード方法で記録した光ディスク、２３は光ディスク１に記録された異なる変調方式の信号に対し元の８ビット単位のデータに復調するデータ復調回路、２４は復調後の複数のセクタ単位のデータで構成される訂正ブロック単位で、光ディスクからの読み出しの際にブロック内に発生したエラーの訂正を行うＰＩ，ＰＯ訂正回路、２６はアクセスビット幅が８ビット、３２ビットと可変にアクセス可能なメモリセルＣ、２７はメモリセルＣにアクセスする対象を制御し、８ビットアクセスの場合は、メモリセルＣの３２ビットデータバスの下位８ビットとアクセスする対象の８ビットデータバスをダイレクトに接続し、３２ビットアクセスの場合はメモリセルＣの３２ビットデータバスをそのままダイレクトに接続するセレクタＣ、２８はメモリセルＣのアクセス選択命令、リード、ライト切替命令、８ビット、３２ビットアクセスビット幅の切替命令、メモリセルＣのアドレス系列（セクタデータ系、ＰＩ，ＰＯ訂正系、ホスト転送系）の選択命令を生成するアクセス制御回路Ｃ、２９はアドレス系列選択命令に従い、各アクセス系列のアドレスを生成するアドレス生成回路Ｃ、３０は生成されたアドレスをメモリセルＣのアドレスにデコードするアドレスデコーダＣであり、第１図、

第７図と共通の部分については同一の参照数字をつけて説明を省略する。

同図において、インターフェイス回路１６がホストコンピュータからのアクセス命令を受付けると、ピックアップ２により光ディスク１に記録されている信号が読み取られ、１４のセクタ同期検出回路でセクタの先頭を検出、２３のデータ復調回路に送られる。データ復調回路２３では光ディスク１に記録された変調方式に従いデータの復調を行う。

ここで、第１３図を用いて復調データの配置方法、訂正系列、ホスト転送系列の説明、及びアドレス制御方法について説明し、第１２図で８ビット、３２ビットとアクセスビット幅の可変な２６のメモリセルＣについて説明する。

第１３図は、アドレス制御を行うデータの配列を示したもので、誤り訂正処理を行う為の訂正ブロックの構成である。図中、復調後のセクタデータ１３Ｇ、行方向のセクタデータに対して訂正を行うＰＩ訂正符号１３Ｈ、列方向のセクタデータに対して訂正を行うＰＯ訂正符号１３Ｉで構成され、誤り訂正はこの訂正ブロック単位内で実行される。１３Ｇのセクタデータは図に示されるように１７２バイト×１２を１単位として構成され、セクタデータ中４バイトのセクタＩＤ，メインデータ１～１２、付加データで構成される。訂正ブロック内ではこの１セクタデータ単位の構成で配置される。また、１３Ａは同期信号の検出、データ復調処理後の８ビット単位のセクタデータ系列を、１３Ｂは１０バイトの１３ＨのＰＩ訂正符号を用い行方向の訂正を行うＰＩ訂正系列を、１３Ｃは１６個の１３ＩのＰＯ訂正符号を用い列方向の訂正を行うＰＯ訂正系列をそれぞれ示す。１３ＤはＰＩ，ＰＯ訂正後のセクタデータ１３Ｇをホストコンピュータに転送する際の読み出し方向であり、１セクタデータの中でメインデータ１～１２の部分を転送、アクセスは４バイト（３２ビット）単位で行われるホスト転送データ系列である。このように配

置されるデータに対してアドレス制御を行う際には１３Ｆのロウアドレス、１３Ｅのカラムアドレスを指定することで行う。

第１２図は第１１図中のメモリセルＣの構成例で、８ビット単位でアクセス可能な４つのメモリバンク１２Ａと１２Ｂ、１２Ｃ、１２Ｄを持ち、行方向、列方向のアドレスを指定する事で各メモリバンクへのアクセスが可能となっている。１２Ｅはバンク切替用のセレクタでバンク選択信号に従い８ビット単位アクセスのメモリバンク１２Ａ～１２Ｄの選択が可能である。１２Ｆのセレクタは８、３２ビット幅切替命令に従い、アクセスビット幅を切替えるセレクタで、３２ビットアクセス時には図中１２Ｈに示すように、メモリバンク１の８ビットバスを最上位８ビットとし、メモリバンク２、３の８ビットバスをそれぞれ中位８ビット、メモリバンク４の８ビットバスを最下位８ビット、合計３２ビットデータとして扱う。８ビットアクセス時にはバンクセレクタ１２Ｅで選択されたメモリバンク１～４の８ビットデータを下位８ビットとし、リード時、上位２４ビットのデータとして“０”を加え３２ビットデータとして扱う。１２Ｇはリード／ライト切替命令に従い、データの転送方向を決定するＩ／Ｏバッファである。このような構成でメモリセルＣは構成され、アクセスビット幅が８ビット、３２ビット単位でアクセスが可能になる。

第１１図において、第１３図に示したデータの配列方法でメモリアクセス制御を実行、第１２図に示した構成のメモリセルＣを用いてアクセスを行い、インターフェイス回路を介しホストコンピュータまでデータ転送を行う様子を第１４図のフローチャートを併せて用い説明する。

第１１図、第１４図において、ホストコンピュータからのホストアクセス命令が１６のインターフェイス回路において受付けられ、光ディスク１から信号の読み出しが開始されると、信号中に含まれるセクタの先

頭を示す同期信号の検出が１４のセクタ同期検出回路で行われ、２３のデータ復調回路で８ビット単位のデータに復調、復調されたデータ中のセクタＩＤを３１のセクタＩＤ検出回路で行う。（ステップ１４Ａ）、ホストコンピュータのアクセス命令には転送を開始する転送開始セクタＩＤが含まれており、この要求セクタＩＤと検出セクタＩＤが一致したのであれば２８のアクセス制御回路Ｃによるメモリセルアレイへのアクセスの為の各設定が開始され、一致しなければセクタＩＤの一致検出を継続する（ステップ１４Ｂ）。

セクタＩＤの一致検出に従い２８のアクセス制御回路Ｃは２７のセレクタＣ、２６のメモリセルＣ、２９のアドレス生成回路Ｃの各制御対象に対し、転送開始セクタＩＤが含まれるセクタデータをメモリセルＣにライトする為命令を生成、セレクタＣはアクセス選択命令に従いデータ復調回路２３からの８ビットデータバスとメモリセルＣの３２ビットデータバスの内、下位８ビットとを接続、メモリセルＣは８ビット、３２ビット切替命令に従い、８ビット単位でデータ復調後のセクタデータをライトする為、アクセスビット幅を８ビットに設定、リード、ライト切替命令に従いライトを選択、アドレス生成回路Ｃはアドレス系列選択命令に従い復調後のセクタ系列のアドレスを生成するように設定される（ステップ１４Ｃ）。メモリセルＣへのアクセス準備が完了するとデータ復調後のセクタデータが送られ、アドレス生成回路Ｃは復調後のセクタデータ系列のロウアドレス、カラムアドレスを８ビット単位のリード毎に生成、３０のアドレスデコーダＣでメモリセルＣのアドレスにデコードされ８ビット単位でセクタデータがメモリセルＣにライトされる（ステップ１４Ｄ）。

誤り訂正が可能な訂正ブロックがメモリセルＣの容量分ライトされると（ステップ１４Ｅ）、アクセス制御回路Ｃは各制御対象にたいしてＰ

Ｉ訂正系列をメモリセルＣからリードする為の命令を生成する。セレクタＣはＰＩ，ＰＯ訂正回路への８ビットデータバスとメモリセルＣの下位８ビットデータバスとを接続、メモリセルＣはリードを選択、アドレス生成回路ＣはＰＩ訂正系列のロウ、カラムアドレスを生成するように設定される（ステップ１４Ｆ）。ＰＩ訂正処理の為のメモリアクセス選択が終了すると、アドレス生成回路ＣはＰＩ訂正系列のアドレスを生成、アドレスデコーダＣでメモリセルＣのアドレスにデコードされ８ビット単位でＰＩ訂正系列データがメモリセルＣからリードされる。リードされたＰＩ訂正系列に対して系列中に発生したエラーの訂正が実行される（ステップ１４Ｇ）。

ＰＩ訂正系列の処理が終了すると、アクセス制御回路Ｃは各制御対象に対してＰＯ訂正系列をメモリセルＣからリードする為の命令を生成する。アドレス生成回路ＣはＰＯ訂正系列のアドレスを生成するように設定され（ステップ１４Ｈ）、ＰＯ訂正系列のロウ、カラムアドレスを８ビット単位のリード毎に生成、アドレスデコーダＣでメモリセルＣのアドレスにデコードされ８ビット単位でＰＯ訂正系列データがメモリセルＣからリードされる。リードされたＰＯ訂正系列に対して系列中に発生したエラーの訂正が実行される（ステップ１４Ｉ）。

ＰＯ訂正系列の訂正処理が終了すると、アクセス制御回路Ｃは各制御対象にたいしてホスト転送データ系列をメモリセルＣからリードする為の命令を生成する。セレクタＣはインターフェイス回路１６への３２ビットバスとメモリセルＣの３２ビットデータバスを接続し、メモリセルＣはアクセスビット幅を３２ビットに選択、アドレス生成回路Ｂはホストへ転送すべきデータ、第１３図の１３Ｇに示すように１セクタデータ中のメインデータ１～１２のホスト転送データ系列のアドレスを生成するように設定され（ステップ１４Ｊ）、ホスト転送データ系列のロウ、

カラムアドレスを生成、３２ビット単位のデータの最初にアクセスするロウ、カラムアドレスを指定する。アドレスデコーダＣは生成された３２ビット単位の先頭アドレスをメモリセルＣのアドレスにデコードし、１回のアクセスにつき３２ビット単位でリード、インターフェイス回路１６に転送、訂正ブロック中に含まれるメインデータに転送処理を行う（ステップ１４Ｋ）。ホストコンピュータからの転送要求セクタ数に満たない場合（ステップ１４Ｌ）、ステップ１４Ｃから処理を繰返し、要求セクタ数に達したのであれば、処理を終了する。

この第３の実施形態において、光ディスク１から読み取られ、ディジタル化されたシリアルデータに対する復調方法が、シリアルデータに同期して送られてくるビットクロック１６個分のシリアルデータから８ビット単位のパラレルデータにデータ復調回路で変換される場合、シリアルデータの転送回数を示すビットクロック数と、インターフェイス回路から３２ビット単位でデータ転送を行う際の転送回数との関係は、アクセスビット幅可変なメモリを用いた場合、誤り訂正符号等の冗長分を考慮し冗長度が１００％とすると、ビットクロック(１６＋１６)個に対して、８ビットで書き込まれたメモリから３２ビットのデータ量のデータ転送が１回で行われるので３２：１となり、また、冗長度が０の場合１６：１の関係となる。よって、一般的に冗長度は１００％より小０％より大であるので、ビットクロック周波数１に対して、出力転送周波数Ｆｏは１／３２＜Ｆｏ＜１／１６となる。

これに対して、インターフェイス回路からのデータ転送が１回につき１６ビット単位であれば、同じ３２ビットのデータ量を転送するのに２回転送が必要となり、上記と同様の条件の場合、ビットクロック周波数１に対して、出力転送周波数Ｆｏは１／６４＜Ｆｏ＜１／３２となる。

更にインターフェイス回路からのデータ転送或は、メモリ手段からイ

ンターフェイス回路へのデータ転送が８ビット単位で行われるのであれば、３２ビットのデータ量を転送するのにインターフェイス回路からの転送或はメモリアクセスが４回必要となり、上記と同様の条件の場合、ビットクロック周波数１に対して、出力転送周波数Ｆｏは１／１２８＜Ｆｏ＜１／６４となり、データ転送効率が著しく低下する。

従って第３の実施の形態においては、光ディスクから読みだされた信号に対し必要な処理を行い、インターフェイス回路を通じてホストコンピュータにデータ転送を行う際には、３２ビット単位で行う事により、ホストコンピュータへのデータの転送速度が向上する。また、メモリセルＣのアクセス回数が減少するので、上記した複数の訂正ブロックを一時的に記憶するのに必要な大容量のメモリセルＣを含む、再生装置全体の消費電力低減につながる。

また、以上説明した再生処理に必要なメモリセルＣ、各処理回路、制御回路を同一の半導体チップ上に設けた場合でも、ホストコンピュータにデータ転送を行う際には、３２ビット単位で行う事が可能となりデータ転送速度が向上すると共に、メモリアクセス回数が減少し、半導体チップ全体の消費電力低減につながる。

第１５図は本発明による第４の実施の形態を示すブロック図であって、ディスク記録装置に適応した例である。参照数字１はホストコンピュータから転送されたディジタルデータを記録可能な光ディスクで、ディスクに記録する際の位置を示す為のセクタ同期信号、物理ＩＤがあらかじめ記録されている光ディスク、２は光ディスク１に対し変調信号の読みだし、書込みが可能なピックアップ、３２は光ディスク１にあらかじめ記録された物理ＩＤを検出し、検出ＩＤと記録を開始する物理ＩＤとの一致を検出する物理ＩＤ検出回路、３３は１訂正ブロックを構成するＰＩ，ＰＯ訂正符号の生成を行う訂正符号生成回路、３４は光ディスク１

へ記録を行う為の信号に変調を行うデータ変調回路、３５は１セクタデータ中に含まれる付加データ、セクタＩＤをメインデータに付加する、付加データ生成回路であり、第１１図と共通の部分は同一の参照数字をつけて説明を省略する。

同図において、インターフェイス回路１６がホストコンピュータからの記録要求命令を受付けると、光ディスク１に記録を行う為のデータがインターフェイス回路に送られてくる。

本実施の形態におけるホストコンピュータからの転送データの配置方法、訂正系列、データ変調系列、アドレス制御方法は第３の実施の形態で説明した第１３図の訂正ブロックと同様の構成を取り、１３Ｇに示すように転送データをメインデータ１～１２に割当て、セクタＩＤ，付加データをそれぞれ付加し１セクタデータを構成、１３Ｄに示す方向に配置する。これを複数集めたセクタデータに対して１３Ｃの方向の系列に対してＰＯ訂正符号を生成、付加を行い、１３Ｂの方向の系列にたいしてＰＩ訂正符号を生成、付加する。変調処理を行う為のデータ読み出し系列は１３Ａの方向に対して行われる。アドレス制御については同様に１３Ｆのロウアドレス、１３Ｅのカラムアドレスを指定することで行う。

第１５図において、第１３図を用いて説明したデータの配列方法でメモリアクセス制御を実行、メモリセルＣにおいてアクセスを行い、光ディスク１にホストコンピュータからの転送データの記録を行う様子を第１６図のフローチャートを併せて用い説明する。

第１５図、第１６図において、ホストコンピュータからの記録要求命令が１６のインターフェイス回路において受付けられ、ホストコンピュータからの３２ビット単位の転送データがインターフェイス回路に送られてくると（ステップ１６Ａ）、記録要求命令に従い２８のアクセス制御回路Ｃは２７のセレクタＣ、２６のメモリセルＣ、２９のアドレス生

成回路Ｃの各制御対象に対し、インターフェイス回路からの転送データをメモリセルＣにライトずる為の命令を生成、セレクタＣはアクセス選択命令に従い３５の付加データ生成回路からの３２ビットデータバスとメモリセルＣの３２ビットデータバスを接続、メモリセルＣは８ビット、３２ビット切替命令に従い、付加データを付加後の３２ビット単位で送られてくる転送データをライトする為、アクセスビット幅を３２ビットに設定、リード、ライト切替命令に従いライトを選択、アドレス生成回路Ｃはアドレス系列選択命令に従い付加データ生成回路からのセクタデータ系列のアドレスを生成するように設定される（ステップ１６Ｂ）。

メモリセルＣへのアクセス準備が完了するとインターフェイス回路に送られた転送データに対して付加データを付加し１セクタデータを形成し（ステップ１６Ｃ）、アドレス生成回路Ｃは第１３図中の１３Ｄに示す系列のロウアドレス、カラムアドレスを３２ビット単位のリード毎に生成、３０のアドレスデコーダＣでメモリセルＣのアドレスにデコードされ３２ビット単位でセクタデータがメモリセルＣにライトされる（ステップ１６Ｄ）。

ＰＩ，ＰＯ訂正符号が生成可能な分のセクタデータがライトされると（ステップ１６Ｅ）、アクセス制御回路Ｃは各制御対象に対してＰＯ訂正系列をメモリセルＣからリードする為の命令を生成する。セレクタＣは訂正符号生成回路への８ビットデータバスとメモリセルＣの下位８ビットデータバスとを接続、メモリセルＣはリードを選択、アドレス生成回路ＣはＰＯ訂正系列のロウ、カラムアドレスを生成するように設定される（ステップ１６Ｆ）。ＰＯ訂正処理の為のメモリアクセス選択が終了すると、アドレス生成回路ＣはＰＯ訂正系列のアドレスを生成、アドレスデコーダＣでメモリセルＣのアドレスにデコードされ８ビット単位でＰＯ訂正系列データがメモリセルＣからリードされる。リードされた

ＰＯ訂正系列に対してＰＯ訂正符号を生成し、メモリセルＣ中のＰＯ訂正符号の領域にあたるアドレスにたいしてＰＯ訂正符号がライトされる（ステップ１６Ｇ）。

ＰＯ訂正符号の生成、付加が終了すると、アクセス制御回路Ｃは各制御対象に対してＰＩ訂正系列をメモリセルＣからリードする為の命令を生成する。アドレス生成回路ＣはＰＩ訂正系列のアドレスを生成するように設定され（ステップ１６Ｈ）、ＰＩ訂正系列のロウ、カラムアドレスを８ビット単位のリード毎に生成、アドレスデコーダＣでメモリセルＣのアドレスにデコードされ８ビット単位でＰＩ訂正系列データがメモリセルＣからリードされる。リードされたＰＩ訂正系列に対してＰＩ訂正符号を生成し、メモリセルＣ中のＰＩ訂正符号の領域にあたるアドレスにたいしてＰＩ訂正符号がライトされる（ステップ１６Ｉ）。

ＰＩ訂正符号の生成、付加が終了すると、アクセス制御回路Ｃは各制御対象にたいして変調データ系列をメモリセルＣからリードする為の命令を生成する。セレクタＣはデータ変調回路３４への８ビットバスとメモリセルＣの下位８ビットデータバスを接続し、、アドレス生成回路Ｂはデータ変調回路へ転送すべき第１３図中の１３Ａに示すデータ系列のアドレスを生成するように設定される（ステップ１６Ｊ）。

光ディスク１への記録データの準備が終了すると、光ディスク１から信号の読み出しを行い、あらかじめ記録されている物理ＩＤの検出を３２の物理ＩＤ検出回路で行われる（ステップ１６Ｋ）。光ディスク１上の記録を開始する物理ＩＤと検出された物理ＩＤがが一致したのであれば（ステップ１６Ｌ）、２９のアドレス生成回路Ｃによるアドレス制御を開始し、変調データ系列のロウ、カラムアドレスを８ビット単位のリード毎に生成、アドレスデコーダＣは生成された３２ビット単位の先頭アドレスをメモリセルＣのアドレスにデコードし、データ復調回路１６

に転送、データ変調処理後光ディスク１に記録する（ステップ１６Ｍ）。

ホストコンピュータからの記録要求セクタ数に満たない場合（ステップ１６Ｎ）、ステップ１６Ｂから処理を繰返し、要求セクタ数を記録したのであれば、処理を終了する。

この第４の実施の形態において、光ディスク１にデータを記録する際に、インターフェイス回路に１回の転送で３２ビット単位でデータ転送を行ってから、記録媒体に記録を行う８ビット単位のデータに対して１６ビットのデータに変調処理を行った後シリアルデータを生成し、その時の変調手段の動作クロック１６個であらわされる転送回数、或はそれと同等の１６個の転送回数が判明するような信号に従ってシリアルデータが記録媒体に記録される場合、インターフェイス手段へ１回の転送につき３２ビット単位のデータ転送を行う際の転送回数と、シリアルデータの記録媒体への転送回数との関係は、アクセスビット幅可変なメモリを用いた場合、誤り訂正符号等の冗長分を考慮し冗長度が１００％とすると、３２ビットのデータ量のデータ転送１回に対して３２ビットで書き込まれたメモリから８ビットのデータ量のデータ転送が４回行われるので、記録媒体へシリアルデータの転送が(１６＋１６)×４＝１２８回行われ、また、冗長度が０の場合１６×４＝６４回行われる。よって、一般的に冗長度は１００％より小０％より大であるので、インターフェイス手段へのデータ転送１回に対して、記録媒体へのシリアルデータの転送回数Ｓｉは６４＜Ｓｉ＜１２８となる。

これに対して、インターフェイス回路へのデータ転送が１回につき１６ビット単位であれば、同じ３２ビットのデータ量を転送するのに２回の転送を必要となり、上記と同様の条件の場合、インターフェイス手段へのデータ転送１回に対して、記録媒体へのシリアルデータの転送回数Ｓｉは３２＜Ｓｉ＜６４となり、記録媒体へのデータ転送効率が低下す

る。

インターフェイス回路が３２ビットでも、アクセスビット幅可変なメモリを用いず、インターフェイス回路からメモリ手段へのデータ転送が１６ビット単位で行われるのであれば、３２ビットのデータ量を転送するのに１６ビット単位のメモリアクセスが２回必要となり、上記と同様に、メモリアクセス１回に対して、記録媒体へのシリアルデータの転送回数Ｓｉは３２＜Ｓｉ＜６４となる。

更にインターフェイス回路へのデータ転送、或はインターフェイス回路からメモリ手段へのデータ転送が８ビット単位で行われるのであれば、３２ビットのデータ量を転送するのに８ビット単位のインターフェイス回路への転送、或はメモリアクセスが４回必要となり、冗長度は１００％の場合８ビットのデータ量のデータ転送１回に対して、記録媒体へシリアルデータの転送が(１６＋１６)×(８÷８)＝３２回行われ、冗長度が０の場合１６×(８÷８)＝１６回行われる。すなわち、上記と同様の条件の場合、インターフェイス手段へのデータ転送、或はインターフェイス回路からメモリ手段へのデータ転送１回に対して、記録媒体へのシリアルデータの転送回数Ｓｉは１６＜Ｓｉ＜３２となり、記録媒体へのデータ転送効率が著しく低下する。

従ってこの実施の形態においては、ホストコンピュータから転送されたデータに対して、光ディスク１に記録する為に必要なエンコード処理を行い、記録を行う際には、転送データを３２ビット単位でメモリセルＣにライトする事によりデータ転送に必要な時間が減少し、記録を行う光ディスクに対するディジタル信号のエンコードの為の処理速度が向上する。また、アクセス回数が減少するので、生成される複数の訂正ブロックを一時的に記憶するのに必要な大容量のメモリセルＣを含む、記録装置全体の消費電力低減につながる。

また、以上説明した記録処理に必要なメモリセルC、各処理回路、制御回路を同一の半導体チップ上に設けた場合でも、転送データを32ビット単位でメモリセルCにライトする事によりデータ転送に必要な時間が減少し、記録を行う光ディスクに対するディジタル信号のエンコードの為の処理速度が向上すると共に、メモリアクセス回数が減少し、半導体チップ全体の消費電力低減につながる。

第17図は本発明による再生装置及び再生方法の第5の実施の形態を示すブロック図であって、第7図を用いて説明した第2の実施の形態と同一の処理を行い、1つのメモリセルDで再生装置を構成した場合を示す。参照数字36はアクセスビット幅が8ビット、16ビット、32ビットと可変にアクセス可能なメモリセルD、37はメモリセルDにアクセスする対象を制御し、8ビットアクセスの場合は、メモリセルDの32ビットデータバスの下位8ビットとアクセスする対象の8ビットデータバスをダイレクトに接続、16ビットアクセスの場合は、メモリセルDの32ビットデータバスの下位16ビットとアクセスする対象の16ビットデータバスをダイレクトに接続、32ビットアクセスの場合はメモリセルDの32ビットデータバスをそのままダイレクトに接続するセレクタD、38はメモリセルDのアクセス選択命令、リード、ライト切替命令、8ビット、16ビット、32ビットアクセスビット幅の切替命令、メモリセルDのアドレス系列（復調データ系、C1、C2訂正系、再生データフレーム系、PI，PO訂正系、ホスト転送系）の選択命令をそれぞれ生成するアクセス制御回路D、39はアドレス系列選択命令に従い、各アクセス系列のアドレスを生成するアドレス生成回路D、40は生成されたアドレスをメモリセルDのアドレスにデコードするアドレスデコーダDであり、第7図に対応する部分は同一の参照数字をつけて重複する説明を省略する。

同図において、インターフェイス回路１６がホストコンピュータからのアクセス命令を受付けると、ホストコンピュータに転送を行うデータが記録されているディスク上の位置の付近から、ピックアップ２により光ディスク１に記録されている信号が読み取りが開始され、フレーム同期信号の検出を４のフレーム同期検出回路で行った後、５のＥＦＭ復調回路で８ビット単位の復調データに復調される。２８のアクセス制御回路Ｄは、これと同時に、３７のセレクタＤ、３６のメモリセルＤ、３９のアドレス生成回路Ｄそれぞれの制御対象に対し、８ビット（１シンボル）単位で送られてくる復調データメモリセルＤにライトするように制御する。メモリセルＤにアクセスする際のアドレス制御方法は、第３図で説明した制御方法（ロウ、カラムアドレス、ロウバンク、カラムバンクアドレスを指定）で行われ、復調データ系列に対するアドレスをアドレス生成回路Ｄで生成、アドレスデコーダＤでメモリセルＤの実際のアドレスにデコードされ、このデコードアドレスに従い復調データをメモリセルＤにライトする。

復調データのライトをホストコンピュータへ転送する容量分、或はメモリセルＤの記憶容量分行いＣ２訂正が可能な復調データがライトされると、アクセス制御回路Ｄはそれぞれの制御対象に対し、８ビット（１シンボル）単位でＣ１訂正を行うデータ系列をメモリセルＤからリードするように制御する。

Ｃ１訂正を行うデータ系列がリードされＣ１訂正処理が終了すると、アクセス制御回路Ｄはそれぞれの制御対象に対し、８ビット（１シンボル）単位でＣ２訂正を行うデータ系列をメモリセルＤからリードするように制御する。

Ｃ２訂正系列に対する誤り訂正処理が終了すると、アクセス制御回路Ｄはそれぞれの制御対象に対し、１６ビット（１ワード）単位で再生デ

ータ系列をリードするように制御し、１４のセクタ同期検出回路に転送される。リードされた再生系列は第９図に示したセクタ単位のデータを構成し、再生データ系列に含まれるセクタ同期信号の検出、同期信号の直後の２ワードデータに記録されているセクタＩＤの検出を３１のセクタＩＤ検出回路で行う。

セクタ同期信号の検出処理が終了すると、アクセス制御回路Ｄはそれぞれの制御対象に対し、セクタ同期信号以外のセクタデータの配列中に含まれるＰ訂正系列に対する誤り訂正処理を行うため、Ｐ訂正系列に対するデータ系列をメモリセルＤからリードするように制御する。

Ｐ訂正系列に対する誤り訂正処理が終了すると、アクセス制御回路Ｄはそれぞれの制御対象に対し、セクタ同期信号以外のセクタデータの配列中に含まれるＱ訂正系列に対する誤り訂正処理を行うため、Ｑ訂正系列に対するデータ系列をメモリセルＤからリードするように制御する。

Ｑ訂正系列に対する誤り訂正処理が終了すると、アクセス制御回路Ｄはそれぞれの制御対象に対し、ホストコンピュータへの転送データ系列を３２ビット単位でメモリセルＤからリードするように制御する。ホストコンピュータのアクセス命令にはデータ転送を開始する転送開始セクタＩＤが含まれており、また、セクタ同期信号の検出を行った際にメモリセルＤに記憶されているセクタデータに対するＩＤが検出されている。この転送開始セクタＩＤと検出セクタＩＤが一致するセクタを含み、それ以降のセクタＩＤに対するセクタに含まれるホスト転送データ系列に対し、メモリセルＤからリードを行い、１回のアクセスにつき３２ビット（２ワード）単位でインターフェイス回路１６に転送され、ホストコンピュータへ転送される。

ホストコンピュータからの転送要求セクタ数に満たない場合は、ＥＦＭ復調回路からの８ビット（１シンボル）単位の復調データライトから

処理を再開し、要求セクタ数に達したのであれば、処理を終了する。

以上説明した処理を実行する為のメモリセルDへのアクセスは全て1バンク単位に対するロウアドレス、カラムアドレス、バンクに対するロウバンクアドレス、カラムバンクアドレスを指定する事でアドレス制御が行われる。

この第5の実施の形態においても、前記した第2の実施の形態と同様に、ＥＦＭ復調回路で変換される場合、シリアルデータ（復調データ14ビットとマージン3ビット単位でシリアル転送）の転送回数を示すビットクロックと、インターフェイス回路から３２ビット単位でデータ転送を行う際の転送回数との関係は、アクセスビット幅可変なメモリを用いた場合、ビットクロック周波数1に対して、出力転送周波数Ｆｏは１／３４＜Ｆｏ＜１／１７となる。また、インターフェイス回路からのデータ転送が1回につき１６ビット単位であれば、１／６８＜Ｆｏ＜１／３４、更にインターフェイス回路からのデータ転送或は、メモリ手段からインターフェイス回路へのデータ転送が8ビット単位で行われるのであれば、１／１３６＜Ｆｏ＜１／６８となり、データ転送効率が著しく低下する。

従ってこの実施の形態においては、光ディスクからの読み出し信号に対し、復調処理を行った8ビット単位の復調データの配列への配置を行うメモリアクセス、Ｃ１、Ｃ２訂正処理を行うデータ系列に対するアクセス、セクタ同期信号の検出を行う系列に対するアクセス、Ｐ，Ｑ訂正処理を行うデータ系列に対するアクセス、インターフェイス回路への転送データ系列に対するアクセスを1つのメモリセルDにより行う事で、第7図で説明した再生装置と同様の処理、同等のデータ転送速度を実現でき、また、再生装置の構成が容易になる。

また、1つのメモリセルDで処理を実現する事により、制御回路が1

系統ですみ、このメモリセルD、処理に必要な各処理回路、制御回路を同一の半導体チップ上に設けた場合、図7の再生装置の構成を同一の半導体チップに実現した場合よりも、半導体チップ全体の消費電力の低減効果が大きく、半導体チップのサイズも押さえる事ができ、半導体の製造コストの面からも有利である。

なお以上に示した実施の形態において、データを貯える記録媒体はこの実施の形態の光ディスクに限定される物でなく、取り扱うディジタル信号をメモリ等の一時的にデータを記憶する手段に記憶し、所定の処理を行い転送データを出力するような形態のディジタル信号処理システム、例えばテープ状の記録媒体の記録再生装置、磁気ディスク記録媒体の記録再生装置、或はデータ転送システム、通信システム等にも適用でき、かつこれらのディジタル信号処理システムにおける処理に必要なアクセスビット幅可変なメモリ等の記憶手段と、所定の処理実行に必要な周辺回路、処理手段を同一の半導体チップ上に設け実現した場合にも適用できる。

また、アクセスビット幅可変なメモリを制御する制御手段は、同等の制御機能を実現する様にプログラムされたマイクロプロセッサを用い実現してもかまわず、プログラムの変更により可変なアクセスビット幅を、処理を実行するディジタル信号のビット幅に合わせ、変更できるようにして処理を実行してもよく、この場合アクセスビット幅可変なメモリとマイクロプロセッサを含む所定の処理を行う手段を同一の半導体チップ上に設る事により実現される。

また、アクセスビット幅可変なメモリを同一の半導体チップ上に設ける場合、メモリは一定時間間隔で書換が必要なダイナミックなメモリ、あるいは書換動作の必要が無いスタティックなメモリどちらで実現しても構わない。

また、第１から第５の実施の形態で用いるメモリセルの構成はこの実施の形態に限定される物でなく、アクセスを行う処理手段に応じてアクセスビット幅を可変にできるメモリセルであればどんな構成をとっても構わない。

第１の実施の形態におけるアドレス制御の単位である１バンクの構成は、この実施の形態に限定される物でなく、メモリ等の一時記憶手段に記録、所定の処理を行った後の転送データに対するアクセスが容易になるような１バンク構成が採用される。

第２、第３、第４の実施の形態における、メモリセルＢ、メモリセルＣにおいて、各処理を行う際に必要なデータ系列のアクセスに対するアドレス制御方法は、第１図の実施の形態で説明した、１バンク単位で、１バンク中のロウアドレス、カラムアドレス、バンクに対するロウバンクアドレス、カラムバンクアドレスを指定することにより行ってもよい。

第２、第３、第４、第５の実施の形態におけるホストコンピュータとの間でデータ転送を行うインターフェイス回路はこの実施の形態に限定される物でなく、ホストコンピュータとのアクセスバス幅が６４ビットあるいはそれ以上でも構わない。この場合メモリセルはインターフェイス回路との間で６４ビット単位、或はそれ以上のアクセスビット幅でデータ転送を実行し、それぞれのアクセスビット幅に対応したメモリセル、アクセスの対象を制御するセレクタが用意される。

また、第４の実施の形態において記録可能な光ディスク１にあらかじめ記録されている物理ＩＤの検出方法は、この実施の形態に限定される物でなく、光ディスク中の記録トラックをうねらせＩＤの代用となる物を記録した光ディスクの記録にも適応される。この場合のＩＤ検出は例えば、トラックのうねりによる周波数変化を物理ＩＤ検出回路で計測し、光ディスク上のアドレスとして認識され処理が行われる。

また、説明した全ての実施の形態において用いられるメモリ手段の、可変なアクセスビット幅の種類は、この実施の形態に限定される物でなく、メモリ手段に記憶されているデータ配列に対して、処理を実行する手段が最も効率よく処理を行えるようアクセスする処理手段に応じて何種類にでも切替えるようにしても良い。

また、説明した全ての実施の形態を実現する為に必要なメモリセル、各処理回路、制御回路、或は処理回路、制御回路と同等の処理をプログラム制御により実行するマイクロプロセッサを同一の半導体チップ上に設けることによっても、再生装置、記録装置と同様の処理が実現できる。

産業上の利用可能性

本発明によると、光ディスクから読みだされた信号に対しデータ復調処理後の１シンボル（８ビット）単位のデータ書込みから、２シンボル（１６ビット）単位で再生データの読み出しを行うまでのアドレス制御を、まとまった複数シンボル単位で１バンクを構成し、１バンク中のロウ、カラムアドレスと、バンクに対するロウバンク、カラムバンクアドレスを指定して１又は２シンボル単位のデータに対するアクセスを行う事によりアドレス制御が容易となる。

また、アドレス制御を行う際の再生データ系列の配置を工夫し、それに対するＣ１、Ｃ２訂正系列、復調系列の配置でアドレス制御する事により１回のアクセスで再生データを２シンボル転送する事が容易になる。

また、再生データ系列の読み出しの際のアクセスビット幅を１６ビット或は３２ビットで行うため、再生データを１回のアクセスにつき１６ビット或は３２ビット単位で転送でき、再生データに対して補間、フィルタ処理を行う手段やホストコンピュータとのインターフェイス手段へのデータ転送速度が向上し、インターフェイス手段からホストコンピュ

ータへのデータ転送速度も向上する。また、一連のディジタル信号処理を行う際に必要なメモリアクセス回数を減少させる事ができる。

また、一連のディジタル信号処理に必要なメモリ手段、各処理回路、制御回路を同一の半導体チップ上に設ける際には、各処理を効率良く行うために必要なメモリ手段へのアクセスビット幅の単位で処理を行えるように構成される。例えばＥＦＭ復調回路は８ビット単位で復調データを出力するように構成され、１６ビットディジタルオーディオ再生データに対する出力補間、フィルタ処理回路はデータの単位にあわせて１６ビット単位で処理を行うよう構成、ホストコンピュータとの間でデータ転送を行うインターフェイス回路は、ホストコンピュータとのインターフェイスバス幅にあわせて１６ビット、３２ビット或はそれ以上のバス幅でメモリ手段とのデータ転送を行うように構成される。これら処理回路により異なるアクセスビット幅に対し、メモリ手段は可変なアクセスビット幅の種類に対応したアクセスが可能なようにカスタマイズされ、アクセスする対象に従って可変にアクセスビット幅を設定できるようなメモリ手段が半導体チップ上に設けられる。

このように一連のディジタル信号処理に必要な手段とアクセスビット幅を可変に設定できるようにカスタマイズされたメモリ手段を同一の半導体チップ上に実現した場合でも、メモリアクセス回数の減少による半導体チップ全体の消費電力低減、一連のディジタル信号処理の高速処理が実現できると共に、半導体チップから出力される再生データの転送速度向上が実現できる。また、アクセスビット幅可変にカスタマイズされたメモリ手段をダイナミックなメモリで構成した場合には、大容量メモリを必要とするディジタル信号処理システムを同一の半導体チップ上に実現でき、消費電力の低減、高速な信号処理、半導体チップからのデータ転送速度の向上の効果を得る事ができる。

請求の範囲

1．記録媒体からの読み出し信号に対し所定の信号処理を行う信号処理手段と、データを一時的に記憶するメモリ手段を有し信号処理後のディジタルデータを出力するディジタル信号再生装置であって、

有効アクセスビット幅をｎビットとｎ×ｍビット（ｎ、ｍは自然数）に変更可能なバス幅可変手段と、

前記メモリ手段のアクセスを行う制御手段とを有し、

該制御手段は、前記バス幅可変手段により、前記メモリ手段の有効アクセスビット幅をｎビットとｎ×ｍビットのバス幅に変更可能であり、少なくとも、前記メモリ手段に対して、ｎビット単位のディジタルデータの書込みを行い、ｎ×ｍビット単位で読出しを行うことを特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

2．請求の範囲第1項記載のバス幅可変メモリを用いたディジタル信号再生装置において、

前記制御手段は、前記メモリ手段のアクセスとして、ｎビット単位で、ディジタルデータを所定の順番に配列するためのデータの書込み、及び、配列中のデータに含まれる誤り訂正に必要な処理を実行する為のデータ系列の読み出しを行い、ｎ×ｍビット単位で転送データ系列の読み出しを行うことを特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

3．請求の範囲第2項記載のバス幅可変メモリを用いたディジタル信号再生装置において、

前記バス幅可変手段と、メモリ手段と、少なくとも前記誤り訂正を行う訂正手段は、同一の半導体チップ上に設けることを特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

4．請求の範囲第3項記載のバス幅可変メモリを用いたディジタル信号再生装置において、

前記メモリ手段は、一定時間で書き直し動作が必要なダイナミックなメモリを用いることを特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

5．請求の範囲第1項記載のバス幅可変メモリを用いたディジタル信号再生装置において、

前記メモリ手段は、nビット幅でアクセスを行う一時記憶手段m個からなり、

前記バス幅可変手段は、前記m個の一時記憶手段の選択を行う第1の選択手段と、

該第1の選択手段で選択されたnビットデータバスと、m個の一時記憶手段で構成されたn×mビットデータバスの選択を行う第2の選択手段と

を有することを特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

6．請求の範囲第1項記載のバス幅可変メモリを用いたディジタル信号再生装置において、

記録媒体からの読取り信号を復調し該復調データをnビット単位で出力する復調手段と、

誤り訂正処理に対するデータ配列に対し、nビット単位で処理を行う誤り訂正手段と、

誤り訂正後のデータ配列に対し、n×mビット単位で処理を行う出力処理手段と、

前記メモリ手段のデータバスに対し、前記復調手段、誤り訂正手段、出力処理手段のデータバスを選択的に接続する接続手段と

前記復調手段、誤り訂正手段、出力処理手段のそれぞれの処理に必要な、データ配列のアクセスに必要なアドレスを生成するアドレス生成手段と、

生成されたアドレスをメモリ手段上のアドレスにデコードする手段と、

前記メモリ手段、接続手段、アドレス生成手段に対する制御命令を生成する手段とを有し、

前記制御手段は、前記メモリ手段のアクセスとして、ｎビット単位で、復調後のディジタルデータを所定の順番に配列するためデータの書込み、及び、配列中のデータに含まれる誤り訂正に必要な処理を実行する為のデータ系列の読み出しを行い、ｎ×ｍビット単位で前記出力処理手段への転送データの読み出しを行う際に、ｎ×ｍビットのバス幅とすることを特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

7．請求の範囲第6項記載のバス幅可変メモリを用いたディジタル信号再生装置において、

前記アドレス生成手段は、前記復調手段からのデータ書込み、前記誤り訂正手段へのデータ読み出し、前記出力手段へのデータ読み出しを行う時、それぞれの処理の対象のデータ配列に対しｎ×ｉビット（ｉは自然数）と（ｎ×ｍ）×ｊビット（ｊは自然数）を単位とするバンク単位でアクセスを行うために、1バンク単位の縦方向のアドレスと横方向のアドレス、及び、各バンクにおける、縦方向のバンクアドレス、横方向のバンクアドレスをそれぞれ生成することを特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

8．請求の範囲第1項記載のバス幅可変メモリを用いたディジタル信号再生装置において、

記録媒体からの読取り信号を復調し該復調データをｎビット単位で出力する復調手段と、

誤り訂正処理に対するデータ配列に対し、ｎビット単位で処理を行う誤り訂正手段と、

誤り訂正後のデータ配列に対し、ｎ×ｍビット単位でデータを受付け、ｎ×ｍビット単位でホストコンピュータへデータ転送を行うインターフェイス手段と、

前記メモリ手段のデータバスに対し、前記復調手段、誤り訂正手段、インターフェイス手段のデータバスを選択的に接続する接続手段と

前記復調手段と前記誤り訂正手段のそれぞれの処理に必要なデータ配列及び前記インターフェイス手段へデータ転送を行う際に必要なデータ配列のアクセスに必要なアドレスを生成するアドレス生成手段と、

生成されたアドレスをメモリ手段上のアドレスにデコードする手段と、

前記メモリ手段、接続手段、アドレス生成手段に対する制御命令を生成する手段とを有し、

前記制御手段は、前記メモリ手段のアクセスとして、ｎビット単位で、変調後のディジタルデータを所定の順番に配列するためデータの書込み、及び、配列中のデータに含まれる誤り訂正に必要な処理を実行する為のデータ配列の読み出しを行い、ｎ×ｍビット単位で前記インターフェイス手段へ転送データの読み出しを行う際に、ｎ×ｍビットのバス幅とすることを特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

9．請求の範囲第8項記載のバス幅可変メモリを用いたディジタル信号再生装置において、

前記復調手段へ送られるシリアルデータの復調方式が、ｋビットをｎビット（ｋ、ｎは自然数）に復調する方式であり、シリアルデータの復調手段への転送回数を示すビットクロックの単位時間当たりのクロック数と、１回の転送につきｎ×ｍビット単位の前記データ転送を行う際の単位時間当たりの転送回数の関係が、１：１／ｋ～１：１／２ｋの範囲の

関係である事を特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

１０．アクセスビットバス幅が可変な、データを一時的に記憶するメモリ手段を用いた、記録媒体からのディジタル信号を再生する再生装置の再生方法であって、

アクセス命令に呼応して、記録媒体からの読取り信号を復調し該復調データをｎビット単位でメモリ手段に書き込むためのアドレス生成、メモリアクセスを行う第１のステップと、

復調データのメモリ手段への書込みが終了した事に呼応して、誤り訂正処理のために該復調データをｎビット単位でメモリ手段から読み出すためのアドレス生成、メモリアクセスを行う第２のステップと、

誤り訂正処理が終了した事に呼応して、メモリ手段に対してはアクセスビット幅をｎ×ｍビットを指定し、誤り訂正処理後の再生データを出力するようにアドレス生成、メモリアクセスを行う第３のステップによりディジタル信号を再生することを特徴とするバス幅可変メモリを用いたディジタル信号の再生方法。

１１．請求の範囲第１０項記載のバス幅可変メモリを用いたディジタル信号の再生方法において、

前記アクセス命令は、前記再生装置のホストコンピュータとのインターフェイス手段から受付けた命令であって、

前記第３のステップにおける再生データの出力は、インターフェイス手段を介してホストコンピュータへデータ転送することを特徴とするバス幅可変メモリを用いたディジタル信号の再生方法。

１２．ディジタルデータに対し所定の信号処理を行う信号処理手段と、データを一時的に記憶するメモリ手段を有し信号処理後のディジタルデータを記録媒体に記録するディジタル信号記録装置であって、

有効アクセスビット幅をｎビットとｎ×ｍビット（ｎ、ｍは自然数）に変更可能なバス幅可変手段と、

前記メモリ手段のアクセスを行う制御手段とを有し、

該制御手段は、前記バス幅可変手段により、前記メモリ手段の有効アクセスビット幅をｎビットとｎ×ｍビットのバス幅に変更可能であり、少なくとも、前記メモリ手段に対して、ｎ×ｍビット単位でディジタルデータの書込みを行い、ｎビット単位で読出しを行うことを特徴としたバス幅可変メモリを用いたディジタル信号記録装置。

１３．請求の範囲第１２項記載のバス幅可変メモリを用いたディジタル信号記録装置において、

前記制御手段は、前記メモリ手段のアクセスとして、ｎ×ｍビット単位で、ディジタルデータを所定の順番に配列するためデータの書込み、及び、配列中のデータに含まれる誤り訂正に必要な処理を実行する為のデータ系列の読み出しを行い、ｎビット単位で転送データ系列の読み出しを行うことを特徴とするバス幅可変メモリを用いたディジタル信号記録装置。

１４．請求の範囲第１３項記載のバス幅可変メモリを用いたディジタル信号記録装置において、

前記バス幅可変手段と、メモリ手段と、少なくとも前記誤り訂正を行う訂正手段は、同一の半導体チップ上に設けることを特徴とするバス幅可変メモリを用いたディジタル信号記録装置。

１５．請求の範囲第１４項記載のバス幅可変メモリを用いたディジタル信号記録装置において、

前記メモリ手段は、一定時間で書き直し動作が必要なダイナミックなメモリを用いることを特徴とするバス幅可変メモリを用いたディジタル信号記録装置。

１６．請求の範囲第１２項記載のバス幅可変メモリを用いたディジタル信号記録装置において、

前記メモリ手段は、ｎビット幅でアクセスを行う一時記憶手段ｍ個からなり、

前記バス幅可変手段は、前記ｍ個の一時記憶手段の選択を行う第１の選択手段と、

該第１の選択手段で選択されたｎビットデータバスと、ｍ個の一時記憶手段で構成されたｎ×ｍビットデータバスの選択を行う第２の選択手段とを有することを特徴とするバス幅可変メモリを用いたディジタル信号記録装置。

１７．請求の範囲第１２項記載のバス幅可変メモリを用いたディジタル信号記録装置において、

ホストコンピュータからのｎ×ｍビット単位の転送データを受信し、前記メモリ手段へｎ×ｍビット単位でデータ転送を行うインターフェイス手段と、

該インターフェイス手段からのｎ×ｍビット単位の転送データに対し記録媒体に記録する必要のある付加データを生成し、該付加データを付加したデータをｎ×ｍビット単位で出力する付加データ生成手段と

誤り訂正処理を行うデータ配列に対し訂正符号を生成しｎビット単位で出力する訂正符号生成手段と、

変調処理を行うデータ配列をｎビット単位で入力し変調データを出力する変調手段と、

メモリ手段のデータバスに対し、前記付加データ生成手段、訂正符号生成手段、変調手段とのデータバスを選択的に接続する接続手段と、

前記付加データ生成手段、訂正符号生成手段、変調手段それぞれの処理に必要なデータ配列のアクセスに必要なアドレスを生成するアドレス

生成手段と、

生成されたアドレスをメモリ手段上のアドレスにデコードする手段と、

前記メモリ手段、接続手段、アドレス生成手段に対する制御命令を生成する手段とを有し、

前記制御手段は、前記メモリ手段のアクセスとして、ｎ×ｍビット単位でホストコンピュータから転送され、記録媒体に記録する際に必要な付加データが付加されたｎ×ｍビット単位のディジタルデータを、所定の順番に配列するためデータの書込みを行う際に、ｎ×ｍビットのバス幅とし、ｎビット単位で、配列中のデータに含まれ誤り訂正符号の付加を実行するのに必要なデータ配列の読み出し、及び、変調処理を行う変調データのデータ配列に対する読み出しを行う際に、ｎビットのバス幅とすることを特徴とするバス幅可変メモリを用いたディジタル信号記録装置。

１８．請求の範囲第１７項記載のバス幅可変メモリを用いたディジタル信号記録装置において、

前記アドレス生成手段は、前記付加データ生成手段からのデータ書込み、前記訂正符号生成手段へのデータ読み出し、前記変調手段へのデータ読み出しを行う時、それぞれの処理の対象のデータ配列に対しｎ×ｉビット（ｉは自然数）と（ｎ×ｍ）×ｊビット（ｊは自然数）を単位とするバンク単位でアクセスを行うために、１バンク単位の縦方向のアドレスと横方向のアドレス、及び、各バンクにおける、縦方向のバンクアドレス、横方向のバンクアドレスをそれぞれ生成することを特徴とするバス幅可変メモリを用いたディジタル信号記録装置。

１９．請求の範囲第１７項記載のバス幅可変メモリを用いたディジタル信号記録装置において、

前記変調手段の変調方式が、ｎビットをｋビット（ｎ、ｋは自然数）

に変調する方式であり、１回の転送につきｎ×ｍビット単位の前記インターフェイス手段からの前記データ転送を行う際の単位時間当たりの転送回数と、前記変調手段からのシリアルデータの転送回数を示すビットクロックの単位時間当たりのクロック数の関係が、１：ｍｋ～１：２ｍｋの範囲の関係である事を特徴とするバス幅可変メモリを用いたディジタル信号記録装置。

２０．アクセスビットバス幅が可変な、データを一時的に記憶するメモリ手段を用いた、ホストコンピュータからの転送データを記録媒体に記録する記録装置の記録方法であって、

ホストコンピュータからの記録開始に呼応して、ｎ×ｍビット単位のホストコンピュータからの転送データに対し記録媒体に記録する必要のある付加データを付加したデータをｎ×ｍビット単位でメモリ手段に書き込むためのアドレス生成、メモリアクセスを行う第１のステップと、

該付加データのメモリ手段への書込みが終了した事に呼応して、メモリ手段に対しアクセスビット幅をｎビットに指定し、誤り訂正符号を付加する処理のために前記付加データをｎビット単位でメモリ手段から読み出すためのアドレス生成、メモリアクセスを行う第２のステップと、

誤り訂正符号付加後データのメモリ手段への書込みが終了した事に呼応して、メモリ手段に対しアクセスビット幅をｎビットに指定し、変調処理のためのメモリ手段から読み出すためのアドレス生成、メモリアクセスを行う第３のステップにより変調処理後のデータを記録媒体に記録することを特徴とするバス幅可変メモリを用いたディジタル信号の記録方法。

２１．記録媒体からの読み取り信号を復調する復調手段と、データを一時的に記憶するメモリ手段と、復調後のデータを誤り訂正処理する誤り訂正手段とを有し、誤り訂正処理により再生された再生データを読み出

しデータ転送を行うディジタル信号再生装置において、

前記復調手段へ送られるシリアルデータの復調方式が、ｋビットをｎビット（ｋ、ｎは自然数）に復調する方式であり、

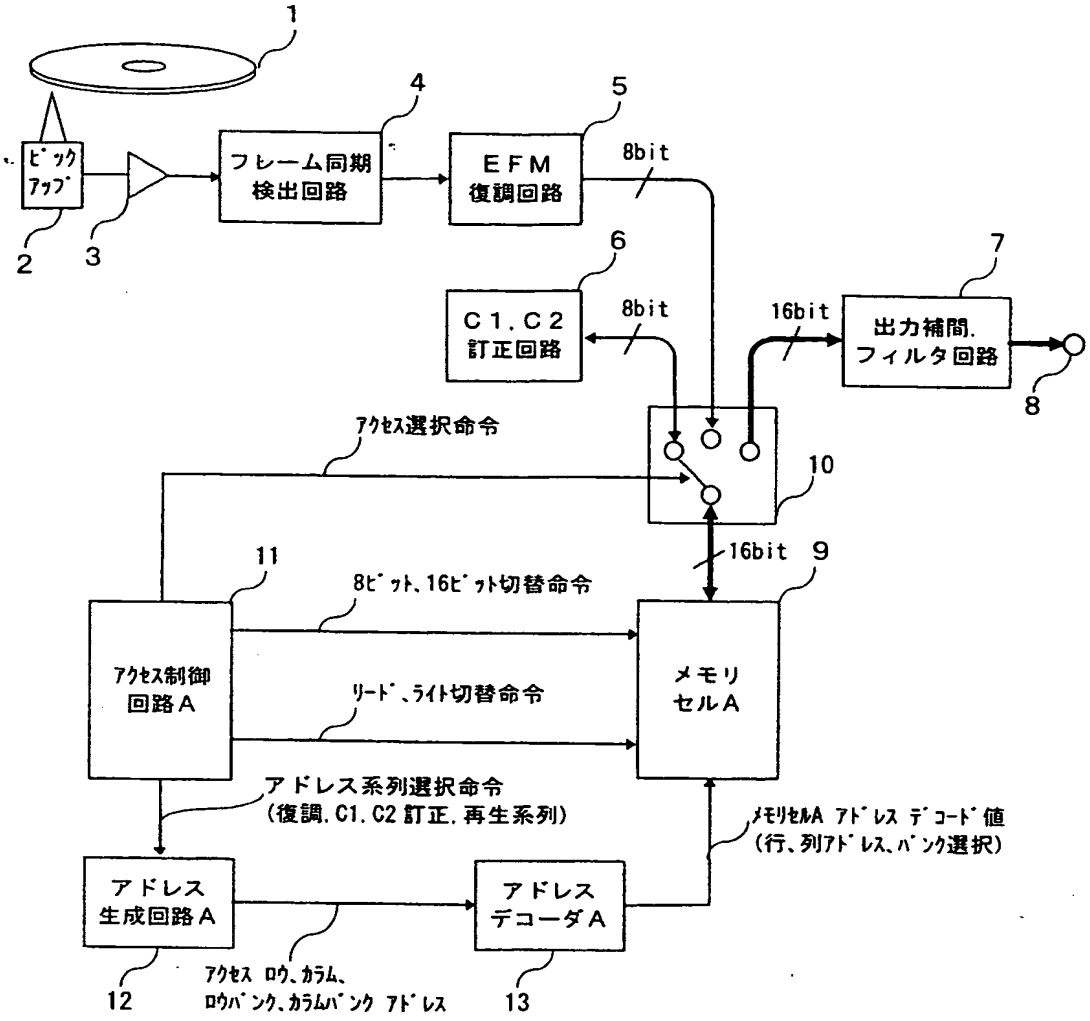
前記復調手段へのシリアルデータの転送回数を示すビットクロックの単位時間当たりのクロック数と、１回の転送につきｎ×ｍビット単位（ｍは２以上の整数）の前記データ転送を行う際の単位時間当たりの転送回数の関係が、１：１/ｋ～１：１/２ｋの範囲の関係であることを特徴とするディジタル信号再生装置。

２２．記録媒体からの読み取り信号を復調する復調手段と、復調後のデータを誤り訂正処理する誤り訂正手段と、データを一時的に記憶するメモリ手段と、誤り訂正処理により再生された再生データを読み出しデータ転送を行うディジタル信号再生装置において、

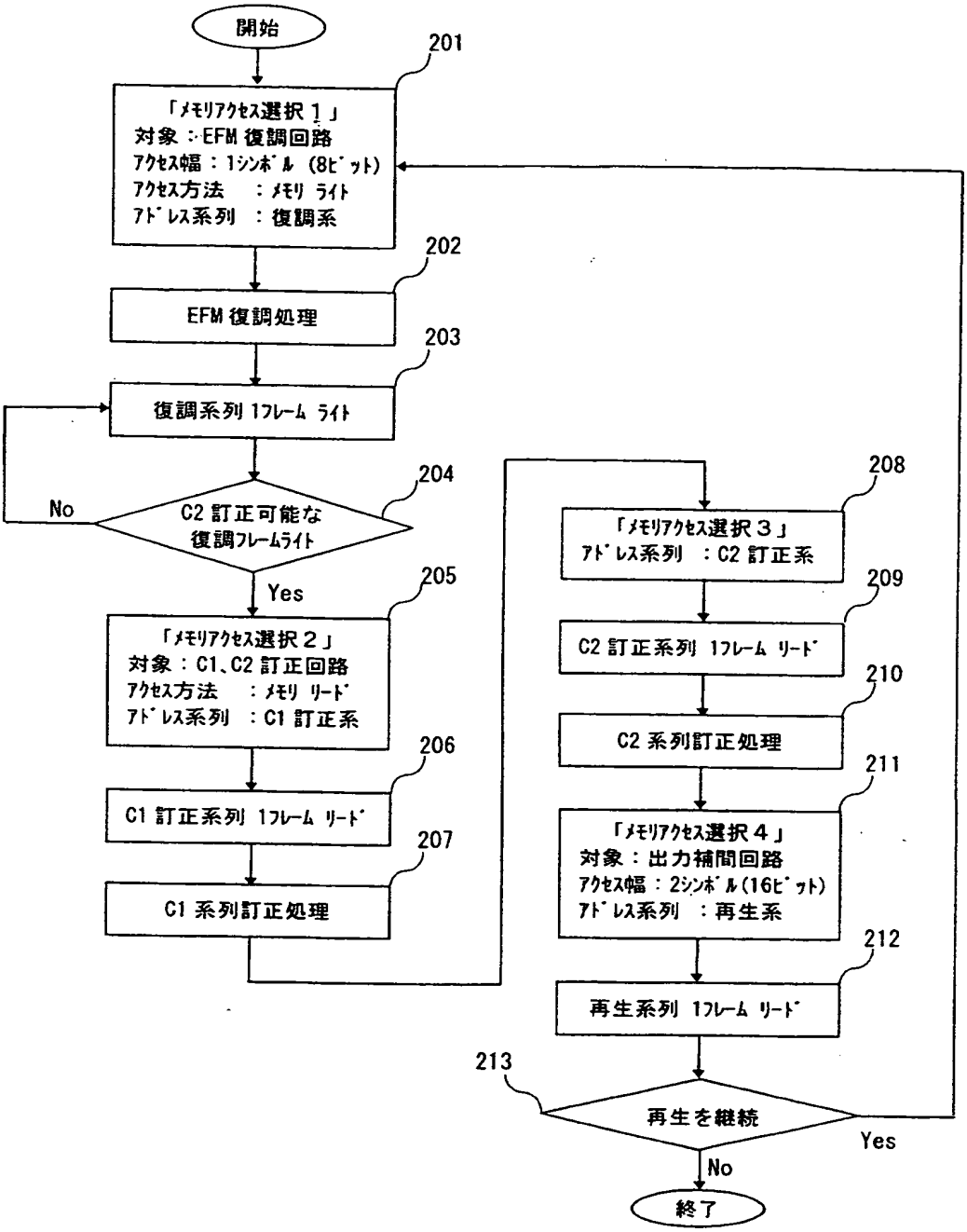
さらに、有効アクセスビット幅をｎビットとｎ×ｍビット（ｎは自然数、ｍは２以上の整数）に変更可能なバス幅可変手段を有し、

前記メモリ手段のアクセスバスは、前記バス幅可変手段を介して有効アクセスビット幅を可変な構成とし、かつ、前記復調、誤り訂正処理後の前記データ転送の有効アクセスビット幅と一致させたことを特徴とするバス幅可変メモリを用いたディジタル信号再生装置。

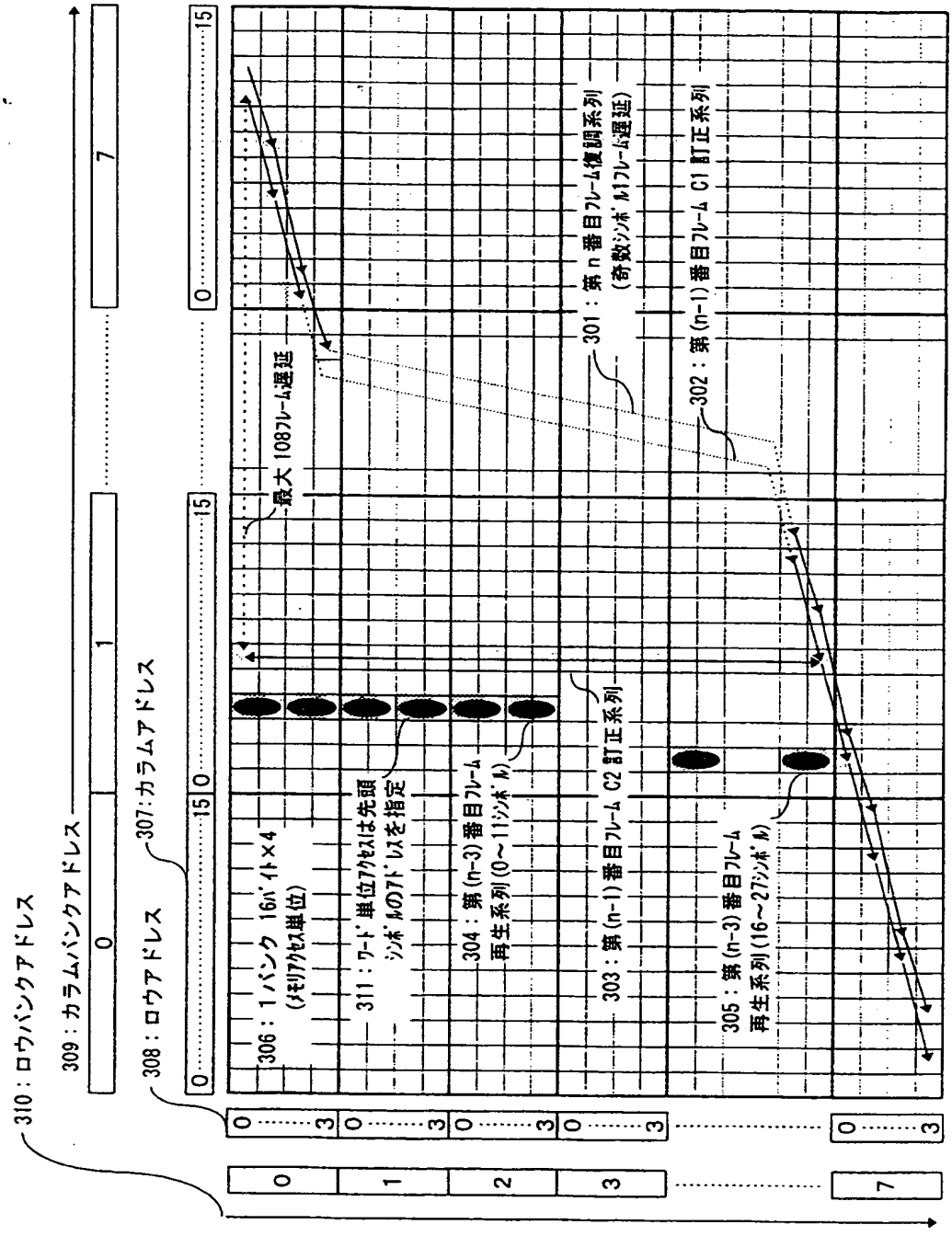
第１図



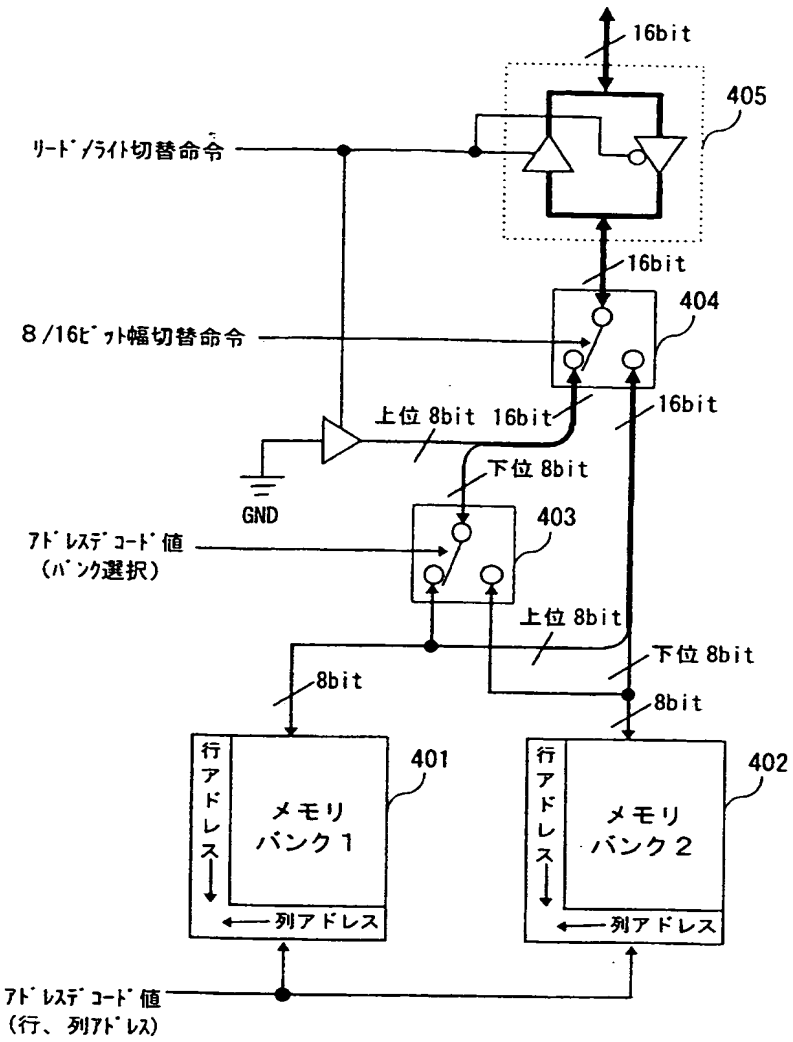
第２図



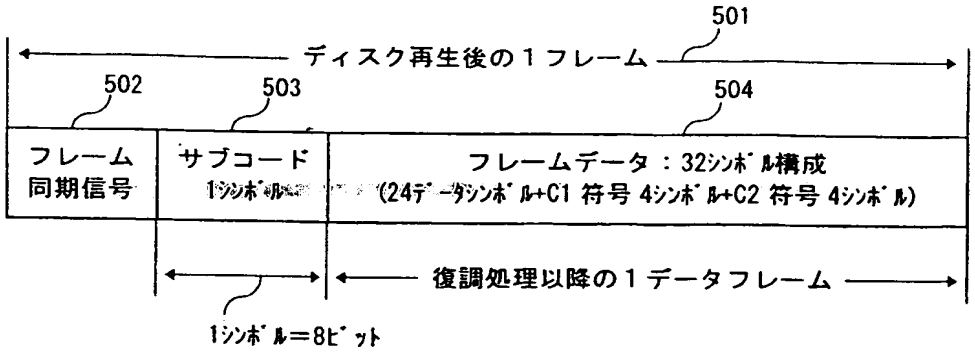
第３図



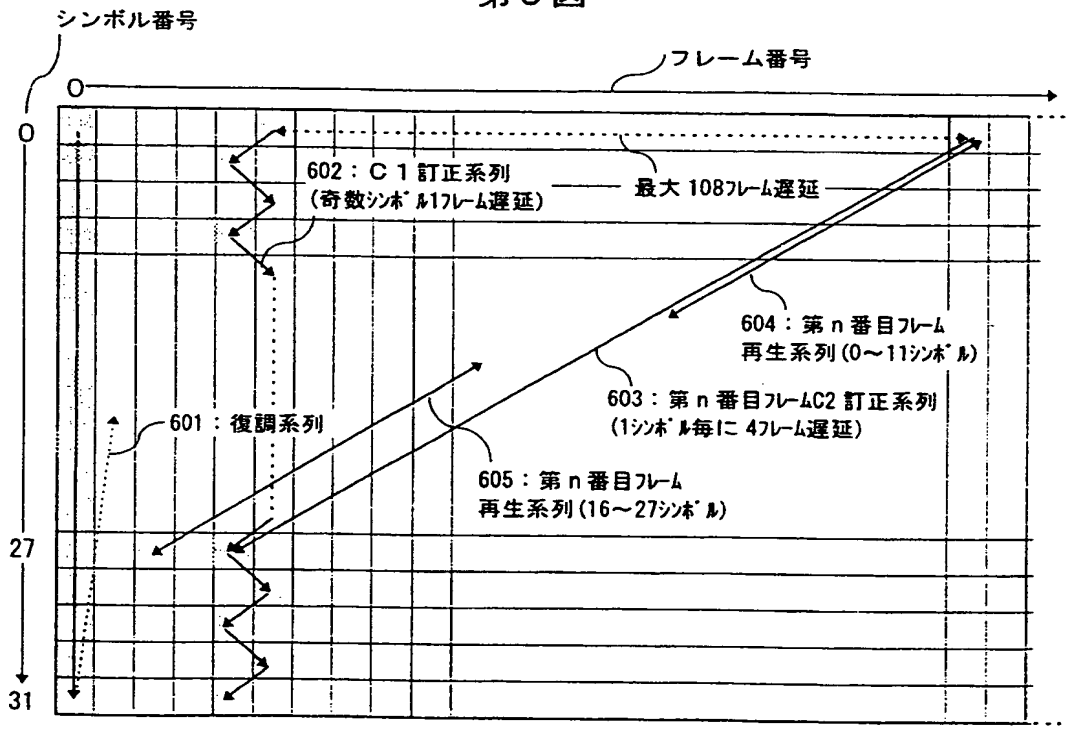
第４図



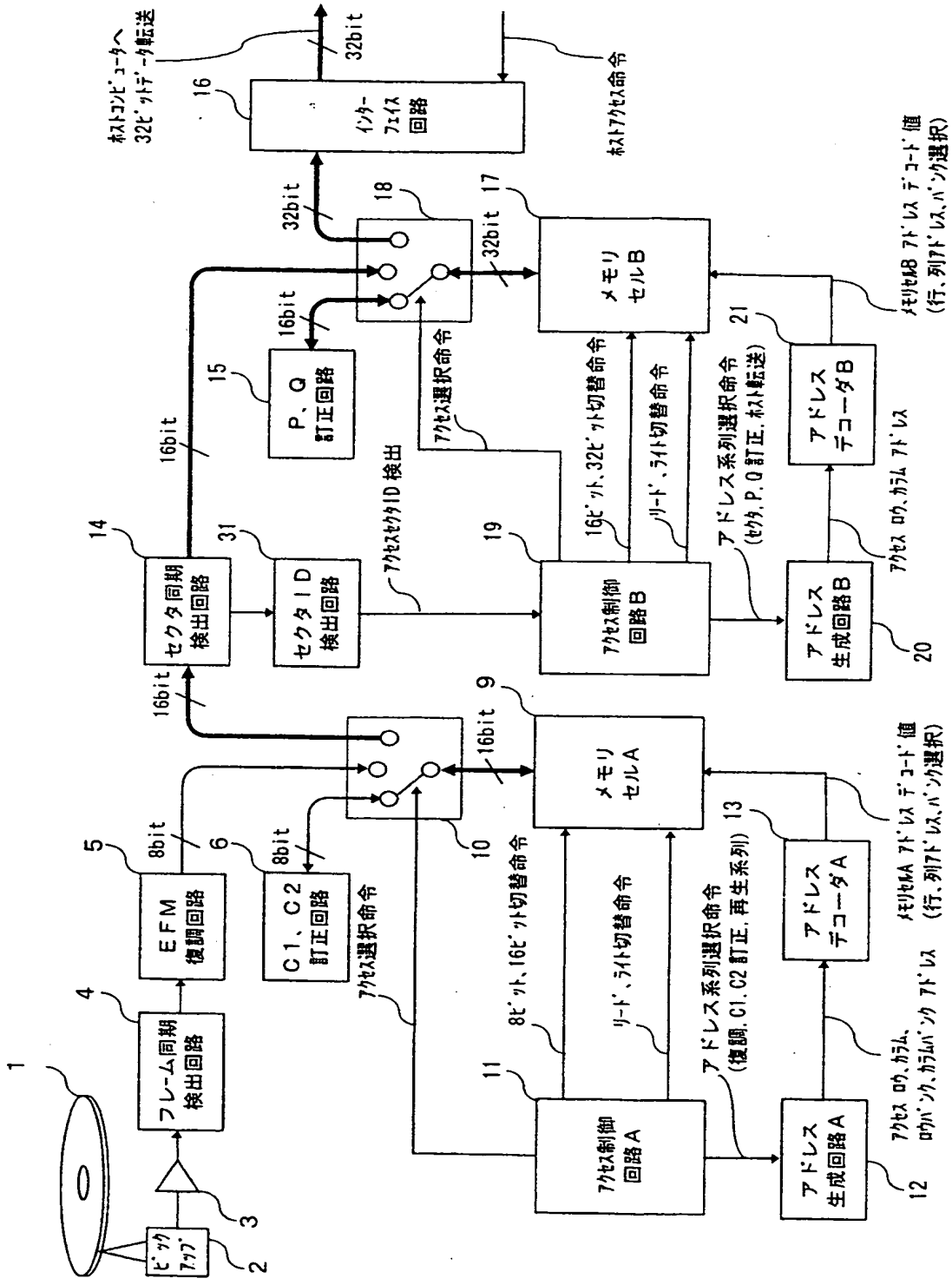
第５図



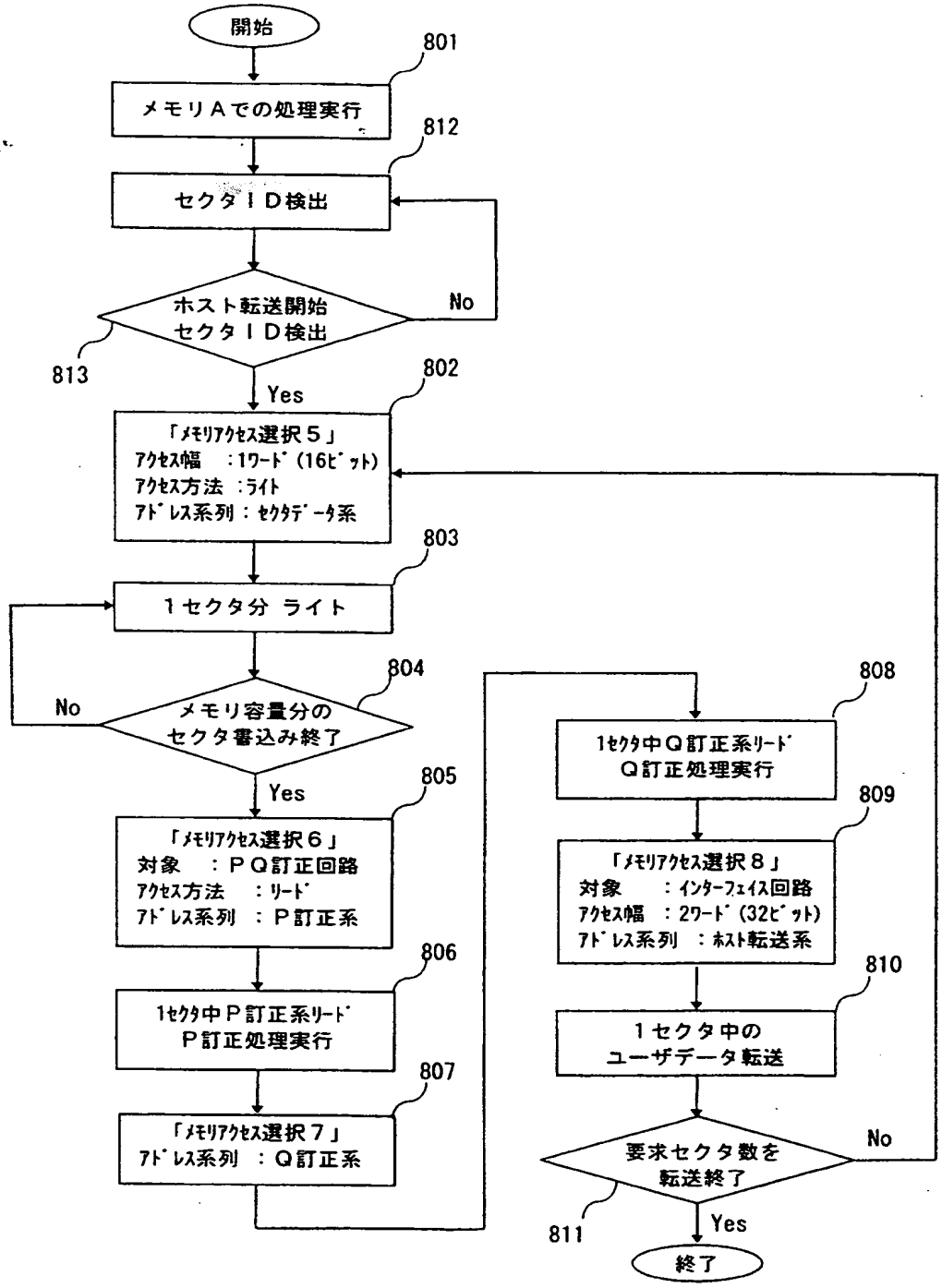
第６図



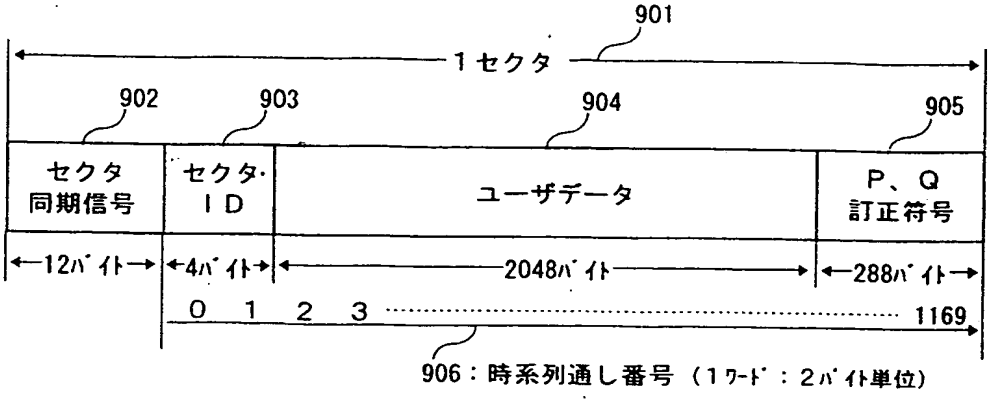
第7図



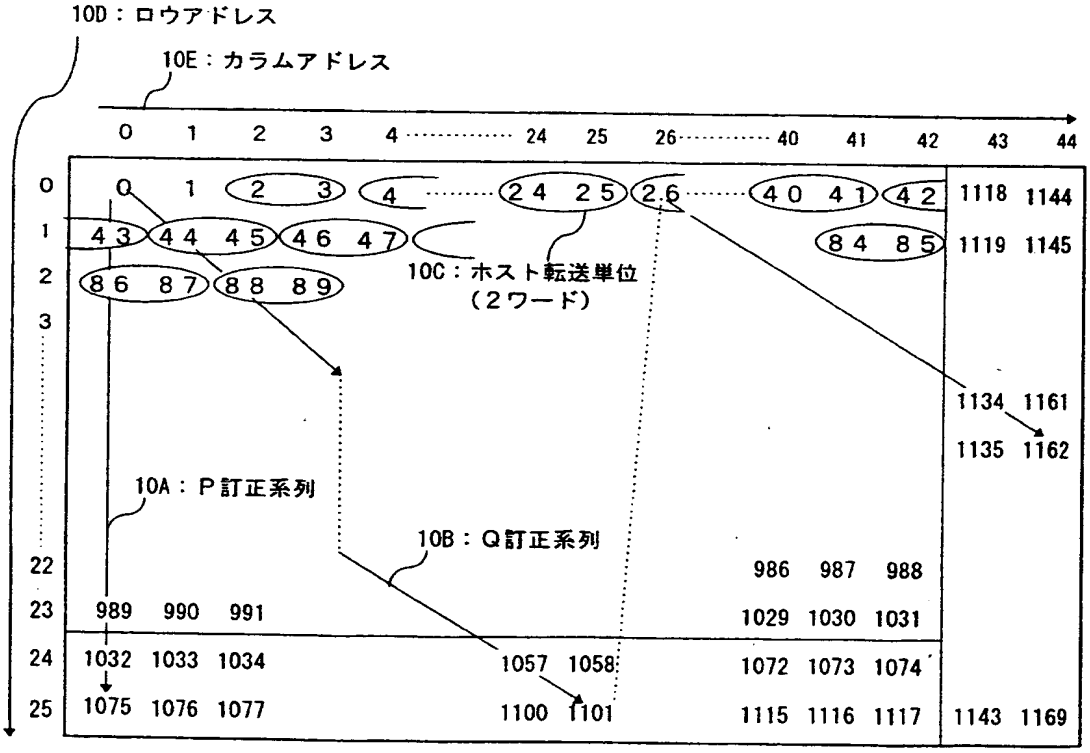
第８図



第９図



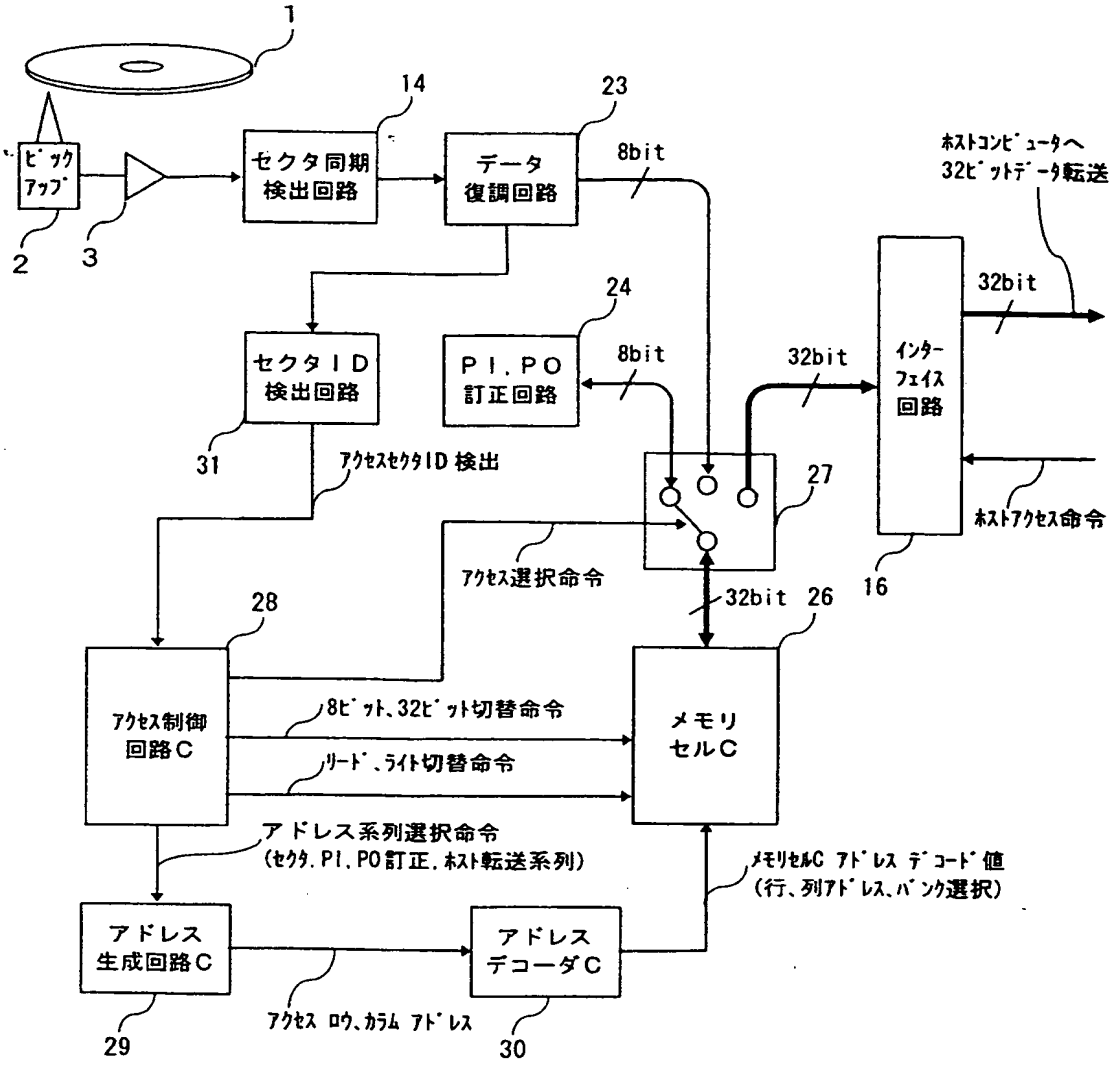
第１０図



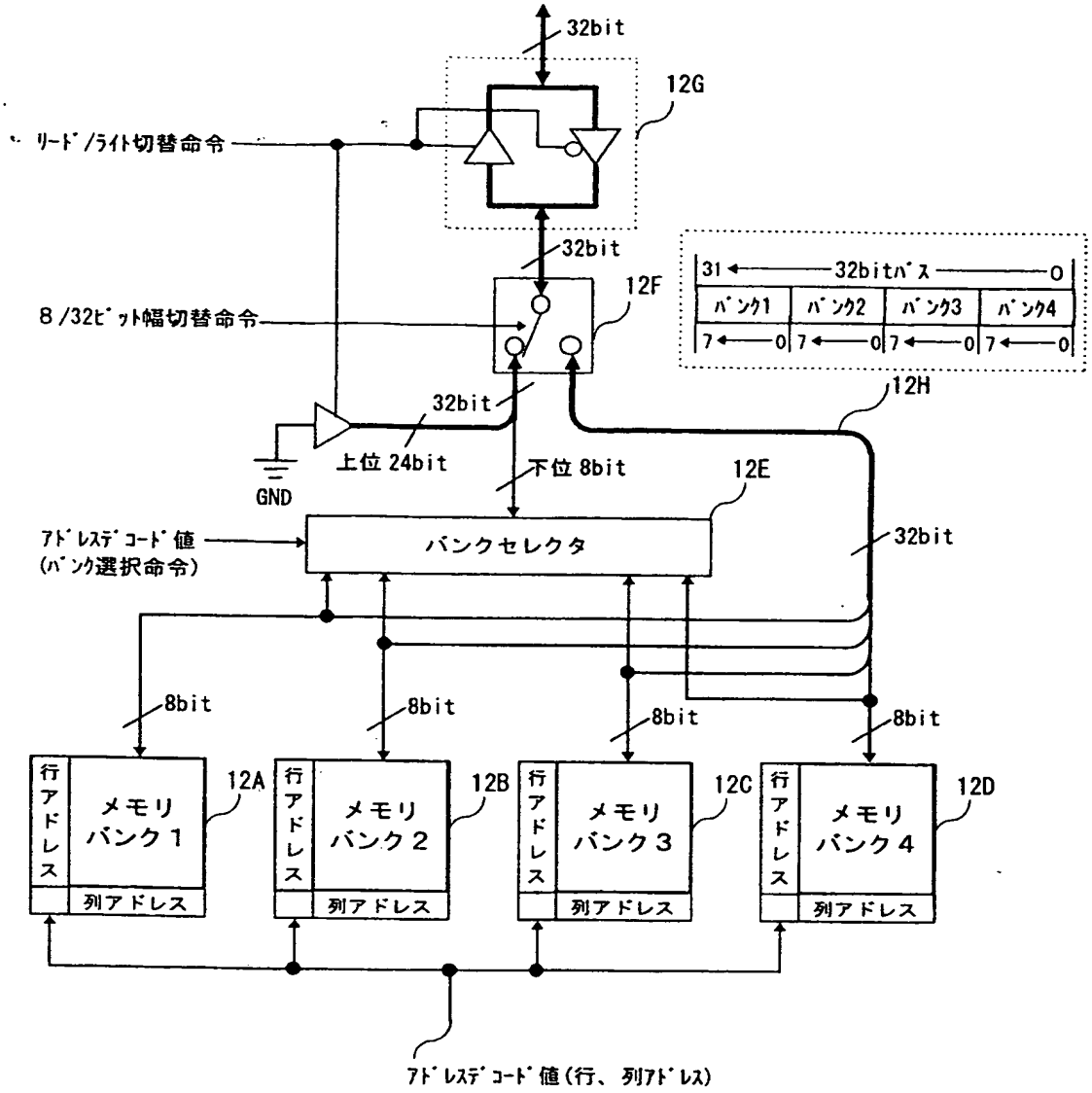
＊番号は時系列データの通し番号。（１ワード単位）

＊０～1031：データ、1032～1117：訂正符号Ｐ、1118～1169：訂正符号Ｑ

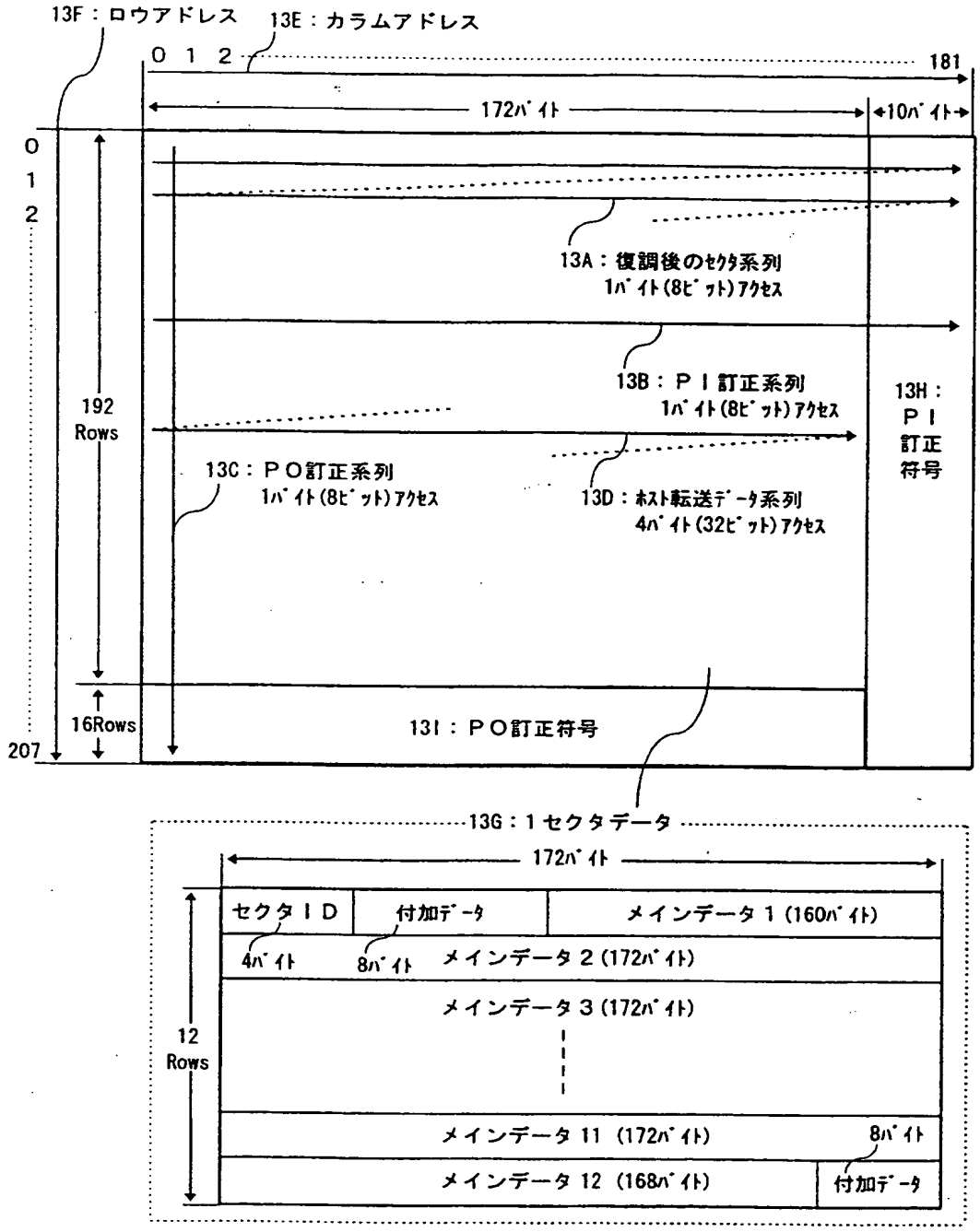
第１１図



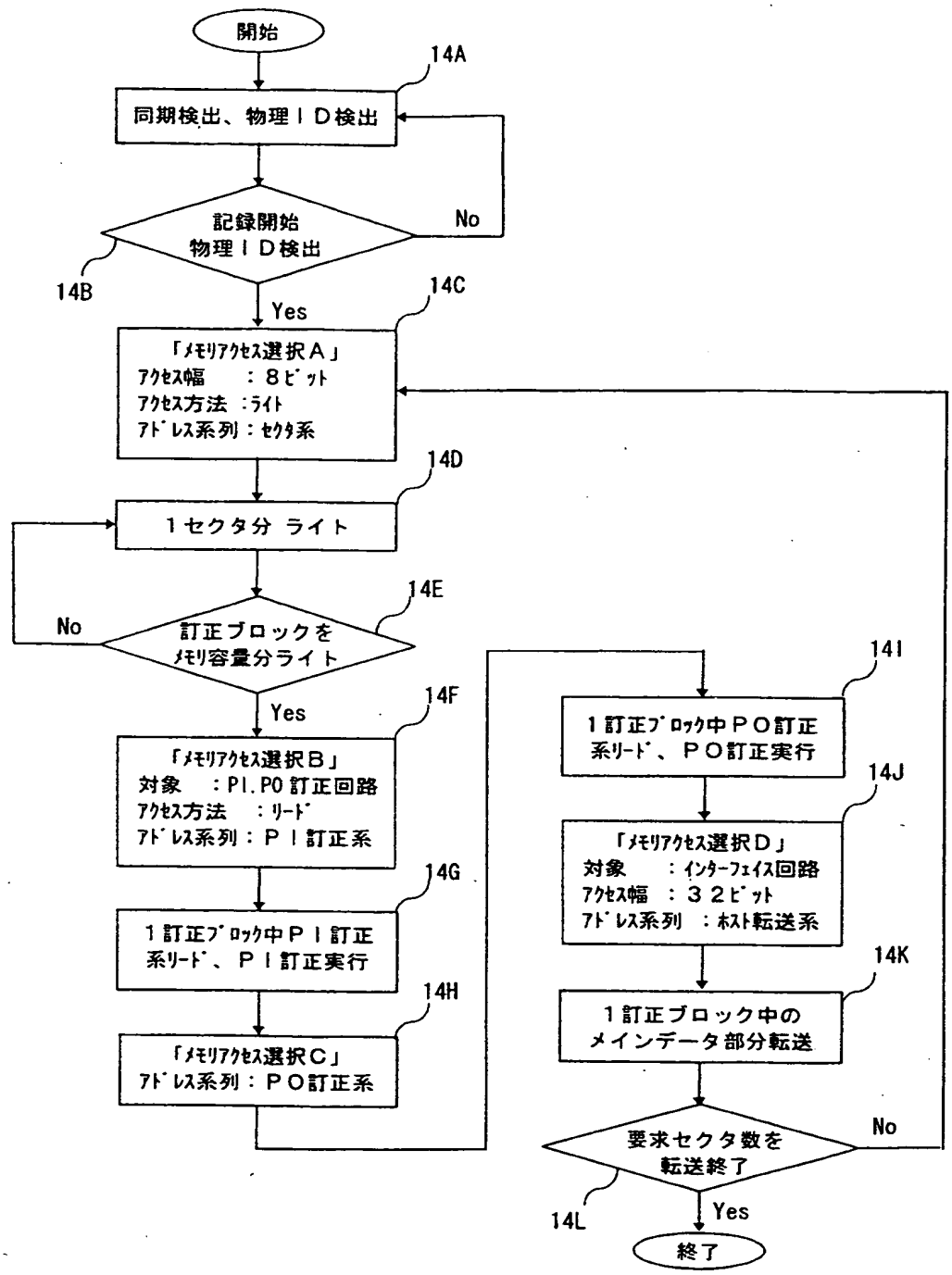
第１２図



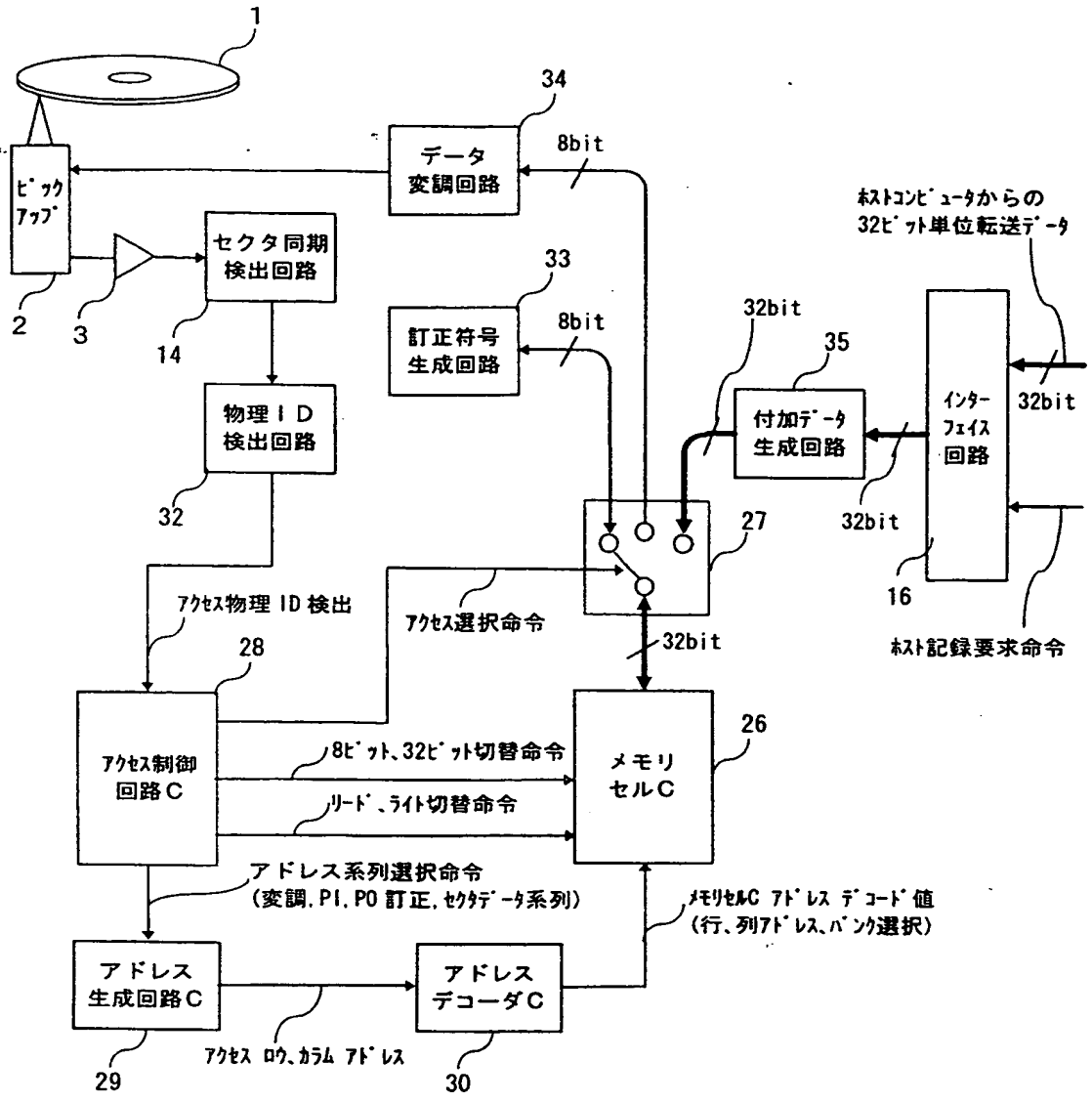
第１３図



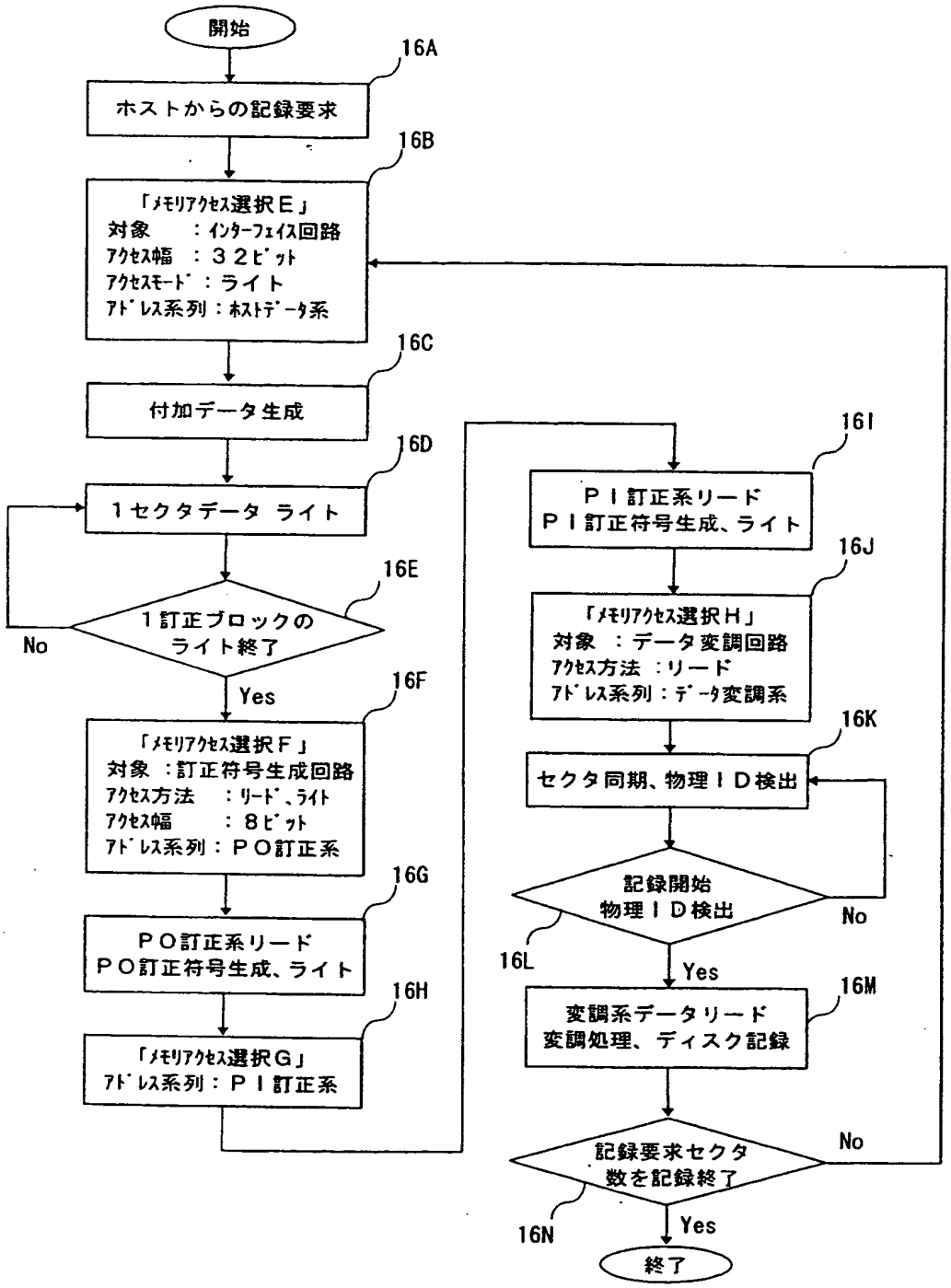
第１４図



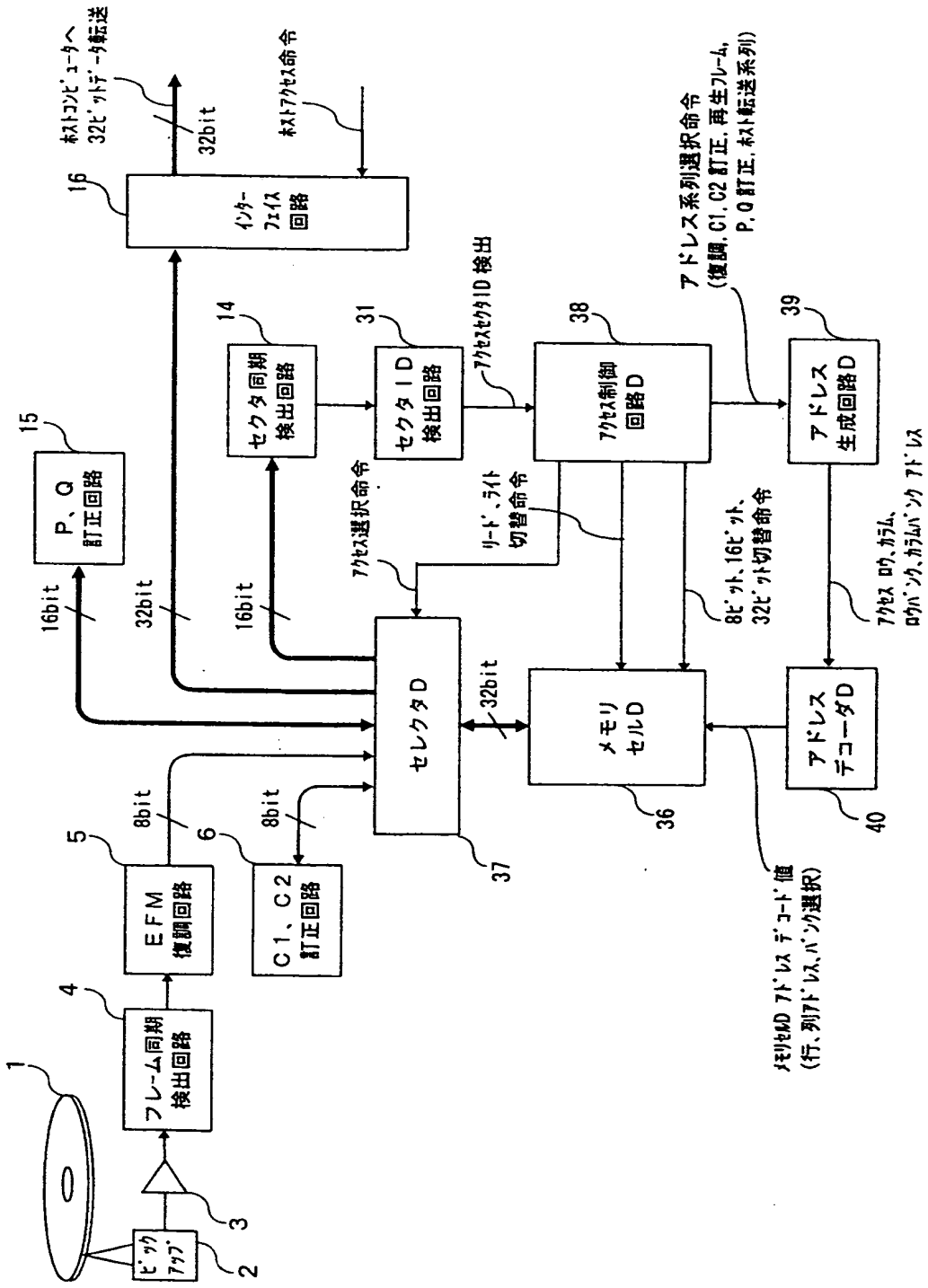
第１５図



第１６図



第１７図



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP97/00910

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl^6 G11B20/10, G11C7/00, H03M13/22

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int. Cl^6 G11B20/10, G11C7/00, H03M13/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1940 - 1997
Kokai Jitsuyo Shinan Koho 1971 - 1997
Toroku Jitsuyo Shinan Koho 1994 - 1997
Jitsuyo Shinan Toroku Koho 1996 - 1997

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 5-12883, A (Nippon Steel Corp.), January 22, 1993 (22. 01. 93)(Family: none)	1 - 22
A	JP, 7-271752, A (NEC Home Electronics Ltd.), October 20, 1995 (20. 10. 95)(Family: none)	1 - 22

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
June 16, 1997 (16. 06. 97)	June 24, 1997 (24. 06. 97)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

国際調査報告

国際出願番号　ＰＣＴ／ＪＰ９７／００９１０

A.　発明の属する分野の分類（国際特許分類（ＩＰＣ））

Ｉｎｔ．Ｃｌ⁶　Ｇ１１Ｂ２０／１０、Ｇ１１Ｃ７／００、Ｈ０３Ｍ１３／２２

B.　調査を行った分野

調査を行った最小限資料（国際特許分類（ＩＰＣ））

Ｉｎｔ．Ｃｌ⁶　Ｇ１１Ｂ２０／１０、Ｇ１１Ｃ７／００、Ｈ０３Ｍ１３／２２

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	１９４０－１９９７年
日本国公開実用新案公報	１９７１－１９９７年
日本国実用新案登録公報	１９９６－１９９７年
日本国登録実用新案公報	１９９４－１９９７年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C.　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
A	ＪＰ，５－１２８８３，Ａ（新日本製鐵株式会社），２２．１月．１９９３（２２．０１．９３）（ファミリーなし）	１－２２
A	ＪＰ，７－２７１７５２，Ａ（日本電気ホームエレクトロニクス株式会社），２０．１０月．１９９５（２０．１０．９５）（ファミリーなし）	１－２２

☐ Ｃ欄の続きにも文献が列挙されている。

☐ パテントファミリーに関する別紙を参照。

＊　引用文献のカテゴリー
「Ａ」特に関連のある文献ではなく、一般的技術水準を示すもの
「Ｅ」先行文献ではあるが、国際出願日以後に公表されたもの
「Ｌ」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「Ｏ」口頭による開示、使用、展示等に言及する文献
「Ｐ」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「Ｔ」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「Ｘ」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Ｙ」特に関連のある文献であって、当該文献と他の１以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「＆」同一パテントファミリー文献

国際調査を完了した日 １６．０６．９７	国際調査報告の発送日 24.06.97
国際調査機関の名称及びあて先 日本国特許庁（ＩＳＡ／ＪＰ） 郵便番号１００ 東京都千代田区霞が関三丁目４番３号	特許庁審査官（権限のある職員） 小松　正　印　5D　7736 電話番号　０３－３５８１－１１０１　内線　３５５１

様式ＰＣＴ／ＩＳＡ／２１０（第２ページ）（１９９２年７月）

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(51) INT CL[5]
G06F 1/32

(52) UK CL (Edition K)
G4A ASX

(56) Documents cited
US 4698748 A

(58) Field of search
UK CL (Edition K) G4A ASX
INT CL[5] G06F

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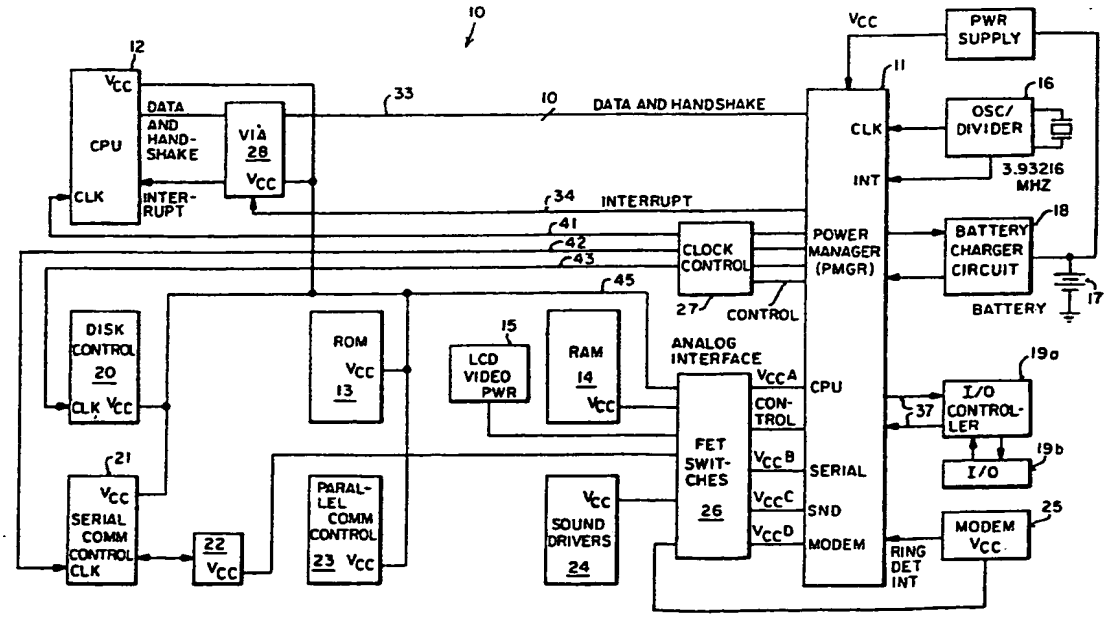
(54) Power management for a portable computer

(57) A power manager (PMGR) within a portable laptop computer provides power (via 26) and clocking control (via 27) to various units within the computer in order to conserve battery power. Transistor switches controlled by the power manager control the distribution of power and clock signals to the various units within the computer. The power manager includes a software routine for continually monitoring various units and when certain units are either not needed and/or not currently in use, power and/or clock signals are removed from a given unit, and the computer can be switched between three modes viz. normal, slow and sleep.

FIG 1



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

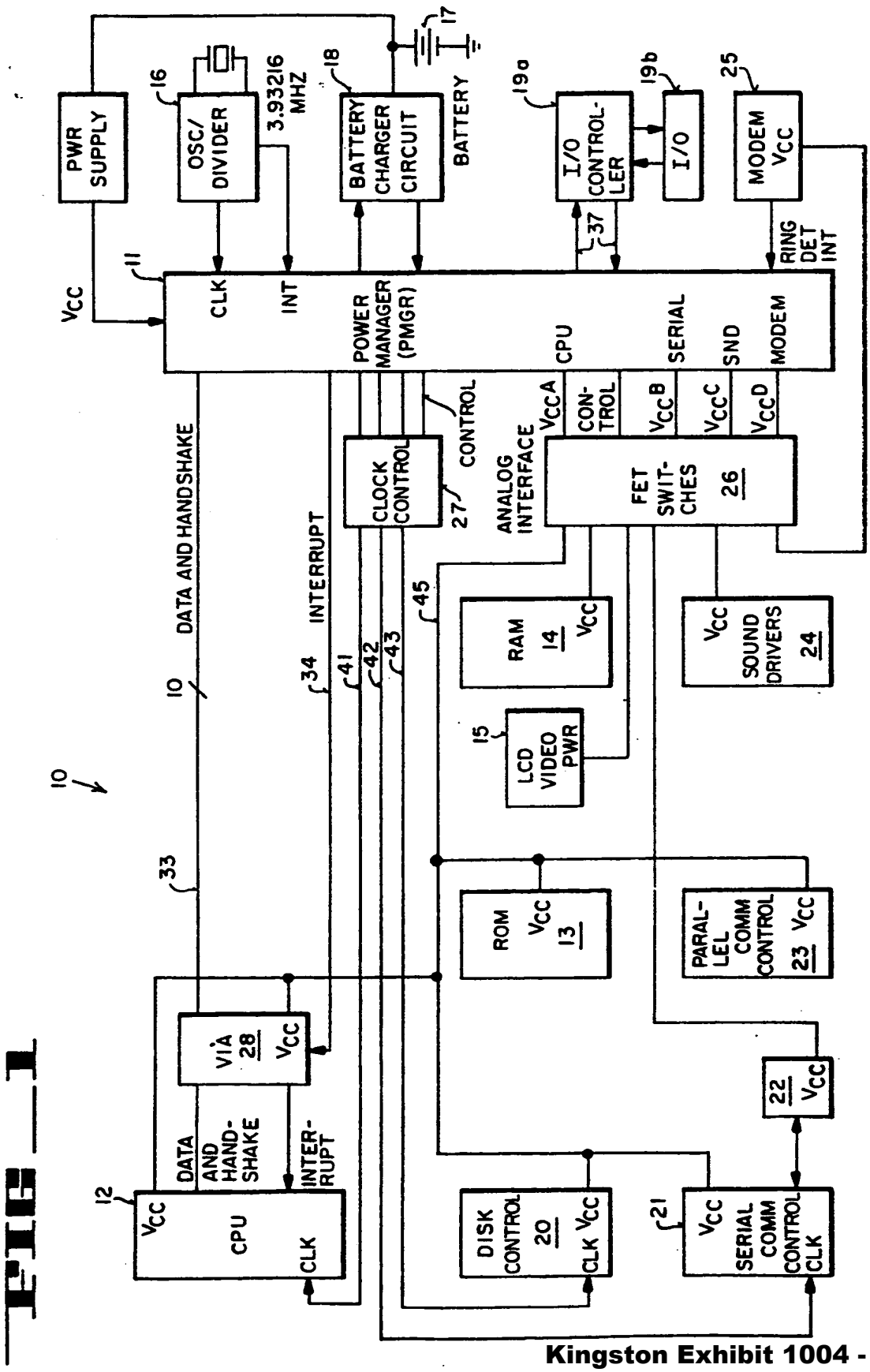


FIG. 1

FIG 2

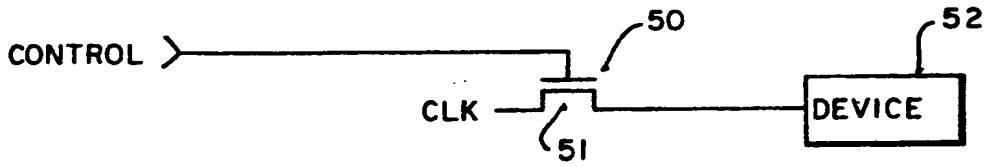
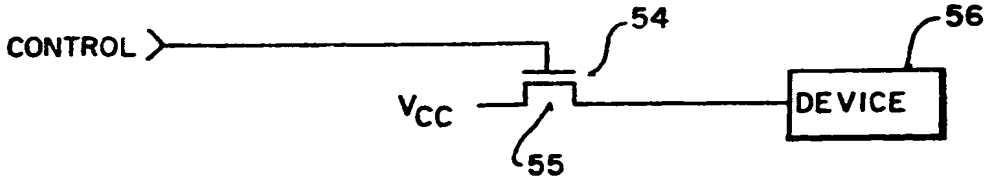


FIG 3



POWER MANAGEMENT FOR A LAPTOP COMPUTER.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power distribution scheme in a portable computer and, more specifically, to power management in a laptop computer.

2. Prior Art

Power consumption in an electronic device is always a significant concern and a power supply must be designed to adequately power the device. Aside from the capability of the power supply to provide ample power to power the corresponding device, heat dissipation, physical size, weight, efficiency, and other related characteristics are paramount in designing or selecting the power source. These characteristics become exceptionally critical when the device the power supply is to support is a self-sufficient portable unit.

In many portable units, a self-supporting power source, such as a battery, is used to provide the power when the unit is decoupled from its main or external power source, such as 110 Volt AC (ordinary house current). Typically a battery is used to provide the independent and portable power source. In some instances the battery functions as an auxiliary power source to maintain certain critical circuits active, such as keeping the memory alive to retain any information stored in the memory. In other instances, the battery functions as the main power source to fully power the device.

In the area of information processing, miniaturization of processing devices has permitted the portability of computing devices. One of the first such portable processing devices was a hand held calculator, wherein the calculator operated from a battery power source and could easily be carried about by the user. The battery would power all of the functions of the calculator

and the user could readily transport the calculator without any attachment to an external power source. The batteries were either replaced or recharged. The earliest calculators simply had an on/off state in which full power was available during the on state and the power was completely shut off during the off state. Because of the volatile nature of many early semiconductor memories, information stored in such volatile memories were lost when the calculator was turned off. Subsequent calculators attempted to incorporate nonvolatile memory, or in the alternative, standby power was provided to such a memory when the device was turned off, so that the memory retained whatever information was present. More advanced schemes were devised to monitor various functions, so that power was removed from various elements when those elements were not needed. Further, a time-out scheme was devised to put the calculator in a stand-by mode, such as when a key was not depressed after a certain time period, in order to preserve power. All of these features were devised primarily to extend the time period that the device could operate from its internal power source.

When the processing technology was expanded beyond a simple calculator to encompass personal desk top computers, additional constraints were placed to power consumption and management control schemes. Aside from the additional circuitry, additional memory devices consumed considerable amounts of power. These memory devices include semi-conductor devices, such as read-only memories (ROMs) and random-access memories (RAMs) which include volatile and non-volatile memories, floppy disk drives and hard disk drives and other magnetic media. Also, additional power is required to power the display unit which typically includes a viewing screen. Various schemes were devised to monitor and control the power distribution during on/off states.

However, as the personal desk top computer systems are made portable, it is desirable to provide a computer which contains a fully contained power source so that the computer is completely portable. These self - sufficient computer systems are typically referred to as laptops (because of the small physical size and light weight) and are designed to operate for a certain number of hours from its internal power source, which is typically a battery. Although a variety of the portable calculator technology can be implemented within such a laptop, additional constraints are placed in that the additional circuitry, memory, viewing screen and any peripheral devices attached to the system will necessarily consume additional power. In order to extend the self-sustaining time period of these laptops while keeping the battery size and weight to a minimum, a sophisticated power management scheme is required to provide power only to those circuits and devices which require such power and to remove power, or at least to make a given circuit enter a low power consumption mode, when that circuit is not needed. The management scheme must also continually monitor the various circuits and devices in order that power can be applied immediately to activate such circuits and devices when needed.

The present invention provides for such a power management apparatus for a laptop computer in order to extend the self-sustaining time period so that the laptop computer can operate for an extended period of time once external power is disconnected.

3. Prior Art References

A number of prior art references are known for monitoring and controlling the consumption of power to a device or to a portion of a device including a means of providing a timeout when user interaction has not occurred for a given time period. However, these references pertain to the simpler calculator technology or to portions of a computer system and fail to disclose the

sophisticated power management scheme for a laptop of the present invention. The references are:

1. U.S. Patent No. 4,019,068, issued April 19, 1977, for Low Power Output Disable Circuit For Random Access Memory;

2. U.S. Patent No. 4,074,351, issued February 14, 1978 for Variable Function Programmed Calculator;

3. U.S. Patent No. 4,151,611, issued April 24, 1979 for Power Supply Control System For Memory Systems;

4. U.S. Patent No. 4,293,927, issued October 6, 1981 for Power Consumption Control System For Electronic Digital Data Processing Devices;

5. U.S. Patent No. 4,279,020, issued July 14, 1981 for Power Supply Circuit For A Data Processor;

6. U.S. Patent No. 4,381,552, issued April 26, 1983 for Standby Mode Controller Utilizing Microprocessor;

7. U.S. Patent No. 4,409,665, issued October 11, 1983 for Turn-Off-Processor Between Keystrokes;

8. U.S. Patent No. 4,611,289, issued September 9, 1986 for Computer Power Management System;

9. U.S. Patent No. 4,615,005, issued September 30, 1986 for Data Processing Apparatus With Clock Signal Control By Microinstruction For Reduced Power Consumption And Method Therefor; and

10. U.S. Patent No. 4,712,196, issued December 8, 1987 for Data Processing Apparatus.

SUMMARY OF THE INVENTION

The present invention describes a power manager for use in a laptop computer. The laptop computer is a fully self-sufficient computer which is powered by an internal battery when the computer is disconnected from an external power source. Because power conservation is paramount to sustain the computer as long as possible from the internal battery, a power manager is provided to monitor and control various circuit operations. Various units of the computer, including peripheral units, generally function equivalently to well-known personal desktop computers. However, the power source to the various devices are controlled by the power manager and a plurality of transistor switches are used to switch the power source to the various devices. The operation of these switches is controlled by the power manager. Additionally, various clock signals are also coupled through switches which are controlled by the power manager so that the clock signals can be disconnected from certain units of the computer.

The power manager continually monitors various circuit functions such that devices not in use have their power sources or clock signals disconnected in order to deactivate devices to conserve battery power. The removal of clock signals from those units having clock control places these various units into an inactive state. However, because power is still applied to these units, various internal states retain their current state until the clock signal is restored.

The power manager is capable of operating in one of three modes of operation. In a first mode the computer operates in a normal active mode where most of the units are active at all times and/or some of the other units are caused to be made active when needed. A second state is a sleep state in which the computer enters into an inactive state and the power manager continues to monitor various circuit conditions. When a certain predetermined

condition occurs, it causes the computer to awake from its sleep state. A third state is an intermediate state in which the power manager controls the frequency of the clock signals to be decreased such that the power consumption drops by approximately 25-30% from the normal active mode.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit block diagram of the various units of the laptop computer and showing power lines, clock signal lines and control lines pertaining to the power management scheme of the present invention.

Figure 2 is a circuit schematic diagram showing an example of a transistor switch utilized to control the switching of a clock signal to a given device.

Figure 3 is a circuit schematic diagram showing an example of a transistor switch utilized to control the switching of power to a given device.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

A power management system for a laptop computer is described. In the following description, numerous specific details are set forth, such as specific circuits, devices, etc., in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known circuits and signal lines have not been described in detail in order not to unnecessarily obscure the present invention.

Referring to Figure 1, an architecture for a portable computer 10 is shown, including the power manager (PMGR) 11 of the present invention. Although computer 10 can be of a variety of computers, computer 10 of the present invention is a portable computer and, more specifically, a laptop computer which is capable of operating without an external power source. Aside from the PMGR 11, computer 10 is comprised of a CPU 12, read-only memory (ROM) 13, random-access memory (RAM) 14, liquid crystal display (LCD) unit 15 which includes a viewing screen and associated video circuitry, crystal controlled clock and oscillator 16, a battery 17, a battery charger circuit 18 and an input/output (I/O) unit 19 which includes an I/O controller 19a and at least one I/O device 19b. These components are typically present in most desktop or portable computer systems. Computer 10 of the present invention further includes a disk controller 20, a serial communication controller 21 and its drivers 22, a parallel communications controller 23, sound circuit and drivers 24, and a modem 25. It is to be appreciated that although units 20-25 are included within computer 10 that these devices are typically a design choice and the computer 10 can readily operate as a functioning computer without the presence of these units.

Several additional units are included within computer 10 to operate with the PMGR unit 11. Analog interface unit 26, clock control unit 27 and an internal interface unit, referred to as a via unit 28, are included to function in conjunction with the PMGR 11. It is to be appreciated that units 12-25 are devices used in prior art computers and such description and operation of these units are not included herein. Units 12-25, except for unit 17 and 18, are available with the Macintosh™ brand computers of Apple Computer Inc., of Cupertino, California.

In functional terms, CPU 12 is the main processing unit for computer 10 and in the preferred embodiment is a 68000 based (part numbers 68000, 68020 and 68030) processor manufactured by Motorola Corporation. ROM 13 is used to store the operating system of the computer 10 as well as other proprietary programs, such as file directory routines. RAM 14 is utilized as the internal memory of the computer for accessing of data. The LCD display 15 with its associated video circuitry provides for the presentation of a display on a viewing screen. The crystal operated clock 16 provides for the necessary timing reference signals which are needed for the operation of computer 10. The battery 17 powers computer 10, permitting computer 10 to be a fully portable unit. Battery charger circuit 18 monitors the level of the battery 17 as well as charging the battery 17 when computer 10 is coupled to an external power source such as 110 Volts AC.

The I/O unit 19 interfaces with various I/O devices, such as keyboards and cursor control devices, such as a "mouse" or a trackball. The disk controller unit 20 is used to access a disk storage medium, such as a floppy disk. In computer 10, a hard disk is coupled and accessed by the parallel communications controller 23. The serial communication controller 21 and its drivers 22 are utilized to provide serial communication, such as supporting a RS-232 protocol. The sound circuits and drivers of sound unit 24 are utilized to

generate various audio signals from computer 10. Modem 25 is typically an external device, however, in this instance it is included within computer 10 to provide full modem capability, in order that the portable computer 10 has capabilities of interfacing with telecommunication lines at various remote locations.

The power management apparatus of the present invention is comprised of PMGR 11, analog interface unit 26, clock control unit 27 and via unit 28. Functionally, PMGR 11 is an intelligent assistant to the CPU 12, wherein PMGR 11 monitors the state of charge of battery 17, controls the power consumption of the various subsystems, includes a real time clock which frequency is determined by the clock circuit 16, interfaces to the internal modem 25, as well as an interface to the I/O peripheral devices 19b through I/O controller19a. It is to be appreciated that PMGR 11 of the preferred embodiment includes its own ROM, RAM, timers, analog to digital converters, and general purpose I/O lines. Although a variety of devices can be used to perform the functions of PMGR 11, the preferred embodiment uses part number 50753, which is a semiconductor chip manufactured by Mitsubishi Corporation.

The software stored within PMGR 11 of the present invention provides for three main functions in controlling the power managernent of the various devices. These functions are receiving commands from the CPU 12 and performing in response to these commands, controlling the transfer of communications between the PMGR and peripheral units coupled to the I/O controller unit 19, and monitoring the system as well as providing the timer to maintain the real time clock. An 8-bit data bus and two handshake lines provide the coupling between CPU 12 and PMGR 11 through the via unit 28. The 8-bit databus is used to transfer command and data between CPU 12 and PMGR 11. This 8-bit communication is achieved by the use of a two line

handshaking scheme wherein commands are provided by CPU 12 and replies are provided by PMGR 11 on data and handshake lines 33.

Once the command is sent from CPU 12 through via unit 28 to PMGR 11 and the handshake is completed, PMGR 11 decodes the command and executes it. If no reply data is to be returned, PMGR 11 waits for the handshake for the next command to begin from CPU 12. If reply data is to be returned, PMGR 11 begins the reply handshake and returns the requested data. In the preferred embodiment commands and replies are transmitted in a protocol comprising of a command/reply byte, a count byte and optional data bytes.

Once every 1/60 of a second (frequency of 60 Hz), the clock oscillator 16 generates an interrupt to PMGR 11 and this interrupt is coupled to CPU 12 on line 34. When this interrupt is generated, PMGR 11 closes the I/O channel from I/O controller 19 and further, will not respond to any handshake requests from CPU 12. The interrupt on line 34 causes CPU 12 to suspend the data transfer to PMGR 11. During this interrupt cycle, PMGR 11 performs its periodic monitoring routines which include updating the real time clock, checking the battery power level and sending an auto poll command. The auto poll command is associated with the auto poll scheme of the preferred embodiment in which the CPU 12, through PMGR 11, automatically interrogates (polls) devices coupled to bus 37 to determine the presence of data for transfer.

PMGR 11 contains the necessary I/O transceiver functions for transfer of information between PMGR 11 and I/O unit 19 on bus 37. Packets of information to be sent on bus 37 to I/O unit 19 are sent by CPU 12 to PMGR 11 in the data portion of the command signal. Data received by PMGR 11 from I/O controller 19 is buffered internally and once received, this data is stored within PMGR 11 until requested by CPU 12. If a new I/O command was transmitted by CPU 12 during a previous command/execution cycle, the new command and

its corresponding data is supplied as the next I/O command which is to be sent. If the I/O device has any data to return, PMGR 11 receives, buffers and stores the data. When the data is completely received, PMGR 11 interrupts CPU 12 on interrupt line 34 and CPU 12 responds to the interrupt by determining the source of the interrupt and data is obtained from PMGR 11.

PMGR 11 includes a one second timer which is based on the 60 Hz frequency of clock 16. PMGR 11 also includes its own internal clock which performs as a real time clock. The one second timer is used to supply a wake up timer and create the one second interrupt for triggering the various monitoring functions. That is, as each new second is counted within PMGR 11, a number of periodic operations occur. Firstly, the real time clock and the wake up timer (if enabled) are updated. The wake up timer is an internal alarm clock which is used to provide an alarm/signal whenever the real time clock coincides with the tome set for the wake up timer (if enabled). Next, computer 10's power system and battery 17 are checked to determine the battery power level and if a low battery condition exists. The battery charger circuit 18 includes means for monitoring the level of the battery and for determining if the power level drops below a predetermined level. Then, the internal temperature is also checked followed by the interrupt to the CPU. Subsequently PMGR 11 sends any pending I/O transactions to CPU 12.

It is to be appreciated that via unit 28 performs the function of an interface unit between the CPU 12 and PMGR 11. Via unit 28 includes general purpose I/O devices, internal timers, interrupt generators, as well as input and output ports. However, it is to be noted that PMGR 11 can be readily adapted to operate without such a via unit 28 without departing from the spirit and scope of the present invention.

In order to provide the control over the consumption of power by computer 10 for the primary purpose of extending the life of battery 17 when

computer 10 is disconnected from an external power source, PMGR 11 provides for a number of control and monitoring functions for this purpose. PMGR 11 is utilized to cause computer 10 to be in one of three separate modes of operation. The three modes are the normal, slow and sleep modes. PMGR 11 responds to each of these modes by controlling the clocking signal being sent to a given device and/or controlling the voltage being supplied to a given unit. The clock signals coupled from the clock oscillator 16 to PMGR 11 are coupled to the clock control unit 27. Clock control unit 27 operates as a switch to couple the various clock signals on lines 41, 42 and 43 to CPU 12, serial communication controller unit 21 and the disk controller unit 20, respectively.

A power supply 29, which receives its power from battery 17, provides the needed voltages by computer 10. These supply voltages, shown as Vcc's in Figure 1, are coupled through PMGR 11, wherein PMGR 11 provides separate Vcc sources to the various units through the analog interface unit 26. As shown in Figure 1, VccA is coupled to the CPU 12 and related units. Three other separate Vcc sources are also provided from PMGR 11 as dedicated Vcc voltages to serial communication drivers 22, sound unit 24 and to the modem 25 through analog interface unit 26. These voltages are designated as VccB, VccC and VccD, respectively. It is to be noted that control lines are also present between PMGR 11 and clock control unit 27 and between PMGR 11 and analog interface unit 26. In the preferred embodiment, analog interface unit 26 is comprised of a plurality of transistor switches for switching the various Vcc sources onto their corresponding lines. The clock control unit 27 also includes various switches for coupling the clock signals to the corresponding units. Further, it is to be appreciated that PMGR 11 also includes circuitry for the various clocking signals for distribution onto lines 41-43. It is to be noted that PMGR 11 can change the various clocking rates of the clocking signals present on lines 41-43.

In the normal (or wake) mode of operation, computer 10 is fully active and all of the switches within clock control unit 27 and the analog interface unit 26 are closed. However, commands can be provided by CPU 12 automatically in response to stored routines, or in response to a user input through I/O unit 19, to deactivate transistor switches which couple VccB, VccC and VccD, in order to remove the applicable Vcc power from the serial communication controller drivers 22, sound drivers of unit 24 and modem 25. Alternatively, in order to conserve power of the battery, Vcc voltages for powering units 22, 24 and 25 need not be applied until such unit usage is requested by the system or the user.

In order to further conserve power, PMGR 11 will send computer 10 into a sleep (inactive) mode under an occurrence of either of two conditions. When the battery charger circuit 18 notes that battery 17 has dropped to a predetermined level, which level is deemed to be detrimental to further operation of computer 10, PMGR 11 places computer 10 into a sleep mode. PMGR 11 can also enter the sleep mode when a sleep command is provided by CPU 12. CPU sends a sleep command to PMGR 11 when there has been no user activity for a predetermined amount of time or when the user decides to stop work and shut down the computer 10.

Before entering the sleep mode, the operating system of the computer, as well as the various drivers, save the current state information in RAM 14. Thus, the state of the various registers, drivers and other memory devices are stored within RAM 14 for later restoration. Once these necessary states are stored in RAM 14, PMGR 11 releases all of the switches in analog interface unit 26 so that power is removed from the various units of computer 10. It is to be noted that power is removed from RAM 14 if RAM 14 is comprised of non-volatile memory such as an EPROM, which is the case with the memory device 14 of the present invention. However, if RAM 14 is comprised of volatile

memory then the transistor switch applying Vcc power to RAM 14 is kept closed so that Vcc is still applied to RAM 14 keeping it active in order to retain the stored information. It is to be noted that non-volatile memory is preferred so that Vcc need not be applied to RAM 14 in the sleep mode. Further, it is to be noted that the preferred embodiment uses CMOS memory.

In an alternative embodiment, VccA can be coupled onto line 45 in order to keep the power supplied to CPU 12. The internal clock of PMGR 11 can be decoupled from CPU 12 by clock control unit 27 thereby disabling the clock input to CPU 12 and halting the execution of the CPU. The CPU internal states are frozen with all CPU internal RAM and control registers remaining intact by halting the execution of the CPU. Halting the execution of CPU 12 typically will lower its power consumption by two orders of magnitude.

Although a number of conditions can cause computer 10 to wake from the sleep mode, computer 10 of the present invention has three possible conditions which triggers it to leave the sleep mode. PMGR 11 continues to monitor lines 37 such that any input from I/O controller19a will cause computer 10 to wake from the sleep state. The I/O input is typically a pressing of a key on the keyboard and/or the movement of the cursor control device. The second condition for waking up computer 10 occurs if the wake up timer (alarm clock) within PMGR 11 had been enabled and matches the real time clock within PMGR 11. Upon the activation of the alarm clock, PMGR wakes computer 10 from its sleep state. Finally, the third condition of computer 10 occurs if PMGR 11 was set to monitor the detection of a ring signal from modem 25. If an incoming signal is received by modem 25, the ring signal is detected by PMGR 11 and causes computer 10 to awake from its sleep state.

Upon waking, computer 10 accesses RAM 14 to retrieve the stored state of the various units for restoring computer 10 to the state it was in prior to

entering the sleep mode. Further, upon waking, computer 10 initiates a diagnostic routine for ensuring proper operation of computer 10.

The third mode of operation of computer 10 is known as the slow mode. The slow mode is a condition similar to the active mode, except that the clock rate of the clocking signal to the various units is slowed. That is, by reducing the clock rate of computer 10, as much as 25-30% of power savings can be obtained. Although all of the clocking signals on lines 41-43 can be slowed, it is to be noted that the clock signal on each line can be slowed. Slowing the clock rate of the clocking signal on line 41 to CPU 12 can achieve 25-30% savings in power.

Furthermore, the slow mode is entered from the normal mode when no activity has been detected after a predetermined time period, this time period being less than the time period for placing the system into the sleep mode. Thus, if no activity occurs for a certain duration, computer 10 enters the slow mode first and if the non-active cycle continues, computer 10 will eventually enter the sleep mode after an additional time period.

The slow state can be entered and departed by user command or CPU command. It is appreciated that clock signals to units 20 and 21 can be decoupled by clock control unit 27, wherein units 20 and 21 are deactivated and will not lose the current internal states of those units.

Referring to Figure 2, a transistor switch 50 utilized in the clock control unit 27 is shown. It is to be appreciated that only one switch 50 is shown, however, the actual clock control unit 27 is comprised of a plurality of these switches 50. A clock signal from PMGR 11 is coupled through transistor 51 to its corresponding device 52. The control signal is also obtained from PMGR 11 and is coupled to the gate of the transistor 51. When transistor 51 is made active by the control signal, the clock signal is coupled to device 52. Typically, device 52 is a CMOS device so that when the clock signal is

removed from this CMOS device, the device shuts down and consumes none or very little power. It is to be noted that in some of the devices, such as units 20 and 21, the clock signal can be decoupled from these devices while the Vcc supply to these devices are present.

Referring to Figure 3, a transistor switch 54 comprising one of the switches within analog interface unit 26 is shown. However, it is to be noted that a plurality of these switches reside within analog interface unit 26. One of the Vcc lines is coupled from PMGR 11 through transistor 55 to device 56. A control line also from PMGR 11 is coupled to the gate of transistor 55 for controlling the coupling of Vcc to device 56 through transistor 55. It is to be noted that power is supplied to device 56 when transistor 55 is made active and that device 56 may not necessarily be a CMOS device since power will be removed from device 56 when transistor 55 is cut off.

It is to be appreciated that the above description in reference to Figures 1-3 can be represented in various other circuit equivalent forms without departing from the spirit and scope of the invention. Further, in reference to Figure 1, the actual devices and the switching of the power and clock signals can be readily adapted to operate with other designs without departing from the spirit and scope of the present invention. However, in order to provide a more detailed workings of the present invention, various specific details pertaining to the preferred embodiment are disclosed below. CPU 12 provides various commands to PMGR 11 for connecting the Vcc power to applicable devices as needed. Further, clock signals can be either disconnected from various devices, or in the alternative, PMGR 11 can provide different clock speeds, such as during the slow mode. CPU 12 can be made to provide these commands in response to a stored routine or in response to a monitoring function of the PMGR or in response to a user interaction through I/O unit 19.

It is to be noted that the various drivers of computer 10 are responsible for powering on and off their respective peripheral devices. It is to be noted that drivers of computer 10 can be hardware or software drivers, or a combination thereof, and the preferred embodiment uses software drivers. That is, software is used to control the powering on and off the respective devices. Thus, the power to the disk control unit 20 also powers the floppy disk, the power to the parallel communications controller 23 also powers its associated peripheral device, such as the hard disk. The drivers of the serial communications controller 21 and the power to the sound drivers 24 also are controlled as needed. These drivers are responsible for maintaining the time that these devices are powered to a minimum in order to conserve power. Thus, they are only activated when a given particular device is needed. Generally, each device driver will enable its peripheral device when the driver is needed.

In the case of the floppy disk controller 20, the power is only applied to the peripheral device when an actual disk read or write is under way. Also, in the instance with the modem 25, it is kept without power until a ring is detected by PMGR 11 or when activated by the CPU 12. As stated previously those devices that have system clock inputs are enabled/disabled by controlling their connection to the clock. They can remain powered even though the rest of the system is off, therby retaining their internal states, but consuming less power. As such, clock control devices do not need be re-initialized or re-enabled when their clock is turned off. Those devices that do not have a clock input or do not require any state to be retain are enabled/disabled by controlling their connection to power. As stated previously, the power can be removed from CPU 12 in which case the internal states of CPU 12 are stored in RAM 14 prior to power down. It is to be stressed that the clock input can be removed from CPU 12 in which case the internal states of CPU 12 are retained.

In reference to the battery charger circuit 18, the circuit charges the battery when coupled to an external power source, but circuit 18 is also utilized to monitor battery 17. PMGR 11 monitors the power level of battery 17 and alerts the user when that level drops to a predetermined level, permitting the user to finish the current job of the computer and shutting down the computer prior to complete breakdown of computer 10. An analog-to-digital converter within PMGR11 provides for the conversion of the analog battery voltage to a digital signal. Although not shown in Figure 1, a temperature sensing mechanism is also coupled to a PMGR 11 to sense the temperature and another analog-to-digital converter within PMGR 11 is also used to convert this analog signal to a digital signal.

It is to be appreciated that the PMGR 11 of the preferred embodiment of the present invention provides for a variety of techniques to monitor and control the distribution of power and clocking signals in order to conserve the time that computer 10 can be self-sustaining when decoupled from an external power source.

CLAIMS

1. In a portable computer, having a central processing unit (CPU), a memory, a plurality of peripheral devices including a user interactive device, and a battery for powering said computer, an apparatus for managing the use of power from said battery by said computer, comprising:

control means coupled to said CPU for receiving commands from said CPU and also coupled to receive inputs from said user interactive device;

said control means also coupled to said battery for controlling distribution of said power to various units of said computer;

said control means also coupled to provide an internal clock and distributing a clock signal to some of said units of said computer;

first switching means coupled to said control means for distributing said power to some of said various units, said first switching means including first switches for switching said power, said first switches being controlled by said control means;

second switching means coupled to said control means for distributing said clock signals to some of said units, said second switching means including second switches for switching said clock signal, said second switches being controlled by said control means.

2. The apparatus of Claim 1, wherein said first switching means decouples power from each of said variuous units coupled to said first switching means until each of said respective units are needed to be accessed by said CPU.

3. The apparatus of Claim 2, wherein said second switching means decouples said clock signal from each of various units coupled to said second switching means until each of said respective units are needed to be accessed by said CPU.

4. The apparatus of Claim 3, wherein said control means provides for three modes of operation, a first mode for providing power and clock signals to said various units when needed by said computer, a second mode for removing power or clock signal to deactivate respective devices to conserve power, and a third state in which the frequency of said clock signal is reduced in order to reduce power consumption to those units coupled to receive said clock signal.

5. In a portable computer, having a central processing unit (CPU), a memory, a plurality of peripheral devices including a user interactive device, and a battery for powering said computer, an apparatus for managing the use of power from said battery by said computer, comprising:

control means coupled to said CPU for receiving commands from said CPU and also coupled to receive inputs from said user interactive device;

said control means also coupled to said battery for controlling distribution of said power to various units of said computer;

said control means also coupled to provide an internal clock and distributing a clock signal to some of said units of said computer;

said control means providing for three modes of operation of said computer, an active mode for providing active operation of said computer, a sleep mode for placing said computer in an inactive state to conserve power and a slow mode in which the frequency of said clock signal is reduced in

order to reduce power consumption to those units coupled to receive said clock signal:

first switching means coupled to said control means for distributing said power to some of said various units, said first switching means including first switches for switching said power, said first switches being controlled by said control means;

second switching means coupled to said control means for distributing said clock signals to some of said units, said second switching means including second switches for switching said clock signal, said second switches being controlled by said control means;

monitoring means for monitoring said various units and providing information of monitored units to said control means.

6. The apparatus of Claim 5, wherein said first switching means decouples power from each of said variuous units coupled to said first switching means until each of said respective units are needed to be accessed by said CPU.

7. The apparatus of Claim 6, wherein said second switching means decouples said clock signal from each of various units coupled to said second switching means until each of said respective units are needed to be accessed by said CPU.

8. The apparatus of Claim 7, wherein prior to entering said sleep mode said apparatus stores CPU states in said memory and retrives said CPU states from said memory when reactivated to said active mode.

9. The apparatus of Claim 8, wherein said computer enters its sleep mode if an input from an input/output (I/O) device does not occur for a first predetermined time period.

10. The apparatus of Claim 9, wherein said monitoring means monitors said I/O device and causes said computer to leave its sleep mode if an input is sensed from said I/O device.

11. The apparatus of Claim 10, wherein said computer enters its slow mode if said input from said I/O device does not occur for a second predetermined time period, said second predetermined time period being shorter than said first predetermined time period.

12. The apparatus of Claim 11, wherein said monitoring means monitors said I/O device and causes said computer to leave its sleep mode if an input is sensed from a modem coupled to said control means.

13. The apparatus of Claim 12, wherein said I/O device is said user interactive device.

14. The apparatus of Claim 10, wherein said first and second switches are field-effect transistors.

15. The apparatus of Claim 14 further including a reference clock means coupled to said control means for providing a crystal controlled reference clock signal.

16. In a portable computer, having a central processing unit (CPU), a memory, a plurality of peripheral devices including a user interactive device, and a battery for powering said computer, an apparatus for managing the use of power from said battery by said computer, substantially as hereinbefore described with reference to the accompanying drawings.

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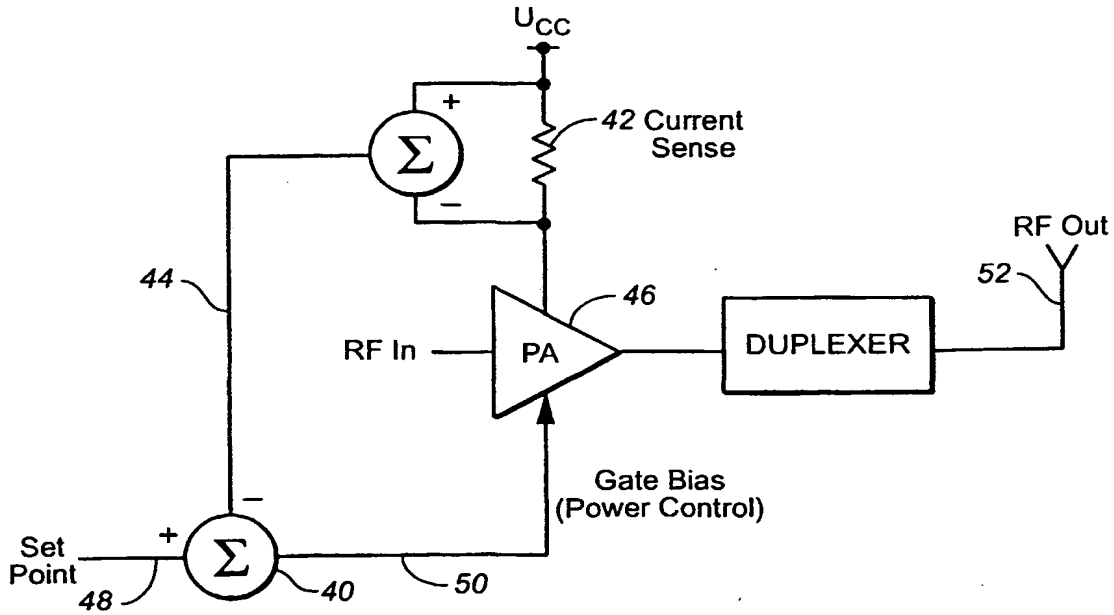
(54) **Title:** PERSONAL COMPUTER CARD RADIO MODEM USING NON-STANDARD POWER OUTPUT LEVEL



(57) **Abstract:** A hand-held, PCMCIA cellular radio modem card is described which uses a non-standard power output level. The non-standard power output is defined as the maximum RF power attainable such that the current drawn by the power amplifier does not exceed 400 mA. This definition permits the use of the wireless modem inside hand-held computing devices without the use of an additional battery pack extension.

WO 02/07494 A2

PERSONAL COMPUTER CARD RADIO MODEM USING NON-STANDARD POWER OUTPUT LEVEL

Background of the Invention

The present invention relates to personal computer (PC) card radio modems. Small hand-held personal computing devices can use Personal Computer Memory Card Interface Association (PCMCIA) radio modems to connect to a wireless network. PC card radio modems typically use battery power from the hand-held PC or from a battery pack extension.

A problem that exists in prior-art systems in which the wireless modem operates on a network such as the North American AMPS or CDPD network, is a battery pack extension is used to supplement the power supplied to the wireless modem. Typically, hand-held PCs use two AA batteries, which suffer from low capacity and a low peak current capability.

Six different standard RF power levels are required by the CDPD standard (CDPD R1.1 Part 409) and the AMPS standard (IS-19B) for a class III cellular device. With two AA batteries supplying the hand-held PC and the PCMCIA wireless card, it is difficult to achieve the highest RF power level; which, for a class III cellular device, is an output power of 28 dBm where 0 dBm is 1mW output power. Typically, prior art uses a battery pack extension on the PCMCIA card to achieve the highest RF power output. This is an undesirable solution as the esthetics of the complete product are poor.

It is desirable to have an improved system, which avoids some of the problems of the prior art.

Summary of the Invention

In one embodiment, the present invention relates to a PC card radio transceiver which uses a non-standard power output level. The non-standard power output level is limited by the peak sustainable current available from the battery inside the hand-held PC. In one embodiment, this current is limited to 600 mA. The non-standard RF power

obtainable, given a 600mA maximum limit, is typically between 24 dBm and 28 dBm (in one implementation, 26.5 dBm). The non-standard power output level has a nominal value less than the nominal value required by the standard, yet is still within the acceptable range (+2, -4dB) specified in the standard.

The advantage of the present invention is that the radio transceiver in the PC card can operate while attached to a hand-held PC without requiring a battery pack extension. The system allows the two AA batteries of the hand-held PC to produce an acceptable, high-level RF output power.

Implementation of a non-standard RF power level, which is based on a current restriction, requires the automatic leveling circuit (ALC) of the power amplifier to be a current leveling circuit as opposed to a power leveling circuit as in prior art systems. A current leveling circuit achieves the same effect as a power leveling circuit, given the load on the power amplifier remains constant. In practice, this is a reasonable assumption.

Brief Description of the Drawings

Fig. 1 is a block diagram illustrating a PCMCIA cellular modem attached to a hand-held PC.

Fig. 2 is a diagram illustrating the power amplifier, current leveling circuit, duplexer and antenna used in the PC card cellular radio transceiver of one embodiment of the present invention.

Fig. 3 is a diagram illustrating both the implemented and non-implemented standard power output levels as well as the non-standard power output level of one embodiment of the present invention.

Fig. 4 is a block diagram illustrating one embodiment of the current leveling system of the present invention.

Fig. 5 is a schematic illustrating one embodiment of the current leveling circuit for one embodiment of the present invention.

Detailed Description of the Preferred Embodiment

Fig. 1 is a block diagram that illustrates a hand-held personal computer 20 and PC card 22. In one embodiment, the PC card is a cellular modem with a built-in radio transceiver.

The hand-held PC 20 sends signals to be transmitted to the PC card cellular modem 22. Additionally, the hand-held PC supplies power for the operation of the PC card cellular modem 22. Typically, two AA batteries in the hand-held PC power both the hand-held PC and the PC card cellular modem 22. Since relatively small batteries are used, the maximum current which can be drawn by the PC card cellular modem 22 is limited to less than what is needed to meet the nominal output power requirements of IS-19B and CDPD Part 409 standards given present power amplifier and duplexer technologies. In one embodiment, the PC card cellular modem 22 should not draw more than 600 mA of current.

Fig. 2 is a simplified diagram of the elements in the PC card cellular modem of one embodiment of the present invention. A current leveling circuit 32 controls the current supplied to power amplifier 30 and hence indirectly controls the output power of amplifier 30. In a PC card cellular modem, the current supplied to the power amplifier makes up a large percentage of the total current consumed by the device. The output of the power amplifier 30 is sent to a duplexer 34, then out the antenna 36.

In the present invention, the current leveling circuit 32 limits the current used by the power amplifier 30 at the highest power output level. This highest power output level is the non-standard power output level described below.

In one embodiment, the current leveling circuit 32 limits the current drawn by the power amplifier 30 to 400 mA when it is transmitting at the highest output power level. The current consumption of the entire card is therefore limited to 600mA.

Fig. 3 illustrates the RF output levels for the standard and non-standard power outputs for CDPD standard R.1.1 Part 409 and AMPS standard IS-19B. There are six standard output power levels for a class III cellular device. The standard, nominal power

output levels range from 8 to 28 dBm in 4 dB steps. In one embodiment, the non-standard power output level is between the highest standard power level, which is not implemented (28 dBm), and the highest implemented power level (24 dBm). In one embodiment, by limiting the current draw by the power amplifier to 400 mA or less (the total PC card current draw to 600mA or less), the non-standard power output level is about 26.5 dBm. This level is below the nominal 28 dBm power level specified in the standard, yet still falls within the acceptable range of +2dB to –4dB from nominal specified in the standard.

Fig. 4 is a block diagram of a circuit to implement one embodiment of the present invention. A set point value 48 is sent to adder 40 and combined with a feedback value on line 44 from current-sensor 42 to produce a gate bias (power control) signal for power amplifier 46. The set point values are controlled by the micro-processor. Each set point value corresponds to a power output level for the power amplifier 46. The current leveling circuit limits the power output by the power amplifier. In a preferred embodiment, the maximum set point value is such that the current drawn by the power amplifier is less than 400 mA.

Fig. 5 illustrates details of one embodiment of the current leveling circuitry for operation with the PC card radio transceiver of the present invention.

Other modifications and implementations will occur to those skilled in the art, without departing from the spirit and scope of the present invention. Accordingly, the above description is not intended to limit the invention, which is to be limited only by the following claims.

Claims:

1. A PC radio card adapted to be connected to and powered by a hand-held personal computer, the PC radio card using a number of output power levels controlled by current supplied to power amplifier in the PC radio card, the output power levels including multiple implemented standard power output levels and a nonstandard battery-limited power output level, the nonstandard battery-limited power output level being greater than the multiple implemented standard power output levels but less than an unimplemented standard power output level.

2. The PC radio card of Claim 1 wherein the non-standard battery-limited power output level is such that the current drawn by the power amplifier is 400 mA or less.

3. The PC radio card of Claim 1 wherein the PC radio card includes a current control automatic leveling circuit, keeping the current supplied to the power amplifier less than 400 mA.

4. The PC radio card of Claim 1 wherein the PC radio card is powered by a hand-held personal computer using two AA batteries.

5. The PC radio card of Claim 1 wherein the non-standard battery-limited power output level is less than 28 dBm and more than 24 dBm, wherein an output of 0 dBm is calibrated to 1 mW of output power.

6. A PC radio card adapted to be connected to and powered by a hand held personal computer, the PC radio card using a number of output power levels set by current supplied to power amplifier in the PC radio card, the output power levels including multiple implemented standard power output levels and a nonstandard battery-

limited power output level, the nonstandard battery-limited power output level being such that the current drawn by the power amplifier is 400mA or less.

7. The PC radio card of Claim 6 wherein the non-standard battery-limited power output level is greater than the implemented standard but less than an unimplemented standard power output level.

8. The PC radio card of Claim 6 wherein the PC radio card is powered by a hand-held personal computer using two AA batteries.

9. The PC radio card of Claim 6 wherein the PC radio card has a current controlled automatic leveling circuit to limit the current supplied to the power amplifier.

10. The PC radio card of Claim 6 wherein the non-standard battery-limited power output level is less than 28 dBm and more than 24 dBm when 0 dBm is calibrated to one mW of output power.

11. A system including:

a battery-powered hand held personal computer; and

a PC radio card connected to and powered by the hand held personal computer, the PC radio card using a number of output power levels set by current supplied to power amplifier in the PC radio card, the output power levels including multiple implemented standard power output levels and a nonstandard battery-limited power output level, the nonstandard battery-limited power output level being greater than the multiple implemented standard power output levels but less than an unimplemented standard power output level.

12. The system of Claim 11 wherein the nonstandard battery-limited power level is such that the current drawn by the power amplifier is 400 mA or less.

13. The system of Claim 11 wherein the hand-held personal computer is powered two AA batteries

14. The system of Claim 11 wherein the nonstandard battery-limited power level limits the current supplied by the hand-held personal computer to the PC radio card to less than a given amount.

15. The system of Claim 11 further comprising a current controlled automatic leveling curcuit in the PC radio card to limit the current supplied to the power amplifier.

16. A PC card transceiver including:

an antenna;

an amplifier operably connected to the antenna:

a current controller operably connected to the amplifier to set the power output of the transceiver, the current controller adapted to produce a number of standard transceiver power output levels and a nonstandard transceiver output power level, the nonstandard transceiver output power level being such that the amplifier current is at a level that makes efficient use of the PC card transceiver batteries.

17. The PC card of Claim 16, further comprising a duplexer operatively positioned between the amplifier and the antenna.

18. The PC card of Claim 16 wherein the non-standard battery-limited power output level is greater than the implemented standard but less than an unimplemented standard power output level.

19. The PC card transceiver of Claim 16 wherein the amplifier is limited to 400 mA of current draw.

20. The PC card transceiver of Claim 16 wherein the PC card transceiver is adapted to be powered by a hand-held personal computer.

FIG._1

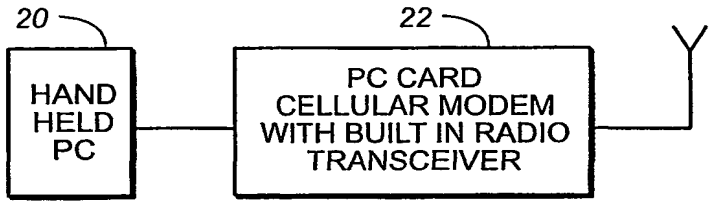
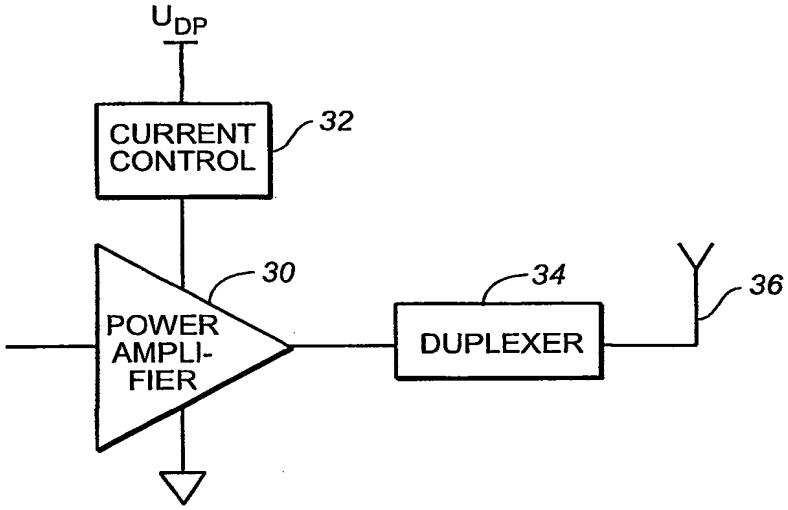


FIG._2



STANDARD POWER OUTPUT LEVELS		NON-STANDARD POWER OUTPUT LEVEL
Not Implememted	0 + 28 dBm	Maximun RF outpout power such that the power drawn by the PC card is less than 600mA. ~ 26.5 dBm
	1 + 28 dBm	
	2 + 28 dBm	
Implememted	3 + 24 dBm	
	4 + 20 dBm	
	5 + 16 dBm	
	6 + 12 dBm	
	7 + .8 dBm	

FIG._3

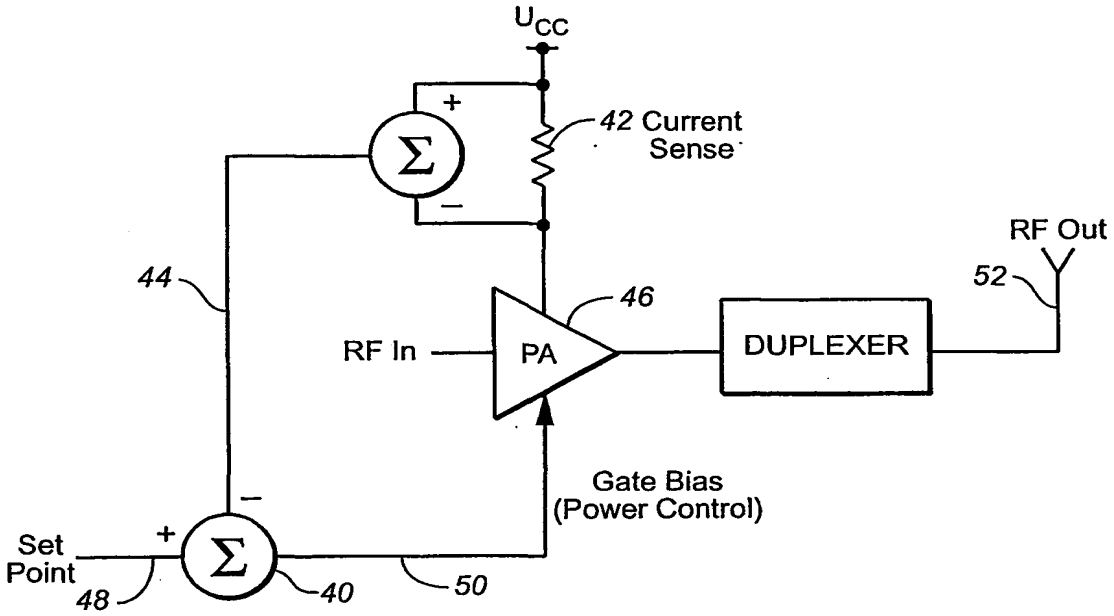

U_{CC}
+
Σ
−
42 Current Sense
RF Out
52
44
46
RF In
PA
DUPLEXER
Gate Bias (Power Control)
Set Point
48
+
−
Σ
40
50

FIG._4

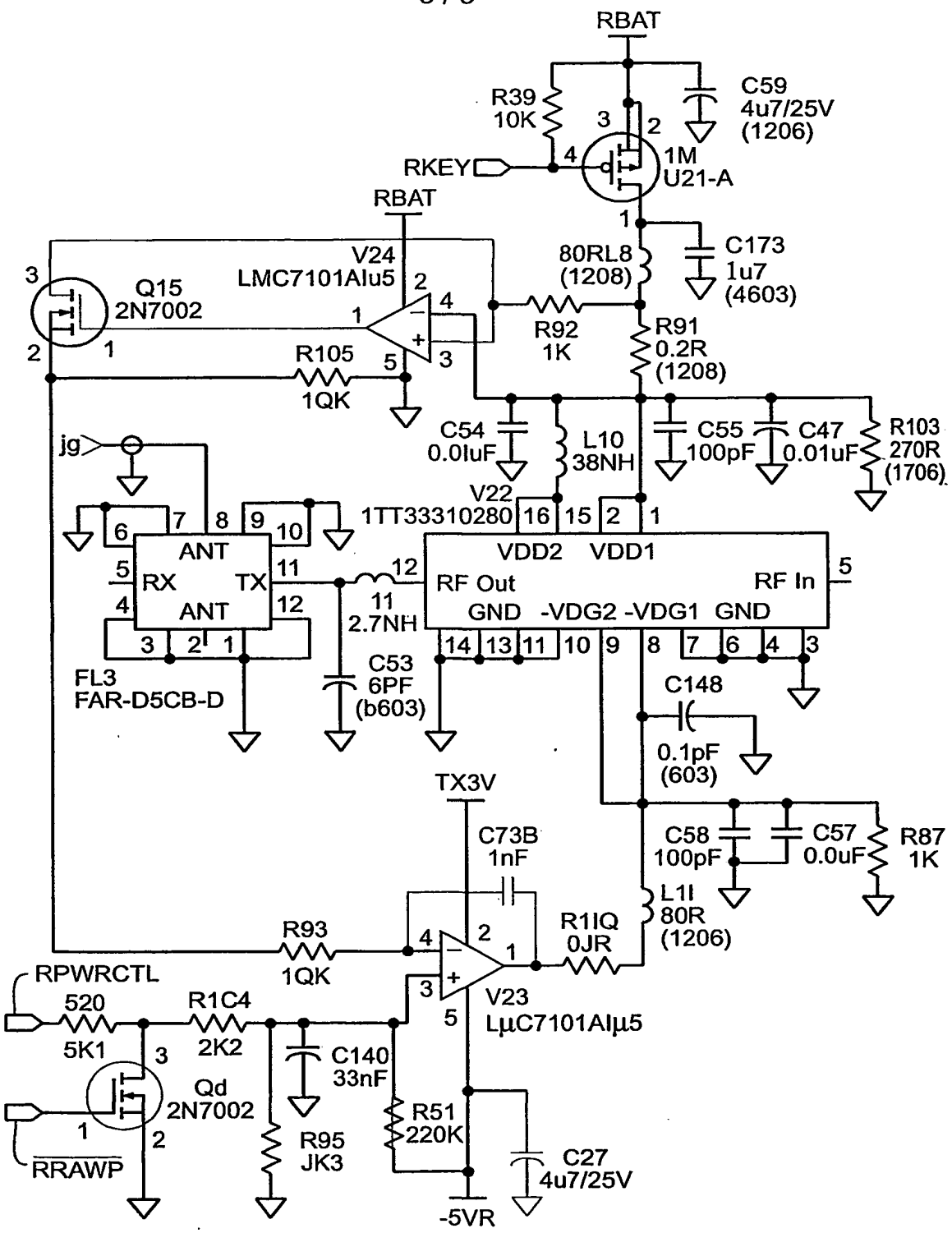


FIG._5 Schematic for Current Control ALC

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10	(bus adj (size width)) with (power near3 (sav$3 reduc$3 conserv$3))	USPAT	OR	OFF	2005/09/15 14:04
L2	123	(bus adj width) with power	USPAT	OR	OFF	2005/09/15 11:41
L3	2	2 and 713/320.ccls.	USPAT	OR	OFF	2005/09/15 11:44
L4	100	(chang$3 modify$3 vary$3) near3 (bus adj width)	USPAT	OR	OFF	2005/09/15 11:45
L5	0	4 same ((sav$3 reduc$4) near3 power)	USPAT	OR	OFF	2005/09/15 11:48
L6	114	(memory near3 bank$1) with (power near3 (sav$3 reduc$4))	USPAT	OR	OFF	2005/09/15 11:49
L7	10	6 with number	USPAT	OR	OFF	2005/09/15 11:52
L8	2077	(bank near3 select$3) near5 memory	USPAT	OR	OFF	2005/09/15 11:53
L9	17	8 with (power near3 (sav$3 reduc$4))	USPAT	OR	OFF	2005/09/15 11:53
L10	17	9 not 7	USPAT	OR	OFF	2005/09/15 11:53
L11	1	"5,996,083".pn.	USPAT	OR	OFF	2005/09/15 14:20
L12	254	multimedia adj card	USPAT	OR	OFF	2005/09/15 14:20
L13	16	12 and (multimedia near3 standard)	USPAT	OR	OFF	2005/09/15 14:20
L14	17	12 and (multimedia near3 (standard specification))	USPAT	OR	OFF	2005/09/15 14:20
S1	8	("4841440" "5758108" "5737616" "5884086" "5758171" "6178514" "5606704" "5613130" "5737616").pn.	USPAT	OR	OFF	2005/09/13 14:54
S2	2	("9841987" "2235797" "0207494").pn.	EPO	OR	OFF	2005/09/13 15:02
S3	1813	(713/300 713/320 713/322).ccls.	USPAT	OR	OFF	2005/09/13 15:08
S4	1030	713/300.ccls.	USPAT	OR	OFF	2005/09/13 15:09
S5	7	mylly.in.	US-PGPUB; USPAT	OR	OFF	2005/09/13 15:12
S6	2	("5532945" "6477388").pn.	USPAT	OR	OFF	2005/09/13 15:18
S7	125068	power near5 (set$4 determin$3 adjust$3)	USPAT	OR	OFF	2005/09/14 10:01
S8	1674	S7 with (between near3 (value$1 level$1 setting$1))	USPAT	OR	OFF	2005/09/14 10:02
S9	1671	S8 and "3"	USPAT	OR	OFF	2005/09/14 10:02
S10	1813	(713/300 713/320 713/322).ccls.	USPAT	OR	OFF	2005/09/14 10:03
S11	5	S8 and S10	USPAT	OR	OFF	2005/09/14 10:05
S12	9689	power near5 intermediate	USPAT	OR	OFF	2005/09/14 10:05
S13	50	S12 and S10	USPAT	OR	OFF	2005/09/14 10:05
S14	31	S13 and peripheral	USPAT	OR	OFF	2005/09/14 10:06
S15	149173	power near5 (middle between intermediate)	USPAT	OR	OFF	2005/09/14 10:07

S16	4863	S15 with (maximum minimum default)	USPAT	OR	OFF	2005/09/14 10:07
S17	37	S16 and S10	USPAT	OR	OFF	2005/09/14 11:41
S18	15	S17 and peripheral	USPAT	OR	OFF	2005/09/14 16:35
S19	1	"6785830".pn.	USPAT	OR	OFF	2005/09/15 11:34

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/401,338	03/26/2003	Kimmo Mylly	915-005.48	4941

4955 7590 09/22/2005

WARE FRESSOLA VAN DER SLUYS &
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EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/401,338	MYLLY, KIMMO	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-26-03, 7-30-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. ____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: ____.

DETAILED ACTION

Examiner acknowledges preliminary amendments filed on 26 March 2003. The present office action is based on the claims and specification as amended.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 20020594, (Finnish Patent Application) , filed on 27 March 2002.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 4, 8, 10, 12, 13, 17, and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 2, applicant has used the word "substantially" in line 5 to describe the difference in degree between a power consumption setting and a first maximum limit. The usage of "substantially" does not unambiguously limit the scope of applicant's claims. Claims 4, 8, 10, 13, 17, and 24 are also rejected on this basis.

In addition, claim 2 recites the limitation "said first maximum limit" in line 5. There is insufficient antecedent basis for this limitation in the claim. It is noted that applicant has replaced all references to a "maximum limit" with a "maximum value." Claim 17 is also rejected on this basis.

Claim 12 recites the limitation "the bus width" in line 4. There is insufficient antecedent basis for this limitation in the claim. Applicant has not previously recited a bus width in the claim or its parent.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 9, 10, and 14-21, are rejected under 35 U.S.C. 102(b) as being anticipated by Amoni et al., U.S. Patent No. 5,884,086[1] (claims 1, 2, 4, 9, 10, 16, 17, and 20), and Robinson, U.S. Patent No. 5,532,945 (claims 1, 3, 9, 16, and 20).

Claims 1, 9, 14-16, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by McKeen et al., U.S. Patent No. 6,785,830[2].

Regarding claim 1, each of Amoni, Robinson, and McKeen teaches:

a method for determining the power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device

[1] Applicant-cited reference.
[2] U.S. issued patent of applicant-cited reference, WO 02/07494 A2.

[Amoni, col. 2, lines 32-44, Fig. 6A/6B, Robinson, Fig. 6], wherein the method comprising determining, for the power consumption, at least a first maximum value [Amoni, Fig. 6A, step 611, Robinson, Fig. 6, step 130, col. 11, lines 31-34] and a second maximum value [Amoni, Fig. 6, step 619, max threshold, Robinson, Fig. 6, step 132, peak power] which is higher than the first maximum value, and performing, between the electronic device and the peripheral device, setting of a maximum for the power consumption of the peripheral device to a value which is between said first and second maximum values [Amoni, Fig. 6, step 625, Robinson, Fig. 6, step 136, reduced power, McKeen, col. 1, lines 39-50].

Regarding claim 2, Amoni teaches:

the method according to claim 1, wherein said first maximum value is used as a default value for the power consumption, wherein the power consumption of the peripheral device is set, at the startup stage, to be substantially not higher than said first maximum value [col. 8, lines 19-22].

Regarding claim 3, Robinson teaches:

the method according to claim 1, wherein said second maximum value is used as the highest allowable value for the power consumption [Fig. 6, step 132, peak power].

Regarding claim 4, Amoni teaches:

the method according to claim 1, wherein messages are transferred between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value substantially between said first maximum limit and said second maximum limit [col. 6, line 32ff, "Auxiliary Power Communication Protocol"].

Regarding claim 5, Robinson teaches:

the method according to claim 1, wherein at least one content is stored in the peripheral device, to be used in connection with the electronic device, wherein at the stage of storing the

content, the power consumption set for the peripheral device is a value corresponding to said second maximum limit, and at the stage of using the content, the power consumption set for the peripheral device is a value corresponding to said first maximum limit [col. 1, line 67 to col. 2, line 3].

Regarding claims 9, 10, 16, 17, and 20, Amoni teaches the method of claims 1 and 4. Amoni also teaches the system, the electronic device, and the peripheral device to implement the claimed method.

Regarding claims 14, 15, 18, and 19, McKeen teaches the method of claim 1. McKeen also teaches the system and the electronic device to implement the claimed method, as recited in claims 9 and 16. McKeen also teaches that the electronic device is portable and comprises a means for performing mobile stations functions [hand-held PC and PC card radio transceiver, col. 1, lines 39-44].

Regarding claim 21, Robinson teaches the method of claims 1 and 5. Robinson also teaches the peripheral device recited in claim 20 and the storage of content recited in claim 21.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 11, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amoni in view of Yonezu et al., U.S. Patent No. 4,841,440[3].

Regarding claims 6, 11, and 22, Amoni teaches that a clock signal is generated in the device, but does not teach that the power consumption is controlled by adjusting the frequency of the clock signal.

Yonezu teaches that power consumption may be reduced by inhibiting a control clock signal for a peripheral device [abstract].

It would have been obvious to one of ordinary skill in the art to modify Amoni using the teachings of Yonezu. Both Amoni and Yonezu disclose methods of power control for peripheral devices. The addition of Yonezu's teaching would improve Amoni by providing a way to reduce power consumption.

Claims 7, 12, and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Amoni in view of Gupta et al., U.S. Patent No. 5,996,083.

Regarding claims 7, 12, and 23, Amoni teaches that the peripheral device comprises a bus, but does not teach controlling power consumption by controlling a width of the bus.

Gupta teaches a technique wherein power consumption in a processor is reduced by changing the width of a bus [col. 9, lines 21-32].

It would have been obvious to one of ordinary skill in the art to modify Amoni by providing a capability to modify the bus width, as taught by Gupta. The teachings of Gupta would improve the system of Amoni by reducing the number of data lines driven on the bus, thus reducing the overall power consumption.

[3] Applicant-cited reference.

Claims 8, 13, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson in view of Holder, Jr., U.S. Patent No. 5,892,729.

Regarding claims 8, 13, and 24, Robinson teaches that the peripheral device comprises one or more storage blocks, but does not teach the controlling of the number of storage blocks processed.

Holder teaches a memory comprising multiple storage banks which may be selectively activated [col. 3, lines 21-32].

It would have been obvious to one of ordinary skill in the art to modify Robinson by providing selectable memory banks, as taught by Holder. The teachings of Holder would improve the system of Robinson by providing selectable memory banks so as to reduce power consumption.

Regarding claim 25, it would have been obvious to one of ordinary skill in the art to store the first and second maximum values in the peripheral device.

Regarding claim 26, it would have been obvious to one of ordinary skill in the art to apply the teachings of Robinson to a multimedia card peripheral device.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Schmutz, U.S. Patent No. 6,477,388 B1;

Fung, U.S. Patent No. 6,859,882 B2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ji H. Bae
Patent Examiner
Art Unit 2115
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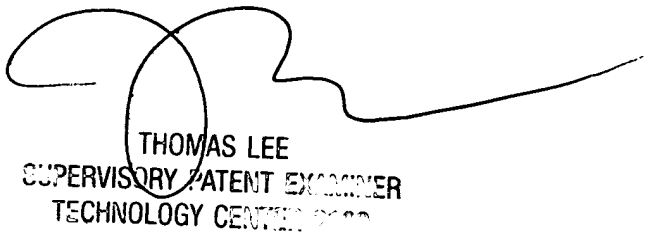
571-272-7181



FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	915-005.48	
(Use several sheets if necessary)	APPLICANT: K. Mylly	
(37 CFR 1.98(b))	FILING DATE: Herewith	GROUP

JC678 U.S. PTO 10/401338 03/26/03

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APROPRIATE
JB		5 6 0 6 7 0 4	2/25/97	Pierce et al			
JB		5 6 1 3 1 3 0	3/18/97	Teng et al			
JB		5 7 3 7 6 1 6	4/7/98	Watanabe			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
JB		0 2 0 7 4 9 4	1/31/02	WO				

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)

EXAMINER	DATE CONSIDERED
J. H. Bai	9-15-05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

(37 CFR 1.98(b))

ATTY. DOCKET NO.	SERIAL NO.
915-005.48	10/401,338
APPLICANT	
K. Mylly	
FILING DATE	GROUP
March 26, 2003	2185

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APROPRIATE
JB		4841440	6/20/89	Yonezu et al			
JB		5758108	5/26/98	Nakamura			
JB		5737616	4/7/98	Watanabe			
JB		5884086	3/16/99	Amoni et al			
JB		5758171	5/26/98	Ramamurthy et al			
JB		6178514	1/23/01	Wood			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
JB		9841987	9/24/98	WO				
JB		2235797	3/13/91	GB				
JB		0207494	1/31/02	WO				

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)

EXAMINER	DATE CONSIDERED
J. K. Bae	9-15-05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Notice of References Cited	Application/Control No. 10/401,338	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO	
	Examiner Ji H. Bae	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,532,945	07-1996	Robinson, Kurt B.	713/321
*	B	US-6,785,830	08-2004	McKeen et al.	713/320
*	C	US-5,996,083	11-1999	Gupta et al.	713/322
*	D	US-5,892,729	04-1999	Holder, Jr., Clinton Hays	365/233
*	E	US-6,477,388	11-2002	Schmutz, Thomas R.	455/522
*	F	US-6,859,882	02-2005	Fung, Henry T.	713/300
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Bib Data Sheet

CONFIRMATION NO. 4941

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/401,338	03/26/2003 RULE	713	2115	915-005.48

APPLICANTS

Kimmo Mylly, Tampere, FINLAND;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********
FINLAND 20020594 03/27/2002

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 05/23/2003

Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
☑ yes ☐ no	COUNTRY	DRAWING	CLAIMS	CLAIMS
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance	FINLAND	4	26	4
Verified and Acknowledged Examiner's Signature Initials JB				

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755 MAIN STREET, P O BOX 224
MONROE , CT
06468

TITLE
Method and a system for determining the power consumption in connection with an electronic device, and an electronic device

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time)

Kingston Exhibit 1004 - 258

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/401,338	MYLLY, KIMMO	
Examiner	**Art Unit**	
Ji H. Bae	2115	

SEARCHED			
Class	Subclass	Date	Examiner
713	300	9/15/2005	JB
713	320	9/15/2005	JB
713	322	9/15/2005	JB

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST text search (see attached search history)	9/15/2005	

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/401,338	MYLLY, KIMMO
Examiner	**Art Unit**
Ji H. Bae	2115

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	9/15/05								
	1	√								
	2	√								
	3	√								
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of: **Kimmo MYLLY**

U.S. Serial No.: **10/401,338** Examiner: **Ji H. Bae**

Filed: **March 26, 2003** Group Art Unit: **2115**

For: **A METHOD AND SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION

Sir:

In response to the Office Action of September 22, 2005, applicant respectfully requests reconsideration of the rejections of the claims of the above-referenced patent application in view of the following amendments and remarks. Please amend the application as follows.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Mail Stop Amendment, the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Kelly Puglio
Kelly Puglio

Dated: 12/22/2005

IN THE CLAIMS:

1. (Currently Amended) A method for determining power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device, wherein the method ~~comprising~~ comprises determining, for the power consumption, at least a first maximum value and a second maximum value which is higher than the first maximum value, and performing, between the electronic device and the peripheral device, setting of a maximum for the power consumption of the peripheral device to a value which is between said first and second maximum values.

2. (Currently Amended) The method according to claim 1, wherein said first maximum value is used as a default value for the power consumption, wherein the power consumption of the peripheral device is set, at a startup stage, to be substantially not higher than said first maximum ~~limit~~ value.

3. (Previously Presented) The method according to claim 1, wherein said second maximum value is used as a highest allowable value for the power consumption.

4. (Previously Presented) The method according to claim 1, wherein messages are transferred between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value substantially between said first maximum value and said second maximum value.

5. (Previously Presented) The method according to claim 1, wherein at least one content is stored in the peripheral device, for use in connection with the electronic device, wherein at a stage of storing the content, the power

consumption set for the peripheral device is a value corresponding to said second maximum value, and at a stage of using the content, the power consumption set for the peripheral device is a value corresponding to said first maximum value.

6. (Previously Presented) The method according to the claim 1, wherein at least one clock signal is generated in the peripheral device and wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

7. (Previously Presented) The method according to the claim 1, wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling a width of said bus.

8. (Previously Presented) The method according to the claim 1, wherein the peripheral device is provided with two or more storage blocks (2) controlled by controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

9. (Previously Presented) A system comprising an electronic device with means for connecting a peripheral device and means for supplying power to the peripheral device, and which system comprises means for determining power consumption, wherein at least a first maximum value and a second maximum value which is higher than the first maximum value are defined for the power consumption, and wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is between said first maximum value and second maximum value.

10. (Previously Presented) The system according to claim 9, comprising means for transferring messages between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value substantially between said first maximum value and said second maximum value.

11. (Previously Presented) The system according to claim 9, wherein the peripheral device comprises means for generating at least one clock signal, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

12. (Currently Amended) The system according to claim 9, wherein the peripheral device comprises at least one bus, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting ~~the bus~~ a bus width of the peripheral device.

13. (Previously Presented) The method according to the claim 9, wherein the peripheral device is provided with two or more storage blocks, and wherein the means for controlling the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

14. (Previously Presented) The system according to the claim 9, wherein the electronic device is a portable electronic device .

15. (Original) The system according to claim 14, comprising means for performing mobile station functions.

16. (Previously Presented) An electronic device provided with means for connecting a peripheral device and means for supplying power to the peripheral device, and means for determining power consumption, wherein at least a first maximum value and a second maximum value which is higher than the first maximum value are defined for the power consumption, and wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value.

17. (Currently Amended) The electronic device according to claim 16, comprising means for transmitting messages from the peripheral device and for receiving messages to the peripheral device, to set power consumption of the peripheral device to a value substantially between said first maximum ~~limit~~ value and said second maximum ~~limit~~ value.

18. (Previously Presented) The electronic device according to claim 16, wherein it is a portable electronic device.

19. (Original) The electronic device according to claim 18, comprising means for performing mobile station functions.

20. (Previously Presented) A peripheral device provided with means for connecting the peripheral device to an electronic device for supplying power to the peripheral device, wherein at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for power consumption, and wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which

is between said first maximum value and said second maximum value.

21. (Previously Presented) The peripheral device according to claim 20, wherein at least one content is stored in the peripheral device for use in connection with the electronic device.

22. (Previously Presented) The peripheral device according to claim 20, comprising means for generating at least one clock signal and means for controlling the power consumption of the peripheral device by frequency control of said at least one clock signal.

23. (Previously Presented) The peripheral device according to claim 20, comprising at least one bus and means for controlling the power consumption of the peripheral device by controlling a bus width of said bus of the peripheral device.

24. (Previously Presented) The peripheral device according to the claim 20, wherein the peripheral device is provided with two or more storage blocks, and that the means for controlling the power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

25. (Previously Presented) The peripheral device according to the claim 20, wherein said first maximum value and said second maximum value are stored in the peripheral device.

26. (Previously Presented) The peripheral device according to the claim 20, wherein said peripheral device is a MultiMediaCard™ peripheral device.

REMARKS

Claims 1-26 are pending. The independent claims are claims 1, 9, 16, and 20. All claims are rejected.

The Word "Substantially" is Not Indefinite

Claims 2, 4, 8, 10, 12, 13, 17, and 24 are rejected under 35 U.S.C. § 112 because the Office Action asserts that "usage of 'substantially' does not unambiguously limit the scope of applicant's claims." Applicant respectfully refers to MPEP § 2173.05(b)(D) which states that the term "substantially" is often used in a claim without rendering the claim indefinite. Applicant therefore traverses these indefiniteness rejections., for the reasons provided at MPEP § 2173.05(b)(D).

The Independent Claims are not Anticipated by the Cited Prior Art

Independent claims 1, 9, 16, and 20 are rejected as anticipated under 35 U.S.C. 102 by *Amoni* (U.S. Patent No. 5,884,086), and also *Robinson* (U.S. Patent No. 5,532,945), and also *McKeen* (U.S. Patent No. 6,785,830).

Amoni discloses a system and a method for supplying power to a peripheral device in a computer system. According to *Amoni*, the peripheral device instructs the main device to provide the necessary power to the peripheral device. The power level is not adjusted (handshaked) but the peripheral device is supplied with the power level it needs. In the main device there are switches for selecting a certain, fixed power level (col. 2, lines 40—44). The *Amoni* document does not mention anything about a maximum level, nor does it mention anything about using a certain value for the power level which is less than or equal to a maximum value. Moreover, the *Amoni*

document does not teach anything about adjusting the power level to a value which is between two different maximum values.

McKeen discloses a radio modem card which is intended to be used in connection with a portable PC device. The maximum transmission power of the radio modem card is adjusted to a value which is between two different power levels defined in a standard of a mobile communication system. The maximum transmission power is within allowed tolerances. The limitation of the transmission power is implemented so that the maximum current consumption of the power amplifier of the radio modem card is limited to a certain maximum value. This maximum value is defined in such a way that the total current consumption of the radio modem card does not exceed a predetermined value. The aim of this arrangement is to prevent the radio modem card from overloading the PC device from which the power is supplied to the radio modem card. This is necessary because, according to the example disclosed in *McKeen*, batteries are used as the power source of the PC device and the current which can be supplied from the batteries is limited.

McKeen discloses the limitation of the transmission power between two standard values. This non-standard transmission power level is defined on the basis of how much power the power source of the PC device can supply to the radio modem card. The non-standard power level is thus set to such value which allows the use of the maximum available current from the PC device. Therefore, a separate power source is not needed in the radio modem card to enable the use of the maximum transmission power of the radio modem card.

The solution of *McKeen* is quite different from the solution of the present claimed invention. In the present application, at least a first and a second maximum

values are defined for the power consumption, and the maximum of the power consumption is set to a value which is substantially between said first and second maximum value. In the system of *McKeen* the portable PC device does not affect the adjustment of the transmission power of the radio modem card. In other words, in the system of *McKeen* no actions are taken between the PC device and the radio modem card to set the power consumption of the radio modem card. This means that the radio modem card always sets its power consumption to a certain value independent of the device to which the radio modem card is connected. Further, the adjustment of the transmission power and the adjustment of the power consumption are not the same issue. The adjustment of the transmission power determines how much power can be transmitted from the card and the adjustment of the power consumption determines how much power the card itself draws from the power source. The standard maximum power levels for the transmission power do not determine any limits for the power consumption of the card.

The Applicant also respectfully points out that the limitation of the transmission power of power amplifier of the radio modem card does not directly limit the power consumption of the radio modem card. It may happen that although the transmission power is limited, the power consumption of the radio modem card may still vary due to alterations in the power consumption of other electronics of the radio modem card. In the solution disclosed by *Robinson*, a "power resource table" stored at the host is used, which table is updated and it can be read by the card.

On page 6 of the Office Action, several dependent claims are rejected in view of *Yonezu* (US Patent No. 4,841,440), or in view of *Gupta* (U.S. Patent No.

5,996,083), or in view of *Holder* (U.S. Patent No. 5,892,729). *Yonezu* discloses a solution where the idle/standby power consumption is controlled to the minimum. *Holder* discloses power consumption by controlling the clock connecting to different integrated circuits. *Gupta* also discloses a solution which seems to comprise two-way handshakes. There is a register on the host side, according to which the external device controls its function (the document mentions controlling the bandwidth as one way to decrease power consumption if the host register indicates a smaller maximum consumption than what is required for the external device).

Because all of the present independent claims should be allowable, the claims depending therefrom should also be allowable, notwithstanding *Yonezu, Gupta, and Holder.*

Further Comments About the Present Application

The invention of the present application provides an improved method and system for determining the power consumption to be suitable in each situation. The invention is based on the idea that at least a first and a second maximum value are determined for the power consumption, wherein the electronic device and the peripheral device set the power consumption to a value between these first and second maximum values. Thus, in different operating situations, for example the peripheral device can adjust its power consumption to be suitable for the situation.

By the method according to the invention, it is possible to avoid the use of an unnecessarily large regulator in an electronic device, which saves costs, and wherein the size of the electronic device can, in some cases, be reduced and, on the other hand, problems of heating caused by high power consumption can be avoided. Also

the power consumption can be reduced, which is advantageous particularly in portable devices. By means of the invention, the peripheral device connection can also be provided with flexibility, because the power consumption of the peripheral device can be adjusted and set to a value suitable for each situation of use. Furthermore, the invention makes it possible that new peripheral devices to be developed will function in connection with electronic devices made earlier, and existing peripheral devices will function in connection with new electronic devices to be developed. None of these advantages can be achieved by the cited references.

CONCLUSION

Thus, the Examiner is asked to kindly reconsider the Office Action in the light of the arguments presented herein, and to correspondingly issue a favorable Office Action at the next stage of the proceedings. The present amendments raise no new issues, and introduce no new matter.

Early allowance of all independent claims (and the pending claims depending therefrom) is earnestly solicited. Applicant would be grateful if the Examiner would please contact Applicant's attorney by telephone if the Examiner detects anything in the present response that might impede a speedy allowance.

Respectfully submitted,

Dated: Dec. 22, 2005

ANDREW T. HYMAN
Attorney for Applicant
Registration No. 45,858

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Facsimile: (203) 261-5676
USPTO Customer No. 004955

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Practitioner's Docket No. 915-005.048 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re application of: K. MYLLY

Application No.: 10/401,338 Group No.: 2115

Filed: March 26, 2003 Examiner: Ji H. Bae

For: **A METHOD AND SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE**

Mail Stop Amendments
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application.

STATUS

2. Applicant is

☐ a small entity. A statement:

☐ is attached.

☐ was already filed.

☒ other than a small entity.

CERTIFICATE OF MAILING/TRANSMISSION UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is, on the date shown below, being:

MAILING
☒ deposited with the United States Postal Service with sufficient postage as first-class mail, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

FACSIMILE
☐ transmitted by facsimile to the U.S. Patent and Trademark Office.

Signature Kelly Puglio

Date: 12/22/2005

Kelly Puglio
(type or print name of person certifying)

EXTENSION OF TERM

NOTE: "Extension of Time in Patent Cases (Supplement Amendments) - If a timely and complete response has been filed after a Non-Final Office Action, an extension of time is not required to permit filing and/or entry of an additional amendment after expiration of the shortened statutory period.

If a timely response has been filed after a Final Office Action, an extension of time is required to permit filing and/or entry of a Notice of Appeal or filing and/or entry of an additional amendment after expiration of the shortened statutory period unless the timely-filed response placed the application in condition for allowance. Of course, if a Notice of Appeal has been filed within the shortened statutory period, the period has ceased to run." Notice of December 10, 1985 (1061 O.G. 34-35).

NOTE: See 37 C.F.R. §1.645 for extensions of time in interference proceedings, and 37 C.F.R. §1.550(c) for extensions of time in reexamination proceedings.

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. §1.136 apply.

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 C.F.R. §1.136 (fees: 37 C.F.R. §1.17(a)(1)-(4)) for the total number of months checked below:

Extension (months)	Fee for other than small entity	Fee for small entity
☐ one month	$ 120.00	$ 60.00
☐ two months	$ 450.00	$225.00
☐ three months	$1,020.00	$510.00
☐ four months	$1,590.00	$795.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured. The fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

OR

(b) ☒ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

FEE FOR CLAIMS

4. The fee for claims (37 C.F.R. §1.16(b)-(d)) has been calculated as shown below:

(Col. 1)	(Col. 2)	(Col. 3)	SMALL ENTITY	OTHER THAN A SMALL ENTITY
CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	ADDIT. RATE FEE *OR*	ADDIT. RATE FEE
TOTAL: 26	MINUS 26 =	0	x $ 25 = $	x $ 50 = $ 0
INDEP: 4	MINUS 4 =	0	x $100 = $	x $200 = $ 0
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM			+ $180 = $	+ $360 = $ 0
			TOTAL ADDL. FEE $	TOTAL ADDL. FEE **$ 0**

WARNING: "After final rejection or action (§1.113) amendments may be made cancelling claims or complying with any requirement of form which has been made." 37 C.F.R. §1.116(a) (emphasis added).

(complete (c) or (d), as applicable)

(c) ☒ No additional fee for claims is required.

OR

(d) ☐ Total additional fee for claims required is $_____.

FEE PAYMENT

5. ☐ Attached is a check in the sum of $_____.

☐ Charge Account No. _____ the sum of $_____. A duplicate of this transmittal is attached.

FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986 (1065 O.G. 31-33).

6. ☒ If any additional extension and/or fee is required, charge Account No. 23-0442.

AND/OR

☒ If any additional fee for claims is required, charge Account No. 23-0442.

Signature of Practitioner

Reg. No.: **45,858**

Telephone No.: **(203) 261-1234**

Customer No.: **004955**

Andrew T. Hyman
Ware, Fressola, Van Der Sluys & Adolphson LLP
Bradford Green, Building Five
755 Main Street, P.O. Box 224
Monroe, CT 06468

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 915-005.48

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	26	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	26 minus 20=	* 6
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	108
X42=		OR	X84=	84
+140=		OR	+280=	0
TOTAL		OR	TOTAL	942

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 26	Minus	** 26	=
Independent	* 4	Minus	*** 4	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/401,338	03/26/2003	Kimmo Mylly	915-005.48	4941

4955 7590 03/23/2006

WARE FRESSOLA VAN DER SLUYS &
ADOLPHSON, LLP
BRADFORD GREEN BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/401,338	MYLLY, KIMMO	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 27 December 2005 have been fully considered but they are not persuasive.

Rejections based on 35 U.S.C. 112:

Regarding claims 2, 4, 8, 10, 12, 13, 17, and 24, applicant has argued that the word "substantially" does not necessarily render the claims indefinite.

It is the opinion of the examiner that, when taking into account the context, the word "substantially" does indeed render the claim indefinite. By way of example, claims 2 recites:

"The method of according to claim 1, wherein said first maximum value is used as a default value for the power consumption, wherein the power consumption of the peripheral device is set, at a startup stage, to be **substantially not higher** than said first maximum value."

The particular wording used by applicant ("substantially not higher") appears to communicate that the power consumption for the device is set to *any* level that is not higher than the first maximum value – e.g. the power consumption may be equal to the first maximum value, it may be somewhat lower than the first maximum value, it may be considerably lower than the first maximum value, etc. Taken as a whole, the phrase "substantially not higher" lacks clarity in regards to the level at which the power consumption is being set. As an alternative, had the applicant chosen a wording such as "not substantially higher", then the word "substantially" would not render the claim indefinite (per MPEP 2173.05(b)(D)). In the alternative wording, the limitation may read as meaning "setting the power consumption to a level marginally higher than the first maximum power value."

Rejections based on prior art:

Regarding independent claims 1, 9, 16, and 20, applicant's usage of the word "maximum" appears to lack any significant meaning in the context of the claims. By way of example, applicant has recited at least three "maximum" values for power consumption in claim 1 – a first maximum value, a second maximum value higher than the first maximum value, and a third maximum value that is between the first and second maximum values. Examiner fails to understand how all three power levels can be considered "maximum" when one of the three is higher than the other two. Since the applicant has not provided any legitimate definition for what "maximum" defines, examiner has interpreted the limitations in the broadest possible sense. As such, any prior art reference that determines a power consumption level for a peripheral device that is between a first power level and a second power level that is higher than the first power level may be considered as anticipating the limitations of these claims.

Based on this interpretation, Amoni teaches a method for determining power consumption for a peripheral device, the method comprising:

determining a first power level [Fig. 6A, step 611, 100 mA @ 5V minimum power];

determining a second power level higher than the first [max threshold, step 619];

setting a power level between the first and second power levels [step 625, col. 8, lines 30-39].

Robinson teaches:

determining a first power level [Fig. 6, step 130, col. 11, lines 31-34, standby power levels];

determining a second power level higher than the first [step 132, peak power levels];

setting a power level between the first and second power levels [step 136, reduced power level].

McKeen teaches:

determining a first power level [col. 1, lines 39-50, col. 2, lines 55-67, 8 dBm minimum power output level];

determining a second power level higher than the first [28 dBm maximum power output level];

setting a power level between the first and second power levels [setting current draw to 400 mA].

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 4, 8, 10, 12, 13, 17, and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 2, applicant has used the word "substantially" in line 5 to describe the difference in degree between a power consumption setting and a first maximum limit. The usage of "substantially" does not unambiguously limit the scope of applicant's claims. Claims 4, 8, 10, 13, 17, and 24 are also rejected on this basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 9, 10, and 14-21, are rejected under 35 U.S.C. 102(b) as being anticipated by Amoni et al., U.S. Patent No. 5,884,086[1] (claims 1, 2, 4, 9, 10, 16, 17, and 20), and Robinson, U.S. Patent No. 5,532,945 (claims 1, 3, 9, 16, and 20).

Claims 1, 9, 14-16, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by McKeen et al., U.S. Patent No. 6,785,830[2].

Regarding claim 1, each of Amoni, Robinson, and McKeen teaches:

a method for determining the power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device [Amoni, col. 2, lines 32-44, Fig. 6A/6B, Robinson, Fig. 6], wherein the method comprising determining, for the power consumption, at least a first maximum value [Amoni, Fig. 6A, step 611, Robinson, Fig. 6, step 130, col. 11, lines 31-34] and a second maximum value [Amoni, Fig. 6, step 619, max threshold, Robinson, Fig. 6, step 132, peak power] which is higher than the first maximum value, and performing, between the electronic device and the peripheral device, setting of a maximum for the power consumption of the peripheral device to a value which is between said first and second maximum values [Amoni, Fig. 6, step 625, Robinson, Fig. 6, step 136, reduced power, McKeen, col. 1, lines 39-50].

[1] Applicant-cited reference.

Regarding claim 2, Amoni teaches:

the method according to claim 1, wherein said first maximum value is used as a default value for the power consumption, wherein the power consumption of the peripheral device is set, at the startup stage, to be substantially not higher than said first maximum value [col. 8, lines 19-22].

Regarding claim 3, Robinson teaches:

the method according to claim 1, wherein said second maximum value is used as the highest allowable value for the power consumption [Fig. 6, step 132, peak power].

Regarding claim 4, Amoni teaches:

the method according to claim 1, wherein messages are transferred between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value substantially between said first maximum limit and said second maximum limit [col. 6, line 32ff, "Auxiliary Power Communication Protocol"].

Regarding claim 5, Robinson teaches:

the method according to claim 1, wherein at least one content is stored in the peripheral device, to be used in connection with the electronic device, wherein at the stage of storing the content, the power consumption set for the peripheral device is a value corresponding to said second maximum limit, and at the stage of using the content, the power consumption set for the peripheral device is a value corresponding to said first maximum limit [col. 1, line 67 to col. 2, line 3].

Regarding claims 9, 10, 16, 17, and 20, Amoni teaches the method of claims 1 and 4. Amoni also teaches the system, the electronic device, and the peripheral device to implement the claimed method.

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[2] U.S. issued patent of applicant-cited reference, WO 02/07494 A2.

Regarding claims 14, 15, 18, and 19, McKeen teaches the method of claim 1. McKeen also teaches the system and the electronic device to implement the claimed method, as recited in claims 9 and 16. McKeen also teaches that the electronic device is portable and comprises a means for performing mobile stations functions [hand-held PC and PC card radio transceiver, col. 1, lines 39-44].

Regarding claim 21, Robinson teaches the method of claims 1 and 5. Robinson also teaches the peripheral device recited in claim 20 and the storage of content recited in claim 21.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 11, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amoni in view of Yonezu et al., U.S. Patent No. 4,841,440[3].

Regarding claims 6, 11, and 22, Amoni teaches that a clock signal is generated in the device, but does not teach that the power consumption is controlled by adjusting the frequency of the clock signal.

Yonezu teaches that power consumption may be reduced by inhibiting a control clock signal for a peripheral device [abstract].

[3] Applicant-cited reference.

It would have been obvious to one of ordinary skill in the art to modify Amoni using the teachings of Yonezu. Both Amoni and Yonezu disclose methods of power control for peripheral devices. The addition of Yonezu's teaching would improve Amoni by providing a way to reduce power consumption.

Claims 7, 12, and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Amoni in view of Gupta et al., U.S. Patent No. 5,996,083.

Regarding claims 7, 12, and 23, Amoni teaches that the peripheral device comprises a bus, but does not teach controlling power consumption by controlling a width of the bus.

Gupta teaches a technique wherein power consumption in a processor is reduced by changing the width of a bus [col. 9, lines 21-32].

It would have been obvious to one of ordinary skill in the art to modify Amoni by providing a capability to modify the bus width, as taught by Gupta. The teachings of Gupta would improve the system of Amoni by reducing the number of data lines driven on the bus, thus reducing the overall power consumption.

Claims 8, 13, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson in view of Holder, Jr., U.S. Patent No. 5,892,729.

Regarding claims 8, 13, and 24, Robinson teaches that the peripheral device comprises one or more storage blocks, but does not teach the controlling of the number of storage blocks processed.

Holder teaches a memory comprising multiple storage banks which may be selectively activated [col. 3, lines 21-32].

It would have been obvious to one of ordinary skill in the art to modify Robinson by providing selectable memory banks, as taught by Holder. The teachings of Holder would improve the system of Robinson by providing selectable memory banks so as to reduce power consumption.

Regarding claim 25, it would have been obvious to one of ordinary skill in the art to store the first and second maximum values in the peripheral device.

Regarding claim 26, it would have been obvious to one of ordinary skill in the art to apply the teachings of Robinson to a multimedia card peripheral device.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

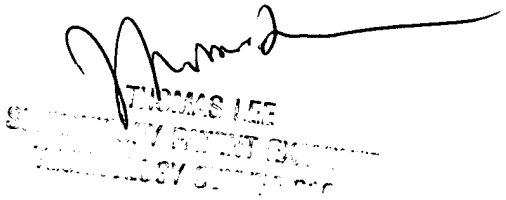
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ji H. Bae
Patent Examiner
Art Unit 2115
ji.bae@uspto.gov
571-272-7181



Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/401,338	MYLLY, KIMMO
Examiner	**Art Unit**
Ji H. Bae	2115

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	9/15/05	3/17/06							
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Bib Data Sheet

CONFIRMATION NO. 4941

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/401,338	03/26/2003 RULE	713	2115	915-005.48

APPLICANTS

Kimmo Mylly, Tampere, FINLAND;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********
FINLAND 20020594 03/27/2002

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 05/23/2003

Foreign Priority claimed ☑ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature Initials	STATE OR COUNTRY FINLAND	SHEETS DRAWING 4	TOTAL CLAIMS 26	INDEPENDENT CLAIMS 4

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TITLE
Method and a system for determining the power consumption in connection with an electronic device, and an electronic device

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time)

Kingston Exhibit 1004 - 289

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of: **Kimmo MYLLY**

U.S. Serial No.: **10/401,338** Examiner: **Ji H. Bae**

Filed: **March 26, 2003** Group Art Unit: **2115**

For: **A METHOD AND SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE**

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION AND
REQUEST FOR CONTINUED EXAMINATION

Sir:

In response to the final Office Action of March 23, 2006, applicant respectfully requests reconsideration of the rejections of the claims of the above-referenced patent application in view of the following amendments and remarks. Please amend the application as follows.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Mail Stop Amendment, the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Margery B. Hood

Margery B. Hood

Dated: June 21, 2006

06/27/2006 CNGUYEN2 00000026 10401338

02 FC:1201 400.00 OP
03 FC:1202 300.00 OP

IN THE CLAIMS:

1. (Currently Amended) A method comprising:

~~for determining~~ initiating determination of power consumption in an electronic device, to which a peripheral device is connected, ~~to~~ and from which the power is supplied to the peripheral device; ~~from the electronic device, wherein the method comprises~~

reading from a memory, ~~determining, for~~ in order to determine a maximum of the power consumption, at least a first maximum limiting value and a second maximum limiting value which is higher than the first maximum limiting value; ~~value,~~ and

~~performing, between the electronic device and the peripheral device, setting of a maximum for~~ setting the maximum of the power consumption ~~of the peripheral device~~ to a value which is between said first and second maximum limiting values.

2. (Currently Amended) The method according to claim 1,

wherein said first maximum limiting value is used as a default value for the power consumption, and

wherein the power consumption of the peripheral device is set, at a startup stage, to be ~~substantially not higher~~ not substantially higher than said first maximum limiting value.

3. (Currently Amended) The method according to claim 1, wherein said second maximum limiting value is used as a highest allowable value for the power consumption.

4. (Currently Amended) The method according to claim 1, wherein messages are transferred between the electronic device and the peripheral device for setting the maximum of the power consumption of the peripheral device to a value substantially between said first maximum limiting value and said second maximum limiting value.

5. (Currently Amended) The method according to claim 1, wherein at least one content is stored in the peripheral device, for use in connection with the electronic device, wherein at a stage of storing the content, the power consumption set for the peripheral device is a value corresponding to said second maximum limiting value, and at a stage of using the content, the power consumption set for the peripheral device is a value corresponding to said first maximum limiting value.

6. (Previously Presented) The method according to the claim 1, wherein at least one clock signal is generated in the peripheral device and wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

7. (Previously Presented) The method according to the claim 1, wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling a width of said bus.

8. (Currently Amended) The method according to the claim 1, wherein the peripheral device is provided with two or more storage blocks [[(2)]] controlled by controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

9. (Currently Amended) A system comprising

a peripheral device;

an electronic device with means for connecting ~~a peripheral~~ the peripheral device and means for supplying power to the peripheral device, and ~~which system comprises~~

means for determining power consumption,

wherein at least a first maximum limiting value and a second maximum limiting value which is higher than the first maximum limiting value are ~~defined~~ stored for the power consumption, and

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is between said first maximum limiting value and second maximum limiting value.

10. (Currently Amended) The system according to claim 9, further comprising means for transferring messages between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value substantially between said first maximum limiting value and said second maximum limiting value.

11. (Previously Presented) The system according to claim 9, wherein the peripheral device comprises means for generating at least one clock signal, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

12. (Previously Presented) The system according to claim 9,

wherein the peripheral device comprises at least one bus, and

wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting a bus width of the peripheral device.

13. (Currently Amended) The ~~method~~ system according to the claim 9,

wherein the peripheral device is provided with two or more storage blocks, and

wherein the means for controlling the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

14. (Previously Presented) The system according to the claim 9, wherein the electronic device is a portable electronic device .

15. (Currently Amended) The system according to claim 14, further comprising means for performing mobile station functions.

16. (Currently Amended) An electronic device ~~provided with~~ comprising:

means for connecting a peripheral ~~device and~~ device;

means for supplying power to the peripheral ~~device,~~ device; and

means for determining power consumption,

wherein at least a first maximum limiting value and a second maximum limiting value which is higher than the first maximum limiting value are defined for the power consumption, and

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is between said first maximum limiting value and said second maximum limiting value.

17. (Currently Amended) The electronic device according to claim 16, further comprising

means for transmitting messages from the peripheral device and for receiving messages to the peripheral device, to set the maximum power consumption of the peripheral device to a value substantially between said first maximum limiting value and said second maximum limiting value.

18. (Previously Presented) The electronic device according to claim 16, wherein it is a portable electronic device.

19. (Currently Amended) The electronic device according to claim 18, further comprising means for performing mobile station functions.

20. (Currently Amended) A peripheral device comprising: ~~provided with~~

means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein at least a first maximum limiting value and a second maximum limiting value which is higher than the first maximum limiting value, are defined for power consumption, and

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is between said first maximum limiting value and said second maximum limiting value.

21. (Previously Presented) The peripheral device according to claim 20, wherein at least one content is stored in the peripheral device for use in connection with the electronic device.

22. (Currently Amended) The peripheral device according to claim 20, further comprising

means for generating at least one clock signal and

means for controlling the power consumption of the peripheral device by frequency control of said at least one clock signal.

23. (Currently Amended) The peripheral device according to claim 20, further comprising

at least one bus and

means for controlling the power consumption of the peripheral device by controlling a bus width of said bus of the peripheral device.

24. (Currently Amended) The peripheral device according to the claim 20,

wherein the peripheral device is provided with two or more storage blocks, and

~~that~~ wherein the means for controlling the power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

25. (Currently Amended) The peripheral device according to the claim 20, wherein said first maximum limiting value and said second maximum limiting value are stored in the peripheral device.

26. (Previously Presented) The peripheral device according to the claim 20, wherein said peripheral device is a MultiMediaCard™ peripheral device.

27. (New) An electronic device comprising:

a connector configured to connect a peripheral device;

a power supply configured to supply power to the peripheral device; and

a power gauge configured to determine power consumption,

wherein at least a first maximum limiting value and a second maximum limiting value which is higher than the first maximum limiting value are defined for the power consumption, and

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is between said first maximum limiting value and said second maximum limiting value.

28. (New) The electronic device according to claim 27, further comprising

a transceiver configured to transmit messages from the peripheral device and for receiving messages to the peripheral device, to set the maximum power consumption of the peripheral device to a value substantially between said first maximum limiting value and said second maximum limiting value.

29. (New) A peripheral device comprising:

a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,

wherein at least a first maximum limiting value and a second maximum limiting value which is higher than the first maximum limiting value, are defined for power consumption, and

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is between said first maximum limiting value and said second maximum limiting value.

30. (New) The peripheral device according to the claim 29, wherein said first maximum limiting value and said second maximum limiting value are stored in the peripheral device.

31. (New) The electronic device according to claim 27, wherein it is a portable electronic device.

32. (New) The electronic device according to claim 27, further comprising a memory configured to store the first maximum limiting value and the second maximum limiting value.

REMARKS

The independent claims are claims 1, 9, 16, and 20 plus new claims 27 and 29. Claims 1-26 are rejected. Claims 1-32 are now pending. All of the present amendments are fully supported by the specification as originally filed, and introduce no new matter.

Amended Claim 2 is Not Indefinite

Claim 2 is now amended to state that the power consumption is "not substantially higher than a maximum" (instead of "substantially not higher"). This wording was suggested in the final Office Action, at page two.

Regarding claims 4, 8, 10, 12, 13, 17, and 24 rejected under 35 U.S.C. § 112, Applicant respectfully refers to MPEP § 2173.05(b)(D) which states that the term "substantially" is often used in a claim without rendering the claim indefinite. Applicant therefore traverses these indefiniteness rejections, for the reasons provided at MPEP § 2173.05(b)(D).

The Amended Independent Claims are not Anticipated by the Cited Prior Art

Independent claims 1, 9, 16, and 20 are rejected as anticipated under 35 U.S.C. § 102 by *Amoni* (U.S. Patent No. 5,884,086), and also *Robinson* (U.S. Patent No. 5,532,945), and also *McKeen* (U.S. Patent No. 6,785,830). However, the independent claims are now amended to clarify the meaning of the word "maximum."

As seen in amended claim 1, for example, it is now clarified that the first value and the second value are limiting values for the maximum, the maximum being not yet set. Then the maximum is set, so that it falls between the limiting values. Claim 1 also clarifies that the first value and the second value are read from a memory. As indicated in claim 25, the memory may be located in the peripheral device.

The present invention is very useful when a peripheral device comes into contact with an electronic device that supplies power to the peripheral device. The peripheral device provides a range within which the maximum power consumption must fall, and the maximum power consumption is then determined, e.g. by the interaction described in claim 4.

The idea that the first and second maximum limiting values are stored is discussed, for example, at page 8, line 23 of the application (also see page 13 discussing that a memory card may be used at the peripheral device). Also, at least page 8, line 22 discusses that the first and second values are "maximum limits" (from between which the maximum will be selected).

The *Amoni* reference discloses a system and a method for supplying power to a peripheral device in a computer system. According to *Amoni*, the peripheral device instructs the main device to provide the necessary power to the peripheral device. The power level is not adjusted (handshaked) but the peripheral device is supplied with the power level it needs. In the main device there are switches for selecting a certain, fixed power level (col. 2, lines 40—44). The *Amoni* document does not mention anything about a maximum level, nor does it mention anything about using a certain value for the power level which is less than or equal to a maximum value. Moreover, the *Amoni* document does not teach anything about adjusting the power level to a value which is between two different maximum values.

McKeen discloses a radio modem card which is intended to be used in connection with a portable PC device. The maximum transmission power of the radio modem card is adjusted to a value which is between two different power levels defined in a standard of a mobile communication system. The maximum transmission power is within allowed tolerances. The limitation of the transmission power is implemented so that the maximum current consumption of the power amplifier of the radio modem card is limited to a certain maximum value. This maximum value is defined in such a way that the total current consumption of the radio modem card does not exceed a predetermined value. The aim of this arrangement is to prevent the radio modem card from overloading the PC device from which the power is supplied to the radio modem card. This is necessary because, according to the example disclosed in *McKeen*, batteries are used as the power source of the PC device and the current which can be supplied from the batteries is limited.

McKeen discloses the limitation of the transmission power between two standard values. This non-standard transmission power level is defined on the basis of how much power the power source of the PC device can supply to the radio modem card. The non-

standard power level is thus set to such value which allows the use of the maximum available current from the PC device. Therefore, a separate power source is not needed in the radio modem card to enable the use of the maximum transmission power of the radio modem card.

The solution of *McKeen* is quite different from the solution of the present claimed invention. In the present application, at least a first and a second maximum values are defined for the power consumption, and the maximum of the power consumption is set to a value which is substantially between said first and second maximum value. In the system of *McKeen* the portable PC device does not affect the adjustment of the transmission power of the radio modem card. In other words, in the system of *McKeen* no actions are taken between the PC device and the radio modem card to set the power consumption of the radio modem card. This means that the radio modem card always sets its power consumption to a certain value independent of the device to which the radio modem card is connected. Further, the adjustment of the transmission power and the adjustment of the power consumption are not the same issue. The adjustment of the transmission power determines how much power can be transmitted from the card and the adjustment of the power consumption determines how much power the card itself draws from the power source. The standard maximum power levels for the transmission power do not determine any limits for the power consumption of the card.

The Applicant also respectfully points out that the limitation of the transmission power of power amplifier of the radio modem card does not directly limit the power consumption of the radio modem card. It may happen that although the transmission power is limited, the power consumption of the radio modem card may still vary due to alterations in the power consumption of other electronics of the radio modem card. In the solution disclosed by *Robinson*, a "power resource table" stored at the host is used, which table is updated and it can be read by the card.

On page 6 of the Office Action, several dependent claims are rejected in view of *Yonezu* (US Patent No. 4,841,440), or in view of *Gupta* (U.S. Patent No. 5,996,083), or in view of *Holder* (U.S. Patent No. 5,892,729). *Yonezu* discloses a solution where the idle/standby power consumption is controlled to the minimum. *Holder* discloses power consumption by controlling the clock connecting to different integrated circuits. *Gupta*

also discloses a solution which seems to comprise two-way handshakes. There is a register on the host side, according to which the external device controls its function (the document mentions controlling the bandwidth as one way to decrease power consumption if the host register indicates a smaller maximum consumption than what is required for the external device).

Because all of the present independent claims should be allowable, the claims depending therefrom should also be allowable, notwithstanding *Yonezu, Gupta, and Holder.*

Further Comments About the Present Application

The invention of the present application provides an improved method and system for determining the power consumption to be suitable in each situation. The invention is based on the idea that at least a first and a second maximum value are determined for the power consumption, wherein the electronic device and the peripheral device set the power consumption to a value between these first and second maximum values. Thus, in different operating situations, for example the peripheral device can adjust its power consumption to be suitable for the situation.

By the method according to the invention, it is possible to avoid the use of an unnecessarily large regulator in an electronic device, which saves costs, and wherein the size of the electronic device can, in some cases, be reduced and, on the other hand, problems of heating caused by high power consumption can be avoided. Also the power consumption can be reduced, which is advantageous particularly in portable devices. By means of the invention, the peripheral device connection can also be provided with flexibility, because the power consumption of the peripheral device can be adjusted and set to a value suitable for each situation of use. Furthermore, the invention makes it possible that new peripheral devices to be developed will function in connection with electronic devices made earlier, and existing peripheral devices will function in connection with new electronic devices to be developed. None of these advantages can be achieved by the cited references.

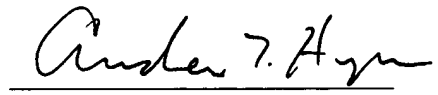
CONCLUSION

Thus, the Examiner is asked to kindly reconsider the Office Action in the light of the arguments presented herein, and to correspondingly issue a favorable Office Action at the next stage of the proceedings. The present amendments raise no new issues, and introduce no new matter.

Early allowance of all independent claims (and the pending claims depending therefrom) is earnestly solicited. Applicant would be grateful if the Examiner would please contact Applicant's attorney by telephone if the Examiner detects anything in the present response that might impede a speedy allowance.

Respectfully submitted,

Dated: June 21, 2006



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USPTO Customer No. 004955

RCE

Practitioner's Docket No. 915-005.048 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: K. Mylly
Application No.: 10/401,338 Group No.: 2115
Filed: March 26, 2003 Examiner: J. Bae
For: Method and System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device

Commissioner for Patents
Washington, D.C. 20231

REQUEST FOR CONTINUED EXAMINATION (RCE)
(37 C.F.R. § 1.114)

1. Applicant hereby requests continued examination, in accordance with 37 C.F.R. § 1.114, for the above identified application.

NOTE: 37 C.F.R. § 1.114 Request for continued examination:

"(a) If prosecution in an application is closed, an applicant may request continued examination of the application by filing a submission and the fee set forth in § 1.17(e) prior to the earliest of:

(1) Payment of the issue fee, unless a petition under § 1.313 is granted;

(2) Abandonment of the application; or

(3) The filing of a notice of appeal to the U.S. Court of Appeals for the Federal Circuit under 35 U.S.C. 141, or the commencement of a civil action under 35 U.S.C. 145 or 146, unless the appeal or civil action is terminated.

(b) Prosecution in an application is closed as used in this section means that the application is under appeal, or that the last Office action is a final action (§ 1.113), a notice of allowance (§ 1.311), or an action that otherwise closes prosecution in the application.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*
*(When using Express Mail, the Express Mail label number is **mandatory**; Express Mail certification is optional.)*

I hereby certify that, on the date shown below, this correspondence is being:

MAILING

☒ deposited with the United States Postal Service in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231

37 C.F.R. § 1.8(a)

☒ with sufficient postage as first class mail.

37 C.F.R. § 1.10 *

☐ as "Express Mail Post Office to Addressee"
Mailing Label No. _____ **(mandatory)**

TRANSMISSION

☐ facsimile transmitted to the Patent and Trademark Office, (703) _____-_____

Date: 6/21/06

Margery B. Hood
Signature

Margery B. Hood
(type or print name of person certifying)

** Only the date of filing (§ 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under § 1.8 continues to be taken into account in determining timeliness. See § 1.703(f). Consider "Express Mail Post Office to Addressee" (§ 1.10) or facsimile transmission (§ 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

(c) A submission as used in this section includes, but is not limited to, an information disclosure statement, an amendment to the written description, claims, or drawings, new arguments, or new evidence in support of patentability. If reply to an Office action under 35 U.S.C. 132 is outstanding, the submission must meet the reply requirements of § 1.111.

(d) If an applicant timely files a submission and fee set forth in § 1.17(e), the Office will withdraw the finality of any Office action and the submission will be entered and considered. If an applicant files a request for continued examination under this section after appeal, but prior to a decision on the appeal, it will be treated as a request to withdraw the appeal and to reopen prosecution of the application before the examiner. An appeal brief under § 1.192 or a reply brief under § 1.193(b), or related papers, will not be considered a submission under this section."

NOTE: An applicant may file a submission under 37 CFR 1.114 containing only an information disclosure statement (37 CFR 1.97 and 1.98) in an application subject to a notice of allowance under 35 U.S.C. § 151. An appeal brief or a reply brief (or related papers) will not be considered a submission under 37 CFR 1.114. See 37 CFR 1.114(d). The submission, however, may consist of the arguments in a previously filed appeal brief or reply brief, or may simply consist of a statement that incorporates by reference the arguments in a previously filed appeal brief or reply brief. In addition, a previously filed amendment after final may satisfy this submission requirement. American Inventor's Protection Act of 1999, Question & Answer A5.

NOTE: Even though an RCE is improper (e.g., because it was filed before the prosecution is closed), an amendment submitted with the RCE will still be entered and considered by the examiner since it was timely filed and responsive to the non-final Office action in compliance with 37 CFR 1.111. American Inventor's Protection Act of 1999, Question & Answer A4.

***WARNING:** 35 U.S.C. 132(b) and § 1.114 provide for the continued examination of an application and **not** examination of a continuing application). Accordingly, the Office will not permit an applicant to obtain continued examination on the basis of claims that are independent and distinct from the claims previously claimed and examined. Notice of March 10, 2000, 65 Fed Reg 14865, at 14868.*

***WARNING:** The provisions of 37 CFR 1.114 also do not apply (1) to a provisional application; (2) an application for a utility or plant patent filed under 35 U.S.C. 111(a) before June 8, 1995; (3) an international application filed under 35 U.S.C. 363 before June 8, 1995; (4) a patent under reexamination or (5) an application for a design patent. 37 CFR § 1.114(e).*

***WARNING:** The PTO has pointed out why § 1.97(b) does not provide that an information disclosure statement will be considered if it is filed within three months after the date of a request for continued examination under § 1.114. The PTO explained that since an RCE filing is a reply under 35 U.S.C. 132, the applicant may be entitled to patent term adjustment if the Office does not act on an application containing a request for continued examination under § 1.114 within four months. See 35 U.S.C. 154(b)(1)(A)(ii). Thus, the Office cannot delay action on RCE applications for three months to determine whether an information disclosure statement will be filed. The Office, however, is adopting provisions (§ 1.103(c)) for a limited suspension of action after the filing of a request for continued examination under § 1.114, for the applicant to obtain additional time (prior to the issuance of the next Office action) to provide an information disclosure statement (or amendments, or an affidavit or declaration) after the filing of the RCE. See, Notice of August 16, 2000, "Request for Continued Examination Practice and Changes to Provisional Application Practice; Final Rule", 65Fed. Reg., pages 50091-50105, at page 50100 (comment 11); OG: September 5, 2000, pages 13-24*

***WARNING:** One of the time periods excluded from patent term adjustment is the time consumed by a continued examination request under 35 U.S.C. 132(b) (§ 1.114(b) (1)).*

***WARNING:** The Office will not suspend action in an application when a reply by the applicant is outstanding. 35 U.S.C. 133 requires an applicant to "prosecute the application" within six months of an Office action (or a shorter period as set in the Office action) to avoid abandonment of the application. If an applicant files a request for continued examination but does not also provide any submission (in reply to the prior Office action) within the period for reply to the prior Office action, the application is abandoned by operation of law (35 U.S.C. 133).*

The Office will treat a request for continued examination under § 1.114 containing a bona fide submission that is not fully responsive to the prior Office action under the practice set forth in § 1.135(c). In addition, under the limited suspension of action provisions of § 1.103(c), an applicant must still file a request for continued examination practice in compliance with § 1.114, but may obtain additional time (prior to the issuance of the next Office action) to provide an information disclosure statement, amendments, or an affidavit or declaration after the filing of the request for continued examination.

See, Notice of August 16, 2000, "Request for Continued Examination Practice and Changes to Provisional Application Practice; Final Rule", 65Fed. Reg., pages 50091-50105, at page 50102 (comment 20); OG: September 5, 2000, pages 13-24] Page 50102

WARNING: *Section 1.97(b) does not provide that an information disclosure statement will be considered if it is filed within three months after the date of a request for continued examination under § 1.114.*

NOTE: There is no limit to the number of times the fee for continued examination may be submitted. Notice of March 10, 2000, 65 Fed Reg 14865, at 14868.

NOTE: Unlike a continuation application, a continued examination request ***can*** *utilize the mailing procedure of 37 CFR 1.8. See 37 CFR § 1.8(a)(2)(i)(A).*

Continued Prosecution Request Fee $ 790.00

TIME REQUEST IS BEING MADE

2. This request is being submitted *(check appropriate item(s) below):*

i ☒ Prior to abandonment of the application

ii. ☐ Payment of the issue fee

- ☐ Prior to payment of issue fee
- ☐ Issue fee has been paid but a petition under § 1.313 has been granted

iii. ☐ Prior to a decision on appeal to the Board of Patent Appeals & Interferences

- ☐ A notice is being separately sent to the Board of Patent Appeals & Interferences that this Request for Continued Examination is being filed.

NOTE: If such a notice is not sent to the Board then may refuse to vacate a decision rendered after the filing of the RCE but before recognition by the Office of the RCE request under § 1.114.

iv. ☐ Appeal to the U.S. Court of Appeals of the Federal Circuit under 35 U.S.C. 145 or ☐ Commencement of a civil action under 35 U.S.C. 146

- ☐ Prior to the filing of such appeal or commencement of civil action
- ☐ Such appeal or commencement of civil action has been terminated

ENCLOSURES

3. Enclosed herewith is/are:

WARNING: *If reply to a final or non-final Office action under 35 U.S.C. 132 is outstanding, the submission must meet the reply requirements of § 1.111. 37 C.F.R. § 1.114(b).*

☐ An information disclosure (37 C.F.R. § 1.98)

- ☐ Form PTO-1449 (PTO/SB/08A and 08B)

☒ An amendment

☒ New arguments

☐ New evidence in support of patentability

☐ Other:

Continued Prosecution Request Fee $ 790.00

FEE FOR REQUEST (37 C.F.R. § 1.17(e)).

4. This application is on behalf of:

☐ Small entity (and status is still as small entity) $375.00

☐ Other than a small entity $790.00

FEE FOR CLAIMS

NOTE: "The fee for continued examination under § 1.114 (§ 1.17(e)) does not include additional claims fee (cf. 1.53 (d)(3)(ii))." See Notice of March 10, 2000, 65 Fed Reg 14865, at 14868.

37 CFR 1.53(d)(3): "The filing fee for a continued prosecution application filed under this paragraph is:

(i) The basic filing fee as set forth in § 1.16; and

Any additional § 1.16 fee due based on the number of claims remaining in the application after entry of any amendment accompanying the request for an application under this paragraph and entry of any amendments under § 1.116 unentered in the prior application which applicant has requested to be entered in the continued prosecution application."

5. The fee for claims (37 C.F.R. § 1.16(b)-(d)) has been calculated as shown below:

	(Col. 1)		(Col. 2)		(Col. 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR		PRESENT EXTRA	RATE	ADDIT. FEE	*OR*	RATE	ADDIT. FEE
TOTAL	* 32	MINUS	** ~~36~~	=	6	x$9 =	$		x$~~50~~	$ 300.00
INDEP.	* 6	MINUS	*** 4	=	2	x$42 =	$		x$~~200~~	$ 400.00
☐FIRST PRESENTATION OF MULTIPLE DEP. CLAIM						+$140 =	$		+$280 =	$
						TOTAL ADDIT. FEE	$	*OR*	TOTAL ADDIT. FEE	$ 700.00

* If the entry in Col. 1 is less than entry in Col. 2, write "0" in Col. 3.

** If the "Highest No. Previously Paid for" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest No. Previously Paid For" (Total or Indep.) is the highest number found in the appropriate box in Col. 1 of a prior amendment or the number of claims originally filed.

WARNING: *See 37 C.F.R. § 1.116.*

(complete (a) or (b), as applicable)

(a) ☐ No additional fee is required.

OR

(b) ☒ Total additional fee required is $ 700.00 .

EXTENSION OF TIME

(If an extension of time is appropriate complete (a) or (b), as applicable)

6. The proceedings herein are for a patent application, and the provisions of 37 C.F.R. § 1.136(a) apply.

NOTE: 37 C.F.R. § 1.704(b) ". . .an applicant shall be deemed to have failed to engage in reasonable efforts to conclude processing or examination of an application for the cumulative total of any periods of time in excess of three months that are taken to reply to any notice or action by the Office making any rejection, objection, argument, or other request, measuring such three-month period from the date the notice or action was mailed or given to the applicant, in which case the period of adjustment set forth in § 1.703 shall be reduced by the number of days, if any, beginning on the day after the date that is three months after the date of mailing or transmission of the Office communication notifying the applicant of the rejection, objection, argument, or other request and ending on the date the reply was filed. The period, or shortened statutory period, for reply that is set in the Office action or notice has no effect on the three-month period set forth in this paragraph."

(a) ☐ Applicant petitions for an extension of time, the fees for which are set out in 37 C.F.R. § 1.17(a)(1)-(4), for the total number of months checked below:

Extension for (months)	Fee for other than small entity	Fee for small entity
☐ one month	$ 110.00	$ 55.00
☐ two months	$ 410.00	$ 205.00
☐ three months	$ 930.00	$ 465.00
☐ four months	$ 1,450.00	$ 725.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

OR

(b) ☒ Applicant believes that no extension of time is required. However, this is a conditional petition and authorization to pay the necessary fees to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

TOTAL FEE(S) DUE

WARNING: *The fee for continued examination under § 1.114 may not be deferred. 37 C.F.R. § 1.53(f).*

7. The total fee(s) due is/are:

Continued Prosecution Fee (§ 1.17(e))	$ 790.00
Fee(s) for additional claims (if any) (§ 1.16(b)-(d))	$ 700.00
Extension of time fee (if any) (§ 1.17(a)(1)-(4))	$ _____
Total Fee(s) Due	$ 1,490.00

PAYMENT OF FEE(S) DUE

8. Please pay the fee(s) for this continued examination application as follows:

☒ Check is attached for the sum of $ 1,490.00

☐ Charge Account _____ the sum of $ _____

☐ Charge Credit Card the sum of $ _____

(Credit Card Payment Form (PTO-2038) attached)

Please charge any required additional fee(s) for § 1.17(e), § 1.16(b)-(d) and/or § 1.17(a)(1)-(4) to

☒ Account 23-0442

☐ Credit Card (Credit Card Payment Form (PTO-2038) attached).

INVENTORSHIP

NOTE: Any change of inventors must be via the procedure set forth in 37 CFR § 1.48. See Notice of March 10, 2000, 65 Fed Reg 14865, at 14868.

9. This application as amended names as inventors:

☐ the same inventors as previously designated for the claims.

☐ fewer than the inventors previously designated ans a statement accompanies this request for the deletion of the name or names of the person or persons who are not inventors of the invention now being claimed.

☐ a person not named previously as an inventor and a petition under 37 C.F.R. § 1.48 is/has separately: ☐ being filed ☐ been filed

DEFERRAL OF EXAMINATION

10. ☐ A request for deferral of examination accompanies this request for continued examination.

Reg. No.: 45,858

Andrew T. Hyman
SIGNATURE OF PRACTITIONER

Tel. No.: (203) 261-1234

Andrew T. Hyman
(type or print name of practitioner)

Customer No.: 004955

WARE, FRESSOLA, VAN DER SLUYS
P.O. Address & ADOLPHSON LLP

755 Main Street, PO Box 224
Monroe CT 06468

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number
10/140,338
915-005.48

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	26	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	26 minus 20=	* 6
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	108
X42=		OR	X84=	84
+140=		OR	+280=	0
TOTAL		OR	TOTAL	942

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 26	Minus	** 26	=
Independent	* 4	Minus	*** 4	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

6-26-04

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 32	Minus	** 26	= 6
Independent	* 6	Minus	*** 4	= 2
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18= 50	300
X42=		OR	X84= 200	400
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	700

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/401,338	03/26/2003	Kimmo Mylly	915-005.48	4941

4955 7590 07/14/2006

WARE FRESSOLA VAN DER SLUYS &
ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/401,338	MYLLY, KIMMO	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see page 9 of applicant's remarks, filed on 26 June 2006, with respect to rejection of claims 2, 4, 8, 10, 12, 13, 17, and 24 under 35 U.S.C. 112 have been fully considered and are persuasive. The rejection of the claims has been withdrawn.

Applicant's arguments filed on 26 June 2006 with respect to prior art rejections have been fully considered but they are not persuasive.

Applicant has amended the claims and offered a number of arguments to clarify the meaning of the word "maximum" as used in the claims. In particular, applicant has amended the "first maximum value" and "second maximum value" to read as a "first maximum limiting value" and a "second maximum limiting value". Applicant presented the argument that the first and second values are limiting values for the maximum value [applicant's remarks, page 9, fifth paragraph]. In addition, applicant has presented the argument that the maximum value for the power consumption is set to be between the first limiting value and second limiting value.

Notwithstanding applicant's arguments and amendments, the usage of "maximum" remains problematic in applicant's claims. With respect to the first and second values, the examiner points out that by applicant's own admission, these values are merely limiting values for the maximum value, and not the maximum value themselves. As such, the usage of "maximum" to describe these limits is superfluous at best, and confusing at worst, as the word "maximum" appears to describe the limit (as opposed to the power consumption value being set). Examiner recommends amending the limitations to read "a first limiting value for the power consumption" and "a second limiting value for the power consumption."

In addition to the limit values, applicant's usage of "maximum" to describe the power settings also remains problematic. Applicant's disclosure teaches that the "maximum" power

consumption may occupy a range between the first and second limiting values, and that the maximum power consumption setting is fixed using applicant's inventive method. However, examiner points out that once the power setting is fixed, then to call the fixed power setting a "maximum" power consumption value is meaningless, since according to applicant's own teaching the power consumption remains static for the duration of the most recent setting. Applicant does appear to teach that the power consumption is variable, but only by **changing** the setting, and not once the setting has been fixed. Unless the power consumption setting is set to the highest limit value, or unless the power consumption may vary once the setting has been made, there appears to be no reasonable justification for labeling the power consumption setting as a maximum. As such, the word "maximum" lacks any significant meaning in the context of the claims.

For these reasons, the rejection of the claims based on Robinson, U.S. Patent No. 5,532,945, remains valid. In particular, Robinson teaches a first and second limiting value for power consumption, and the setting of the power consumption to a value between the limiting values [Fig. 6]. Since the power consumption of Robinson is fixed based on the most recent setting, Robinson also teaches the "maximum" power setting taught by applicant.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by Robinson, U.S. Patent No. 5,532,945.

Regarding claim 1, Robinson teaches a method comprising [Fig. 6]:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device;

reading from a memory [CIS, col. 11, lines 31-34], in order to determine a maximum of the power consumption, at least a first maximum limiting value and a second maximum limiting value [peak and standby values]; and

setting the maximum of the power consumption to a value which is between said first and second maximum limiting values [step 136, reduced power].

Regarding claim 2, Robinson teaches that the first maximum limiting value is a default value, and that the power consumption settings are set to the default upon reset [col. 9, lines 57-64].

Regarding claim 3, Robinson teaches that the second maximum limiting value is used as a highest allowable value for the power consumption.

Regarding claim 4, Robinson teaches that messages are transferred between the peripheral device and the electronic device for setting the maximum power consumption value [col. 11, lines 35-50, request_power_function and success return codes].

Regarding claim 5, Robinson teaches at least one content is stored in the peripheral device, to be used in connection with the electronic device, wherein at the stage of storing the content, the power consumption set for the peripheral device is a value corresponding to said second maximum limiting value, and at the stage of using the content, the power consumption set for the peripheral device is a value corresponding to said first maximum limiting value [col. 1, ,line 65 to col. 2, line 7].

Regarding claims 9, 10, 14-21, 25, and 27-32 Robinson teaches the method of claims 1-5, and also the system and device to implement the claimed method. Robinson also teaches

that the peripheral device is a portable electronic device [Fig. 1, removable flash card, fax/modem card], and that the peripheral device performs mobile station functions [fax/modem card, Fig. 1].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 11, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson in view of Yonezu et al., U.S. Patent No. 4,841,440[1].

Regarding claims 6, 11, and 22, Robinson teaches the method of claim 1, but does not teach that the power consumption is controlled by adjusting the frequency of a clock signal.

Yonezu teaches that power consumption may be reduced by inhibiting a control clock signal for a peripheral device [abstract].

It would have been obvious to one of ordinary skill in the art to modify Robinson using the teachings of Robinson. Both Robinson and Yonezu disclose methods of power control for peripheral devices. The addition of Yonezu's teaching would improve Robinson by providing a way to reduce power consumption.

[1] Applicant-cited reference.

Claims 7, 12, and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson in view of Gupta et al., U.S. Patent No. 5,996,083.

Regarding claims 7, 12, and 23, Robinson teaches the method of claim 1, but does not teach controlling power consumption by controlling a width of a bus.

Gupta teaches a technique wherein power consumption in a processor is reduced by changing the width of a bus [col. 9, lines 21-32].

It would have been obvious to one of ordinary skill in the art to modify Robinson by providing a capability to modify the bus width, as taught by Gupta. The teachings of Gupta would improve the system of Robinson by reducing the number of data lines driven on the bus, thus reducing the overall power consumption.

Claims 8, 13, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson in view of Holder, Jr., U.S. Patent No. 5,892,729.

Regarding claims 8, 13, and 24, Robinson teaches that the peripheral device comprises one or more storage blocks, but does not teach the controlling of the number of storage blocks processed.

Holder teaches a memory comprising multiple storage banks which may be selectively activated [col. 3, lines 21-32].

It would have been obvious to one of ordinary skill in the art to modify Robinson by providing selectable memory banks, as taught by Holder. The teachings of Holder would improve the system of Robinson by providing selectable memory banks so as to reduce power consumption.

Regarding claim 25, it would have been obvious to one of ordinary skill in the art to store the first and second maximum values in the peripheral device.

Regarding claim 26, it would have been obvious to one of ordinary skill in the art to apply the teachings of Robinson to a multimedia card peripheral device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae
Patent Examiner
Art Unit 2115
ji.bae@uspto.gov
571-272-7181

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10401338	MYLLY, KIMMO
Examiner	**Art Unit**
Bae, Ji H	2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	7/6/2006								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
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	31	✓								
	32	✓								

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Bib Data Sheet

CONFIRMATION NO. 4941

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/401,338	03/26/2003 RULE	713	2115	915-005.48

APPLICANTS
Kimmo Mylly, Tampere, FINLAND;

**** CONTINUING DATA **************************

**** FOREIGN APPLICATIONS *********************
FINLAND 20020594 03/27/2002

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 05/23/2003

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☑ yes ☐ no	FINLAND	4	26 32	4/6
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials				

ADDRESS
4955

TITLE
Method and a system for determining the power consumption in connection with an electronic device, and an electronic device

FILING FEE RECEIVED		
1642	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Kingston Exhibit 1004 - 319

TIW 2115

915-005.048

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of: **Kimmo MYLLY**

U.S. Serial No.: **10/401,338** Examiner: **Ji H. Bae**

Filed: **March 26, 2003** Group Art Unit: **2115**

For: **A METHOD AND SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE**

Mail Stop Amendment – No Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION

Sir:

In response to the non-final Office Action of July 14, 2006, applicant respectfully requests reconsideration of the rejections of the claims of the above-referenced patent application in view of the following amendments and remarks. Please amend the application as follows.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Margery B. Hood
Margery B. Hood

Dated: Oct. 11, 2006

IN THE CLAIMS:

1. (Currently Amended) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device;

setting the power consumption of the peripheral device at a startup stage to a default value;

reading from a memory, in order to determine a maximum of the power consumption, at least a ~~first maximum~~ limiting value ~~and a second maximum limiting value~~ which is higher than ~~the first maximum limiting~~ said default value; and

setting the maximum of the power consumption to a value which is ~~between~~ in a range from said ~~first~~ default value to said ~~and second maximum~~ limiting ~~values~~ value, wherein the range includes said default value and said limiting value.

2. CANCEL.

3. (Currently Amended) The method according to claim 1, wherein said ~~second maximum~~ limiting value is used as a highest allowable value for the power consumption.

4. (Currently Amended) The method according to claim 1, wherein messages are transferred between the electronic device and the peripheral device for setting the maximum of the power consumption of the peripheral device to a value ~~substantially between said first maximum limiting value and said second maximum limiting value~~ in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value.

5. (Currently Amended) The method according to claim 1, wherein at least one content is stored in the peripheral device, for use in connection with the electronic device, wherein at a stage of storing the content, the power consumption set for the peripheral device is a value

corresponding to said ~~second maximum~~ limiting value, and at a stage of using the content, the power consumption set for the peripheral device is a value corresponding to said ~~first maximum limiting~~ default value.

6. (Previously Presented) The method according to the claim 1, wherein at least one clock signal is generated in the peripheral device and wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

7. (Previously Presented) The method according to the claim 1, wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling a width of said bus.

8. (Previously Presented) The method according to the claim 1, wherein the peripheral device is provided with two or more storage blocks controlled by controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

9. (Currently Amended) A system comprising

a peripheral device;

an electronic device with means for connecting the peripheral device and means for supplying power to the peripheral device, and

means for determining power consumption,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a ~~first maximum~~ limiting value ~~and a second maximum limiting value~~ which is higher than ~~the first maximum limiting~~ said default value ~~are~~ is stored for the power consumption, and

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value. ~~between said first maximum limiting value and second maximum limiting value~~.

10. (Currently Amended) The system according to claim 9, further comprising means for transferring messages between the electronic device and the peripheral device for setting the power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value ~~substantially between said first maximum limiting value and said second maximum limiting value~~.

11. (Previously Presented) The system according to claim 9, wherein the peripheral device comprises means for generating at least one clock signal, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

12. (Previously Presented) The system according to claim 9,

wherein the peripheral device comprises at least one bus, and

wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting a bus width of the peripheral device.

13. (Previously Presented) The system according to the claim 9,

wherein the peripheral device is provided with two or more storage blocks, and

wherein the means for controlling the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

14. (Previously Presented) The system according to the claim 9, wherein the electronic device is a portable electronic device .

15. (Previously Presented) The system according to claim 14, further comprising means for performing mobile station functions.

16. (Currently Amended) An electronic device comprising:

means for connecting a peripheral device;

means for supplying power to the peripheral device; and

means for determining power consumption,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a ~~first maximum~~ limiting value ~~and a second maximum limiting value~~ which is higher than ~~the first maximum limiting~~ said default value ~~are~~ is defined for the power consumption, and

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value. ~~between said first maximum limiting value and said second maximum limiting value~~.

17. (Currently Amended) The electronic device according to claim 16, further comprising

means for transmitting messages from the peripheral device and for receiving messages to the peripheral device, to set the maximum power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value ~~substantially between said first maximum limiting value and said second maximum limiting value~~.

18. (Previously Presented) The electronic device according to claim 16, wherein it is a portable electronic device.

19. (Previously Presented) The electronic device according to claim 18, further comprising means for performing mobile station functions.

20. (Currently Amended) A peripheral device comprising:

means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a ~~first maximum~~ limiting value ~~and a second maximum limiting value~~ which is higher than ~~the first maximum limiting~~ said default value, ~~are~~ is defined for power consumption, and

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value ~~between said first maximum limiting value and said second maximum limiting value~~.

21. (Previously Presented) The peripheral device according to claim 20, wherein at least one content is stored in the peripheral device for use in connection with the electronic device.

22. (Previously Presented) The peripheral device according to claim 20, further comprising

means for generating at least one clock signal and

means for controlling the power consumption of the peripheral device by frequency control of said at least one clock signal.

23. (Previously Presented) The peripheral device according to claim 20, further comprising

at least one bus and

means for controlling the power consumption of the peripheral device by controlling a bus width of said bus of the peripheral device.

24. (Previously Presented) The peripheral device according to the claim 20,

wherein the peripheral device is provided with two or more storage blocks, and

wherein the means for controlling the power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

25. (Currently Amended) The peripheral device according to the claim 20, wherein said ~~first maximum limiting~~ default value and at least one ~~said second maximum~~ limiting value are stored in the peripheral device.

26. (Previously Presented) The peripheral device according to the claim 20, wherein said peripheral device is a MultiMediaCard™ peripheral device.

27. (Currently Amended) An electronic device comprising:

a connector configured to connect a peripheral device;

a power supply configured to supply power to the peripheral device; and

a power gauge configured to determine power consumption,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a ~~first maximum~~ limiting value ~~and a second maximum limiting value~~ which is higher than ~~the first maximum limiting~~ said default value ~~are~~ is defined for the power consumption, and

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value. ~~between said first maximum limiting value and said second maximum limiting value~~.

28. (Currently Amended) The electronic device according to claim 27, further comprising

a transceiver configured to transmit messages from the peripheral device and for receiving messages to the peripheral device, to set the maximum power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value ~~substantially between said first maximum limiting value and said second maximum limiting value~~.

29. (Currently Amended) A peripheral device comprising:

a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a ~~first maximum~~ limiting value ~~and a second maximum limiting value~~ which is higher than ~~the first maximum limiting~~ said default value, ~~are~~ is defined for power consumption, and

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which in a range from said default value to said limiting value, said range including said default value and said limiting value ~~is between said first maximum limiting value and said second maximum limiting value~~.

30. (Currently Amended) The peripheral device according to the claim 29, wherein said ~~first maximum limiting~~ default value and at least one ~~said second maximum~~ limiting value are stored in the peripheral device.

31. (Previously Presented) The electronic device according to claim 27, wherein it is a portable electronic device.

32. (Currently Amended) The electronic device according to claim 27, further comprising a memory configured to store the ~~first maximum limiting~~ default value and the ~~second maximum~~ limiting value.

REMARKS

The independent claims are claims 1, 9, 16, 20, 27 and 29. All of claims 1-32 now stand rejected. The Office Action has withdrawn the anticipation rejection based upon *Amoni* and *McKeen*. However, all claims are again rejected as anticipated by *Robinson* (U.S. Patent No. 5,532,945).

All of the present amendments are fully supported by the specification as originally filed, and introduce no new matter. The present amendments of the independent claims are supported at least by claim 2 as originally filed; and by the paragraph beginning on page 7, line 20; and the paragraph beginning at page 9, line 5; and by the paragraph beginning at page 11, line 5.

A major difference between the present application and prior art is that, in the present solution, the power consumption is at a first stage that is low (default) and is raised (if possible). In contrast, according to prior solutions, the power consumption is at a first stage that is high (peak power) and is decreased if necessary.

The invention of the present application provides an improved method and system for determining the power consumption. By the method according to the invention, it is possible to avoid the use of an unnecessarily large regulator in an electronic device, which saves costs, and wherein the size of the electronic device can, in some cases, be reduced and, on the other hand, problems of heating caused by high power consumption can be avoided. Also the power consumption can be reduced, which is advantageous particularly in portable devices. By means of the invention, the peripheral device connection can also be provided with flexibility, because the power consumption of the peripheral device can be adjusted and set to a value suitable for each situation of use. Furthermore, the invention makes it possible that new peripheral devices to be developed will function in connection with electronic devices made earlier, and existing peripheral devices will function in connection with new electronic devices to be developed. None of these advantages can be achieved by the cited solution disclosed by *Robinson*, which includes a "power resource table" stored at the host, which table is updated and can be read by a card.

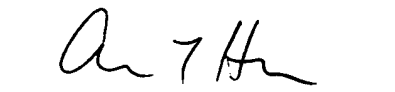
CONCLUSION

Thus, the Examiner is asked to kindly reconsider the Office Action in the light of the arguments presented herein, and to correspondingly issue a favorable Office Action at the next stage of the proceedings. The present amendments raise no new issues, and introduce no new matter.

Early allowance of all independent claims (and the pending claims depending therefrom) is earnestly solicited. Please not that the Applicant has partially followed the recommendation in the penultimate full sentence on page 2 of the non-final Office Action. Applicant would be grateful if the Examiner would please contact Applicant's attorney by telephone if the Examiner detects anything in the present response that might impede a speedy allowance.

Respectfully submitted,

Dated: Oct. 11, 2006



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PTO/SB/06 (12-04)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 10401338	Filing Date: 03/26/2003	☐ To be Mailed

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $25 =		OR	X $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $100 =			X $200 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+ $180			+$360	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT A	101606	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 31	Minus	** 32	=	X $25 =		OR	X $50=	
	Independent (37 CFR 1.16(h))	* 6	Minus	** 6	=	X $100 =		OR	X $200=	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $25 =		OR	X $50 =	
	Independent (37 CFR 1.16(h))	*	Minus	**	=	X $100 =		OR	X $200 =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
	CALCULATE					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
carol barnes

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/401,338	03/26/2003	Kimmo Mylly	915-005.48	4941

4955 7590 12/27/2006

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755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
BAE, JI H	
ART UNIT	**PAPER NUMBER**
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/401,338	MYLLY, KIMMO	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 16 October 2006 have been fully considered but they are not persuasive.

Applicant has amended the claims and provided supporting argumentation for those features of the applicant's invention that the applicant believes are novel over the prior art. Specifically, on page 9 of applicant's remarks, the applicant states:

"A major difference between the present application and prior art is that, in the present solution, the power consumption is at a first stage that is low (default) and is raised (if possible). In contrast, according to prior solutions, the power consumption is at a first stage that is high (peak power) and is decreased if necessary."

In response, the examiner respectfully disagrees and re-asserts the position that Robinson does in fact teach the features that the applicant believes are novel over the prior art. Referring to Fig. 6 of Robinson, step 130 of the method teaches reading the CIS of the removable device. According to Robinson's disclosure, reading the CIS involves obtaining the **default standby power levels** for the system [col. 11, lines 27-34, col. 9, lines 62-64]. In the next step [132], a request for **peak** power is made. When the request for peak power is made, the system issues a request_power function [col. 11, lines 35-37]. Robinson teaches that the request_power function first determines **existing** power allocations in the system, and then determines if there is enough power available to provide the requested amount. Thus, it is presupposed in Robinson's request_power method that there is already some power allocated to the system before the request for additional power is made. Robinson further teaches that if there is not enough power to provide the requested peak power, the request is repeated with a lower requested power until the available power is able to satisfy the requested power [col. 11,

lines 35-50]. Since in this case the power supplied is less than the peak power, the result is that the power consumption is set to a value that is between the initially supplied value and the requested peak power.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9, 10, 14-21, 25, and 27-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Robinson, U.S. Patent No. 5,532,945.

Regarding claim 1, Robinson teaches a method comprising [Fig. 6]:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device;

setting the power consumption of the peripheral device at a startup stage to a default value [see examiner's response to arguments]

reading from a memory [CIS, col. 11, lines 31-34], in order to determine a maximum of the power consumption, at least a limiting value which is higher than said default value [peak and standby values]; and

setting the maximum of the power consumption to a value which is in a range from said default value to said limiting value [step 136, reduced power].

Regarding claim 2, Robinson teaches that a default value, and that the power consumption settings are set to the default upon reset [col. 9, lines 57-64].

Regarding claim 3, Robinson teaches that the limiting value is used as a highest allowable value for the power consumption.

Regarding claim 4, Robinson teaches that messages are transferred between the peripheral device and the electronic device for setting the maximum power consumption value [col. 11, lines 35-50, request_power_function and success return codes].

Regarding claim 5, Robinson teaches at least one content is stored in the peripheral device, to be used in connection with the electronic device, wherein at the stage of storing the content, the power consumption set for the peripheral device is a value corresponding to said limiting value, and at the stage of using the content, the power consumption set for the peripheral device is a value corresponding to said default value [col. 1, ,line 65 to col. 2, line 7].

Regarding claims 9, 10, 14-21, 25, and 27-32 Robinson teaches the method of claims 1-5, and also the system and device to implement the claimed method. Robinson also teaches that the peripheral device is a portable electronic device [Fig. 1, removable flash card, fax/modem card], and that the peripheral device performs mobile station functions [fax/modem card, Fig. 1].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 11, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson in view of Yonezu et al., U.S. Patent No. 4,841,440[1].

Regarding claims 6, 11, and 22, Robinson teaches the method of claim 1, but does not teach that the power consumption is controlled by adjusting the frequency of a clock signal.

Yonezu teaches that power consumption may be reduced by inhibiting a control clock signal for a peripheral device [abstract].

It would have been obvious to one of ordinary skill in the art to modify Robinson using the teachings of Robinson. Both Robinson and Yonezu disclose methods of power control for peripheral devices. The addition of Yonezu's teaching would improve Robinson by providing a way to reduce power consumption.

Claims 7, 12, and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson in view of Gupta et al., U.S. Patent No. 5,996,083.

Regarding claims 7, 12, and 23, Robinson teaches the method of claim 1, but does not teach controlling power consumption by controlling a width of a bus.

Gupta teaches a technique wherein power consumption in a processor is reduced by changing the width of a bus [col. 9, lines 21-32].

It would have been obvious to one of ordinary skill in the art to modify Robinson by providing a capability to modify the bus width, as taught by Gupta. The teachings of Gupta would improve the system of Robinson by reducing the number of data lines driven on the bus, thus reducing the overall power consumption.

[1] Applicant-cited reference.

Claims 8, 13, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson in view of Holder, Jr., U.S. Patent No. 5,892,729.

Regarding claims 8, 13, and 24, Robinson teaches that the peripheral device comprises one or more storage blocks, but does not teach the controlling of the number of storage blocks processed.

Holder teaches a memory comprising multiple storage banks which may be selectively activated [col. 3, lines 21-32].

It would have been obvious to one of ordinary skill in the art to modify Robinson by providing selectable memory banks, as taught by Holder. The teachings of Holder would improve the system of Robinson by providing selectable memory banks so as to reduce power consumption.

Regarding claim 25, it would have been obvious to one of ordinary skill in the art to store the first and second maximum values in the peripheral device.

Regarding claim 26, it would have been obvious to one of ordinary skill in the art to apply the teachings of Robinson to a multimedia card peripheral device.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae
Patent Examiner
Art Unit 2115
ji.bae@uspto.gov
571-272-7181

CHUN CAO
PRIMARY EXAMINER

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10401338	MYLLY, KIMMO
	Examiner	Art Unit
	Bae, Ji H	2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2006	12/19/2006							
	1	✓	✓							
	2	✓	-							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
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	28	✓	✓							
	29	✓	✓							
	30	✓	✓							
	31	✓	✓							
	32	✓	✓							

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Bib Data Sheet

CONFIRMATION NO. 4941

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/401,338	03/26/2003 RULE	713	2115	915-005.48

APPLICANTS
Kimmo Mylly, Tampere, FINLAND;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS *********************
FINLAND 20020594 03/27/2002

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 05/23/2003

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☑ yes ☐ no	FINLAND	4	26	4
35 USC 119 (a-d) conditions met	☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature JB Initials				

ADDRESS
4955

TITLE
Method and a system for determining the power consumption in connection with an electronic device, and an electronic device

FILING FEE RECEIVED		
1642	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Kingston Exhibit 1004 - 340

RCE/Ziab

915-005.048

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of: **Kimmo MYLLY**

U.S. Serial No.: **10/401,338** Examiner: **Ji H. Bae**

Filed: **March 26, 2003** Group Art Unit: **2115**

For: **A METHOD AND SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE**

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION AND
REQUEST FOR CONTINUED EXAMINATION

Sir:

In response to the final Office Action of 27 December 2006, applicant respectfully requests reconsideration of the rejections of the claims of the above-referenced patent application in view of the following amendments and remarks. Please amend the application as follows.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Margery B. Hood

Margery B. Hood

Dated: March 27, 2007

03/30/2007 TBESHAH1 00000008 10401338

02 FC:1201 200.00 OP

IN THE CLAIMS:

1. (Currently Amended) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device;

setting the power consumption of the peripheral device at a startup stage to a default value;

reading from a memory, in order to determine a maximum of the power consumption, at least a limiting value which is higher than said default value; and

setting the maximum of the power consumption to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein information is transferred from the electronic device to the peripheral device for setting the maximum of the power consumption of the peripheral device.

2. CANCEL.

3. (Previously Presented) The method according to claim 1, wherein said limiting value is used as a highest allowable value for the power consumption.

4. (Currently Amended) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device;

setting the power consumption of the peripheral device at a startup stage to a default value;

reading from a memory, in order to determine a maximum of the power consumption, at least a limiting value which is higher than said default value; and

setting the maximum of the power consumption to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

~~The method according to claim 1,~~ wherein messages are transferred between the electronic device and the peripheral device for setting the maximum of the power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value.

5. (Previously Presented) The method according to claim 1, wherein at least one content is stored in the peripheral device, for use in connection with the electronic device, wherein at a stage of storing the content, the power consumption set for the peripheral device is a value corresponding to said limiting value, and at a stage of using the content, the power consumption set for the peripheral device is a value corresponding to said default value.

6. (Previously Presented) The method according to the claim 1, wherein at least one clock signal is generated in the peripheral device and wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

7. (Previously Presented) The method according to the claim 1, wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling a width of said bus.

8. (Previously Presented) The method according to the claim 1, wherein the peripheral device is provided with two or more storage blocks controlled by controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

9. (Currently Amended) A system comprising

a peripheral device;

an electronic device with means for connecting the peripheral device and means for supplying power to the peripheral device, and

means for determining power consumption,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a limiting value which is higher than said default value is stored for the power consumption, ~~and~~

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

10. CANCEL.

11. (Previously Presented) The system according to claim 9, wherein the peripheral device comprises means for generating at least one clock signal, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

12. (Previously Presented) The system according to claim 9,

wherein the peripheral device comprises at least one bus, and

wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting a bus width of the peripheral device.

13. (Previously Presented) The system according to the claim 9,

wherein the peripheral device is provided with two or more storage blocks, and

wherein the means for controlling the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

14. (Previously Presented) The system according to the claim 9, wherein the electronic device is a portable electronic device .

15. (Previously Presented) The system according to claim 14, further comprising means for performing mobile station functions.

16. (Currently Amended) An electronic device comprising:

means for connecting a peripheral device;

means for supplying power to the peripheral device; and

means for determining power consumption,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a limiting value which is higher than said default value is defined for the power consumption, ~~and~~

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the means for supplying the power is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

17. CANCEL.

18. (Previously Presented) The electronic device according to claim 16, wherein it is a portable electronic device.

19. (Previously Presented) The electronic device according to claim 18, further comprising means for performing mobile station functions.

20. (Currently Amended) A peripheral device comprising:

means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a limiting value which is higher than said default value, is defined for power consumption, ~~and~~

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device.

21. (Previously Presented) The peripheral device according to claim 20, wherein at least one content is stored in the peripheral device for use in connection with the electronic device.

22. (Previously Presented) The peripheral device according to claim 20, further comprising

means for generating at least one clock signal and

means for controlling the power consumption of the peripheral device by frequency control of said at least one clock signal.

23. (Previously Presented) The peripheral device according to claim 20, further comprising

at least one bus and

means for controlling the power consumption of the peripheral device by controlling a bus width of said bus of the peripheral device.

24. (Previously Presented) The peripheral device according to the claim 20,

wherein the peripheral device is provided with two or more storage blocks, and

wherein the means for controlling the power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

25. (Previously Presented) The peripheral device according to the claim 20, wherein said default value and at least one limiting value are stored in the peripheral device.

26. (Previously Presented) The peripheral device according to the claim 20, wherein said peripheral device is a MultiMediaCard™ peripheral device.

27. (Currently Amended) An electronic device comprising:

a connector configured to connect a peripheral device;

a power supply configured to supply power to the peripheral device; and

a power gauge configured to determine power consumption,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a limiting value which is higher than said default value is defined for the power consumption, ~~and~~

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

28. CANCEL.

29. (Currently Amended) A peripheral device comprising:

a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to a default value,

wherein at least a limiting value which is higher than said default value, is defined for power consumption, ~~and~~

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device.

30. (Previously Presented) The peripheral device according to the claim 29, wherein said default value and at least one limiting value are stored in the peripheral device.

31. (Previously Presented) The electronic device according to claim 27, wherein it is a portable electronic device.

32. (Previously Presented) The electronic device according to claim 27, further comprising a memory configured to store the default value and the limiting value.

33. (New) The method according to claim 4, wherein said limiting value is used as a highest allowable value for the power consumption.

REMARKS

The independent claims are claims 1, 9, 16, 20, 27 and 29. All of these independent claims now stand rejected as anticipated by *Robinson* (U.S. Patent No. 5,532,945). Claim 4 is now placed in independent form, because Applicant respectfully submits claim 4 should not have been rejected.

Claim 4 is not Suggested by the *Robinson* Reference

The Office Action stated (at page 4, second paragraph): "Robinson teaches that messages are transferred between the peripheral device and the electronic device for setting the maximum power consumption value [col. 11, lines 35-50, request_power_function and success return codes]." However, Applicant respectfully submits that those messages described at col. 11, lines 35-50 of *Robinson* do not involve any peripheral device. The *Robinson* reference states (at col. 11 lines 35-40) the following:

> "[T]he card services client device driver requests peak power from the card services **64** using the request_power function.... [T]he card services client device driver determines whether a success code was returned from the card services **64** for the request_power function."

The messages are thus transferred between the card services **64** and the card services client device driver such as the card services clients **60** and **61** or the logical device driver **56** (see col. 11, lines 20-23). ***None*** of these elements (**60**, **61**, and **56**) is a peripheral device, as can be seen in Figure 3 of the *Robinson* reference.

Figure 3 of *Robinson* shows that the card services client device drivers **60**, **61**, and **56** are not located in the peripheral devices **30** or **32** (also see also Figure 2 which shows components in the peripheral device **30**). Therefore, the messages of *Robinsons* are ***not*** transferred between any peripheral device and the electronic device.

The card services **64** is clearly indicated in Figure 3 of *Robinson*. It is also explained in *Robinson* (col. 11 lines 20-23) that "Each card service client device driver such as the card service clients **60** and **61** and the logical device driver **56**..." All of this is shown in Figure 3 of *Robinson*, and therefore it is evident that *Robinson* does not teach

or suggest that messages are transferred between the peripheral device and the electronic device for setting the maximum power consumption value, as claimed by claim 4.

Amendment of the Independent Claims

Dependent claims 10, 17, and 28 are now cancelled. Independent claims 1, 9, 16, 20, 27, and 29 are now amended in order to include limitations similar to those in claim 4. Support for these limitations can be found at page 9 of the application as originally filed. These amendments introduce no new matter. New claim 33 is supported by present claim 3.

CONCLUSION

Thus, the Examiner is asked to kindly reconsider the Office Action in the light of the arguments presented herein, and to correspondingly issue a favorable Office Action at the next stage of the proceedings.

Early allowance of all independent claims (and the pending claims depending therefrom) is earnestly solicited. Applicant would be grateful if the Examiner would please contact Applicant's attorney by telephone if the Examiner detects anything in the present response that might impede a speedy allowance.

Respectfully submitted,

Dated: 26 March 2007

Andrew T. Hyman
Attorney for Applicant
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Practitioner's Docket No. 915-005.048 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: K. Mylly
Application No.: 10 / 401,338 Group No.: 2115
Filed: March 26, 2003 Examiner: J. Bae
For: Method and System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device

Commissioner for Patents
Washington, D.C. 20231

REQUEST FOR CONTINUED EXAMINATION (RCE)
(37 C.F.R. § 1.114)

1. Applicant hereby requests continued examination, in accordance with 37 C.F.R. § 1.114, for the above identified application.

NOTE: 37 C.F.R. § 1.114 Request for continued examination:

"(a) If prosecution in an application is closed, an applicant may request continued examination of the application by filing a submission and the fee set forth in § 1.17(e) prior to the earliest of:

(1) Payment of the issue fee, unless a petition under § 1.313 is granted;

(2) Abandonment of the application; or

(3) The filing of a notice of appeal to the U.S. Court of Appeals for the Federal Circuit under 35 U.S.C. 141, or the commencement of a civil action under 35 U.S.C. 145 or 146, unless the appeal or civil action is terminated.

(b) Prosecution in an application is closed as used in this section means that the application is under appeal, or that the last Office action is a final action (§ 1.113), a notice of allowance (§ 1.311), or an action that otherwise closes prosecution in the application.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*
*(When using Express Mail, the Express Mail label number is **mandatory**; Express Mail certification is optional.)*

I hereby certify that, on the date shown below, this correspondence is being:

MAILING

☒ deposited with the United States Postal Service in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231

37 C.F.R. § 1.8(a)

☒ with sufficient postage as first class mail.

37 C.F.R. § 1.10 *

☐ as "Express Mail Post Office to Addressee"
Mailing Label No. _____ **(mandatory)**

TRANSMISSION

☐ facsimile transmitted to the Patent and Trademark Office, (703) _____-_____

Date: 3/27/07

Margery B. Hood
Signature

03/30/2007 TBESHAH1 00000008 10401338
01 FC1801 790.00 OP

Margery B. Hood
(type or print name of person certifying)

** Only the date of filing (§ 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under § 1.8 continues to be taken into account in determining timeliness. See § 1.703(f). Consider "Express Mail Post Office to Addressee" (§ 1.10) or facsimile transmission (§ 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

Kingston Exhibit 1004 - 351

(c) A submission as used in this section includes, but is not limited to, an information disclosure statement, an amendment to the written description, claims, or drawings, new arguments, or new evidence in support of patentability. If reply to an Office action under 35 U.S.C. 132 is outstanding, the submission must meet the reply requirements of § 1.111.

(d) If an applicant timely files a submission and fee set forth in § 1.17(e), the Office will withdraw the finality of any Office action and the submission will be entered and considered. If an applicant files a request for continued examination under this section after appeal, but prior to a decision on the appeal, it will be treated as a request to withdraw the appeal and to reopen prosecution of the application before the examiner. An appeal brief under § 1.192 or a reply brief under § 1.193(b), or related papers, will not be considered a submission under this section."

NOTE: *An applicant may file a submission under 37 CFR 1.114 containing only an information disclosure statement (37 CFR 1.97 and 1.98) in an application subject to a notice of allowance under 35 U.S.C. § 151. An appeal brief or a reply brief (or related papers) will not be considered a submission under 37 CFR 1.114. See 37 CFR 1.114(d). The submission, however, may consist of the arguments in a previously filed appeal brief or reply brief, or may simply consist of a statement that incorporates by reference the arguments in a previously filed appeal brief or reply brief. In addition, a previously filed amendment after final may satisfy this submission requirement. American Inventor's Protection Act of 1999, Question & Answer A5.*

NOTE: *Even though an RCE is improper (e.g., because it was filed before the prosecution is closed), an amendment submitted with the RCE will still be entered and considered by the examiner since it was timely filed and responsive to the non-final Office action in compliance with 37 CFR 1.111. American Inventor's Protection Act of 1999, Question & Answer A4.*

WARNING: *35 U.S.C. 132(b) and § 1.114 provide for the continued examination of an application and* ***not*** *examination of a continuing application). Accordingly, the Office will not permit an applicant to obtain continued examination on the basis of claims that are independent and distinct from the claims previously claimed and examined. Notice of March 10, 2000, 65 Fed Reg 14865, at 14868.*

WARNING: *The provisions of 37 CFR 1.114 also do not apply (1) to a provisional application; (2) an application for a utility or plant patent filed under 35 U.S.C. 111(a) before June 8, 1995; (3) an international application filed under 35 U.S.C. 363 before June 8, 1995; (4) a patent under reexamination or (5) an application for a design patent. 37 CFR § 1.114(e).*

WARNING: *The PTO has pointed out why § 1.97(b) does not provide that an information disclosure statement will be considered if it is filed within three months after the date of a request for continued examination under § 1.114. The PTO explained that since an RCE filing is a reply under 35 U.S.C. 132, the applicant may be entitled to patent term adjustment if the Office does not act on an application containing a request for continued examination under § 1.114 within four months. See 35 U.S.C. 154(b)(1)(A)(ii). Thus, the Office cannot delay action on RCE applications for three months to determine whether an information disclosure statement will be filed. The Office, however, is adopting provisions (§ 1.103(c)) for a limited suspension of action after the filing of a request for continued examination under § 1.114, for the applicant to obtain additional time (prior to the issuance of the next Office action) to provide an information disclosure statement (or amendments, or an affidavit or declaration) after the filing of the RCE. See, Notice of August 16, 2000, "Request for Continued Examination Practice and Changes to Provisional Application Practice; Final Rule", 65Fed. Reg., pages 50091–50105, at page 50100 (comment 11); OG: September 5, 2000, pages 13–24*

WARNING: *One of the time periods excluded from patent term adjustment is the time consumed by a continued examination request under 35 U.S.C. 132(b) (§ 1.114(b) (1)).*

WARNING: *The Office will not suspend action in an application when a reply by the applicant is outstanding. 35 U.S.C. 133 requires an applicant to "prosecute the application" within six months of an Office action (or a shorter period as set in the Office action) to avoid abandonment of the application. If an applicant files a request for continued examination but does not also provide any submission (in reply to the prior Office action) within the period for reply to the prior Office action, the application is abandoned by operation of law (35 U.S.C. 133).*

The Office will treat a request for continued examination under § 1.114 containing a bona fide submission that is not fully responsive to the prior Office action under the practice set forth in § 1.135(c). In addition, under the limited suspension of action provisions of § 1.103(c), an applicant must still file a request for continued examination practice in compliance with § 1.114, but may obtain additional time (prior to the issuance of the next Office action) to provide an information disclosure statement, amendments, or an affidavit or declaration after the filing of the request for continued examination.

See, Notice of August 16, 2000, "Request for Continued Examination Practice and Changes to Provisional Application Practice; Final Rule", 65Fed. Reg., pages 50091-50105, at page 50102 (comment 20); OG: September 5, 2000, pages 13-24] Page 50102

WARNING: *Section 1.97(b) does not provide that an information disclosure statement will be considered if it is filed within three months after the date of a request for continued examination under § 1.114.*

NOTE: There is no limit to the number of times the fee for continued examination may be submitted. Notice of March 10, 2000, 65 Fed Reg 14865, at 14868.

NOTE: Unlike a continuation application, a continued examination request **can** *utilize the mailing procedure of 37 CFR 1.8. See 37 CFR § 1.8(a)(2)(i)(A).*

Continued Prosecution Request Fee $ _____

TIME REQUEST IS BEING MADE

2. This request is being submitted *(check appropriate item(s) below):*

i ☒ Prior to abandonment of the application

ii. ☐ Payment of the issue fee

- ☐ Prior to payment of issue fee
- ☐ Issue fee has been paid but a petition under § 1.313 has been granted

iii. ☐ Prior to a decision on appeal to the Board of Patent Appeals & Interferences

- ☐ A notice is being separately sent to the Board of Patent Appeals & Interferences that this Request for Continued Examination is being filed.

NOTE: If such a notice is not sent to the Board then may refuse to vacate a decision rendered after the filing of the RCE but before recognition by the Office of the RCE request under § 1.114.

iv. ☐ Appeal to the U.S. Court of Appeals of the Federal Circuit under 35 U.S.C. 145 or ☐ Commencement of a civil action under 35 U.S.C. 146

- ☐ Prior to the filing of such appeal or commencement of civil action
- ☐ Such appeal or commencement of civil action has been terminated

ENCLOSURES

3. Enclosed herewith is/are:

WARNING: *If reply to a final or non-final Office action under 35 U.S.C. 132 is outstanding, the submission must meet the reply requirements of § 1.111. 37 C.F.R. § 1.114(b).*

☐ An information disclosure (37 C.F.R. § 1.98)

- ☐ Form PTO-1449 (PTO/SB/08A and 08B)

☒ An amendment

☒ New arguments

☐ New evidence in support of patentability

☐ Other:

Continued Prosecution Request Fee $ _____

FEE FOR REQUEST (37 C.F.R. § 1.17(e)).

4. This application is on behalf of:

☐ Small entity (and status is still as small entity) $375.00

☒ Other than a small entity $790.00

FEE FOR CLAIMS

NOTE: "The fee for continued examination under § 1.114 (§ 1.17(e)) does not include additional claims fee (cf. 1.53 (d)(3)(ii))." See Notice of March 10, 2000, 65 Fed Reg 14865, at 14868.

37 CFR 1.53(d)(3): "The filing fee for a continued prosecution application filed under this paragraph is:

(i) The basic filing fee as set forth in § 1.16; and

Any additional § 1.16 fee due based on the number of claims remaining in the application after entry of any amendment accompanying the request for an application under this paragraph and entry of any amendments under § 1.116 unentered in the prior application which applicant has requested to be entered in the continued prosecution application."

5. The fee for claims (37 C.F.R. § 1.16(b)-(d)) has been calculated as shown below:

(Col. 1)	(Col. 2)	(Col. 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDIT. FEE	*OR*	RATE	ADDIT. FEE
TOTAL * 29	MINUS ** 32	=	x$9=	$		x$18=	$ —
INDEP. * 7	MINUS *** 6	=	x$42=	$		~~x200~~=	$ 200
☐FIRST PRESENTATION OF MULTIPLE DEP. CLAIM			+$140=	$		+$280=	$
			TOTAL ADDIT. FEE	$	*OR*	TOTAL ADDIT. FEE	$ 200.00

* If the entry in Col. 1 is less than entry in Col. 2, write "0" in Col. 3.

** If the "Highest No. Previously Paid for" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest No. Previously Paid For" (Total or Indep.) is the highest number found in the appropriate box in Col. 1 of a prior amendment or the number of claims originally filed.

WARNING: *See 37 C.F.R. § 1.116.*

(complete (a) or (b), as applicable)

(a) ☐ No additional fee is required.

OR

(b) ☒ Total additional fee required is $ 200.00.

EXTENSION OF TIME

(If an extension of time is appropriate complete (a) or (b), as applicable)

6. The proceedings herein are for a patent application, and the provisions of 37 C.F.R. § 1.136(a) apply.

NOTE: 37 C.F.R. § 1.704(b) ". . .an applicant shall be deemed to have failed to engage in reasonable efforts to conclude processing or examination of an application for the cumulative total of any periods of time in excess of three months that are taken to reply to any notice or action by the Office making any rejection, objection, argument, or other request, measuring such three-month period from the date the notice or action was mailed or given to the applicant, in which case the period of adjustment set forth in § 1.703 shall be reduced by the number of days, if any, beginning on the day after the date that is three months after the date of mailing or transmission of the Office communication notifying the applicant of the rejection, objection, argument, or other request and ending on the date the reply was filed. The period, or shortened statutory period, for reply that is set in the Office action or notice has no effect on the three-month period set forth in this paragraph."

(a) ☐ Applicant petitions for an extension of time, the fees for which are set out in 37 C.F.R. § 1.17(a)(1)-(4), for the total number of months checked below:

Extension for (months)	Fee for other than small entity	Fee for small entity
☐ one month	$ 110.00	$ 55.00
☐ two months	$ 410.00	$ 205.00
☐ three months	$ 930.00	$ 465.00
☐ four months	$ 1,450.00	$ 725.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

OR

(b) ☒ Applicant believes that no extension of time is required. However, this is a conditional petition and authorization to pay the necessary fees to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

TOTAL FEE(S) DUE

WARNING: *The fee for continued examination under § 1.114 may not be deferred. 37 C.F.R. § 1.53(f).*

7. The total fee(s) due is/are:

Continued Prosecution Fee (§ 1.17(e))	$ 790.00
Fee(s) for additional claims (if any) (§ 1.16(b)-(d))	$ 200.00
Extension of time fee (if any) (§ 1.17(a)(1)-(4))	$ —
Total Fee(s) Due	$ 990.00

PAYMENT OF FEE(S) DUE

8. Please pay the fee(s) for this continued examination application as follows:

☒ Check is attached for the sum of $ 990.00

☐ Charge Account _____ the sum of $ _____

☐ Charge Credit Card the sum of $ _____

(Credit Card Payment Form (PTO-2038) attached)

Please charge any required additional fee(s) for § 1.17(e), § 1.16(b)-(d) and/or § 1.17(a)(1)-(4) to

☒ Account 23-0442

☐ Credit Card (Credit Card Payment Form (PTO-2038) attached).

INVENTORSHIP

NOTE: Any change of inventors must be via the procedure set forth in 37 CFR § 1.48. See Notice of March 10, 2000, 65 Fed Reg 14865, at 14868.

9. This application as amended names as inventors:

☐ the same inventors as previously designated for the claims.

☐ fewer than the inventors previously designated ans a statement accompanies this request for the deletion of the name or names of the person or persons who are not inventors of the invention now being claimed.

☐ a person not named previously as an inventor and a petition under 37 C.F.R. § 1.48 is/has separately: ☐ being filed ☐ been filed

DEFERRAL OF EXAMINATION

10. ☐ A request for deferral of examination accompanies this request for continued examination.

Andrew T. Hyman

SIGNATURE OF PRACTITIONER

Reg. No.: 45,858

Andrew T. Hyman

(type or print name of practitioner)

Tel. No.: (203) 261-1234

WARE, FRESSOLA, VAN DER SLUYS

P.O. Address & ADOLPHSON LLP

Customer No.: 004955

755 Main Street, PO Box 224

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PTO/SB/06 (12-04)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 10401338	Filing Date: 03/26/2003	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		X $25 =		OR	X $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		X $100 =			X $200 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+ $180			+$360	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	101606	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	* 31	Minus	** 32	=	X $25 =		OR	X $50=	
	Independent (37 CFR 1.16(h))	* 6	Minus	** 6	=	X $100 =		OR	X $200=	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

3-29-07

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	* 29	Minus	** 32	= 0	X $25 =		OR	X $50 =	0
	Independent (37 CFR 1.16(h))	* 7	Minus	** 6	= 1	X $100 =		OR	X $200 =	200
	☐ Application Size Fee (37 CFR 1.16(s))									0
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		0
	CALCULATE					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	200

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
carol barnes

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S50	478	multimediacard	US-PGPUB; USPAT; EPO	OR	OFF	2007/05/31 15:43
S51	67	("4782355" | "4884287" | "4901217" | "5121500" | "5179710" | "5313642" | "5408669" | "5483656" | "5493684" | "5514859" | "5560022" | "5652895" | "5742514").PN. OR ("5884086"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/04 16:32
S53	475	multimediacard	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/04 17:18
S52	36	S51 and usb	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/04 17:18
S55	0	S53 with (request$3 near3 power)	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/04 17:19
S54	1	S53 and (peripheral device) near3 request$3 near3 power	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/04 17:19
S57	19	S53 and (peripheral device card) near5 (suppl$4 provid$3) near5 (more additional)	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/04 17:21
S56	28	S53 and (peripheral device card) near3 (suppl$4 provid$3) near3 power	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/04 17:21
S58	0	S53 and (peripheral device card) near5 (suppl$4 provid$3) near5 (more additional) near5 power	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/04 17:23
S59	10	S53 and 713/3$2.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/04 17:25
S60	1	S53 and (peripheral device card) with (power near3 (maximum limit))	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/05 10:33
S61	4	multimediacard same (power near3 (control$4 manag$5 request$3))	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/05 10:42
S62	6	multimediacard same (power near3 (set$4 determin$3 level))	US-PGPUB; USPAT; USOCR	OR	OFF	2007/06/05 10:43
L3	16	2.clm.	US-PGPUB	OR	OFF	2007/06/08 11:34
L2	81	"peripheral device" with "power consumption"	US-PGPUB	OR	OFF	2007/06/08 11:34

EAST Search History

L1	2325	713/3$2.ccls.	US-PGPUB	OR	OFF	2007/06/08 11:34
L6	1	5.clm. and 3	US-PGPUB	OR	OFF	2007/06/08 11:35
L5	10670	(first second) near2 maximum	US-PGPUB	OR	OFF	2007/06/08 11:35
L4	1	3 and ("default value" "limiting value").clm.	US-PGPUB	OR	OFF	2007/06/08 11:35
L8	7	7.clm.	US-PGPUB	OR	OFF	2007/06/08 11:36
L7	21	(memory near3 stor$3) with value$1 near3 "power consumption"	US-PGPUB	OR	OFF	2007/06/08 11:36

UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

4955 7590 06/13/2007

WARE FRESSOLA VAN DER SLUYS &
ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
BAE, JI H	
ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/13/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/401,338	03/26/2003	Kimmo Mylly	915-005.48	4941

TITLE OF INVENTION: METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	09/13/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 06/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

4955 7590 06/13/2007

WARE FRESSOLA VAN DER SLUYS &
ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/401,338	03/26/2003	Kimmo Mylly	915-005.48	4941

TITLE OF INVENTION: METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	09/13/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
BAE, JI H	2115	713-300000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/401,338	03/26/2003	Kimmo Mylly	915-005.48	4941

4955 7590 06/13/2007

WARE FRESSOLA VAN DER SLUYS &
ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
BAE, JI H	
ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/13/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 472 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 472 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/401,338	MYLLY, KIMMO	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendments filed on 3-29-2007*.

2. ☒ The allowed claim(s) is/are *1,3-9,11-16,18-27 and 29-33*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20070604* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andrew Hyman on 7 June 2007.

The application has been amended as follows:

Claim 1, amended to read:

A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device, **wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;**

setting the power consumption of the peripheral device at a startup state to **said** default value;

reading from the memory at least **said** limiting value which is higher than said default value; and

setting the maximum of the power consumption to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein information is transferred from the electronic device to the peripheral device for setting the maximum of the power consumption of the peripheral device.

Claim 4, amended to read:

A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device, **wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;**

setting the power consumption of the peripheral device at a startup stage to **said** default value;

reading from the memory at least **said** limiting value which is higher than said default value; and

setting the maximum of the power consumption to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein messages are transferred between the electronic device and the peripheral device for setting the maximum of the power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value.

Claim 9, amended to read:

A system comprising

a peripheral device, **wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;**

an electronic device with means for connecting the peripheral device and means for supplying power to the peripheral device, and

means for determining power consumption,

wherein the power consumption of the peripheral device is set at a startup stage to **said** default value,

wherein at least **said** limiting value which is higher than said default value is stored for the power consumption,

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

Claim 16, amended to read:

An electronic device comprising:

means for connecting a peripheral device, **wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;**

means for supplying power to the peripheral device; and

means for determining power consumption,

wherein the power consumption of the peripheral device is set at a startup stage to **said** default value,

wherein at least **said** limiting value which is higher than said default value is defined for the power consumption,

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the means for supplying the power is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

Claim 20, amended to read:

A peripheral device comprising:

a memory storing a default value and a limiting value for power consumption;

means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to **said** default value,

wherein at least **said** limiting value which is higher than said default value is defined for power consumption,

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device.

Claim 27, amended to read:

An electronic device comprising:

a connector configured to connect to a peripheral device, **wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;**

a power supply configured to supply power to the peripheral device; and

a power gauge configured to determine power consumption,

wherein the power consumption of the peripheral device is set at a startup stage to **said** default value,

wherein at least **said** limiting value which is higher than said default value is defined for the power consumption,

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

Claim 29, amended to read:

A peripheral device comprising:

a memory storing a default value and a limiting value for power consumption;

a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to **said** default value,

wherein at least **said** limiting value which is higher than said default value is defined for power consumption,

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae
Patent Examiner
Art Unit 2115
ji.bae@uspto.gov
571-272-7181

CHUN CAO
PRIMARY EXAMINER

Interview Summary	Application No.	Applicant(s)	
	10/401,338	MYLLY, KIMMO	
	Examiner	Art Unit	
	Ji H. Bae	2115	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Ji H. Bae*. (3)_____.

(2) *Andrew Hyman*. (4)_____.

Date of Interview: *07 June 2007*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1,4,9,16,20,27 and 29*.

Identification of prior art discussed: *U.S. Patent Nos. 5,532,945 (Robinson) and 5,884,086 (Amoni)*.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *The examiner proposed amending the independent claims to recite a peripheral device comprising a memory, wherein the memory stores a default value and a limiting value for the power consumption. Although applicant's most recent amendment defined over the Robinson reference, the additional amendments were necessary to further define over the Amoni reference. The applicant agreed to all amendments*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

_____
Examiner's signature, if required

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Bib Data Sheet

CONFIRMATION NO. 4941

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/401,338	03/26/2003 RULE	713	2115	915-005.48

APPLICANTS
Kimmo Mylly, Tampere, FINLAND;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS *********************
FINLAND 20020594 03/27/2002

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 05/23/2003

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☑ yes ☐ no	FINLAND	4	26	4
35 USC 119 (a-d) conditions met: ☑ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged: Examiner's Signature JB Initials				

ADDRESS
4955

TITLE
Method and a system for determining the power consumption in connection with an electronic device, and an electronic device

FILING FEE RECEIVED		
1842	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Kingston Exhibit 1004 - 372

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10401338	MYLLY, KIMMO
	Examiner	Art Unit
	Bae, Ji H	2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2006	12/19/2006	06/08/2007						
1	1	✓	✓	=						
	2	✓	-	-						
2	3	✓	✓	=						
8	4	✓	✓	=						
3	5	✓	✓	=						
4	6	✓	✓	=						
5	7	✓	✓	=						
6	8	✓	✓	=						
9	9	✓	✓	=						
	10	✓	✓	-						
10	11	✓	✓	=						
11	12	✓	✓	=						
12	13	✓	✓	=						
13	14	✓	✓	=						
14	15	✓	✓	=						
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24	26	✓	✓	=						
25	27	✓	✓	=						
	28	✓	✓	-						
28	29	✓	✓	=						
29	30	✓	✓	=						
26	31	✓	✓	=						
27	32	✓	✓	=						
7	33			=						

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
10401338	MYLLY, KIMMO
Examiner	**Art Unit**
Bae, Ji H	2115

ORIGINAL	
CLASS	SUBCLASS
713	300

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
713	320	322			

INTERNATIONAL CLASSIFICATION					
CLAIMED					NON-CLAIMED
G	0	6	F	1 / 00 (2006.0)	
G	0	6	F	1 / 26 (2006.0)	
G	0	6	F	1 / 32 (2006.01.01)	

Bae, Ji H (Assistant Examiner)	6/7/2007 (Date)	CHUN CAO PRIMARY EXAMINER	Total Claims Allowed: 29
(Legal Instruments Examiner)	(Date)	(Primary Examiner) 6/8/07 (Date)	O.G. Print Claim(s): 1 / O.G. Print Figure: 1

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10401338	MYLLY, KIMMO
	Examiner	Art Unit
	Bae, Ji H	2115

SEARCHED

Class	Subclass	Date	Examiner
713	300	6/7/2007	/jb/
713	320	6/7/2007	/jb/
713	322	6/7/2007	/jb/

SEARCH NOTES

Search Notes	Date	Examiner
EAST text search (see attached search history)	6/7/2007	/jb/
PGPUB text search for interferences	6/7/2007	/jb/

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
713	300	6/7/2007	/jb/
713	320	6/7/2007	/jb/
713	322	6/7/2007	/jb/

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10401338	MYLLY, KIMMO
	Examiner	Art Unit
	Bae, Ji H	2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2006	12/19/2006	06/08/2007						
1	1	✓	✓	=						
	2	✓	-	-						
2	3	✓	✓	=						
7	4	✓	✓	=						
3	5	✓	✓	=						
4	6	✓	✓	=						
5	7	✓	✓	=						
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12	13	✓	✓	=						
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15	16	✓	✓	=						
	17	✓	✓	-						
16	18	✓	✓	=						
17	19	✓	✓	=						
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25	27	✓	✓	=						
	28	✓	✓	-						
28	29	✓	✓	=						
29	30	✓	✓	=						
26	31	✓	✓	=						
27	32	✓	✓	=						
8	33			=						

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
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P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

4955 7590 06/13/2007

WARE FRESSOLA VAN DER SLUYS &
ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Marilyn O'Connell	(Depositor's name)
Marilyn O'Connell	(Signature)
August 16, 2007	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/401,338	03/26/2003	Kimmo Mylly	915-005.48	4941

TITLE OF INVENTION: METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	09/13/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
BAE, JI H	2115	713-300000

08/21/2007 HNGUYEN2 00000013 10401338
01 FC:1501 1400.00 OP
02 FC:1504 300.00 OP

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Nokia Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Espoo, Finland

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 23-0442 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Andrew T. Hyman Date 15 Aug. 2007

Typed or printed name Andrew T. Hyman Registration No. 45,858

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/401,338	10/02/2007	7278033	915-005.48	4941

4955 7590 09/12/2007

WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 472 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Kimmo Mylly, Tampere, FINLAND;

PTO/AIA/82 (07-13)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 29150

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒ The address associated with Customer Number: 29150

OR

☐	Firm or Individual Name		
	Address		
	City	State	Zip
	Country		
	Telephone	Email	

Assignee Name and Address: Memory Technologies LLC
6787 W. Tropicana Avenue, Suite 238
Las Vegas, NV 89103

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Robert Saltzer	Date	6/26/13
Name	Robert Saltzer	Telephone	
Title	Authorized Representative		

Atty Docket No: **NKM-002-US1 / M089 - 0002US**

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Kimmo J. Mylly

Application No./Patent No.: 10/401,338 Filed/Issue Date: 3/26/2003

Titled: METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, ELECTRONIC DEVICE

Memory Technologies LLC, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Inventor To: Nokia Corporation

   The document was recorded in the United States Patent and Trademark Office at

   Reel 01392, Frame /0450, or for which a copy thereof is attached.

2. From: Nokia Corporation To: Nokia Inc.

   The document was recorded in the United States Patent and Trademark Office at

   Reel 030189, Frame 0381, or for which a copy thereof is attached.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

3. From: Nokia Inc. To: Memory Technologies LLC

The document was recorded in the United States Patent and Trademark Office at

Reel 030190, Frame 0043, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Lance D. Reich/	2013-06-26
Signature	Date
Lance D. Reich	42097
Printed or Typed Name	Title or Registration Number

Electronic Acknowledgement Receipt

EFS ID:	16177175
Application Number:	10401338
International Application Number:	
Confirmation Number:	4941
Title of Invention:	METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE
First Named Inventor/Applicant Name:	Kimmo Mylly
Customer Number:	4955
Filer:	Daniel Leo Hayes/Vanessa Lyman
Filer Authorized By:	Daniel Leo Hayes
Attorney Docket Number:	915-005.048
Receipt Date:	27-JUN-2013
Filing Date:	26-MAR-2003
Time Stamp:	16:52:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		YK1451.PDF	351044 4eb53a2dd759ed32ee520aa342f80b0d646499c5	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73.	2	3
Warnings:			
Information:			
	Total Files Size (in bytes):	351044	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/401,338	03/26/2003	Kimmo Mylly	NKM-002-US1/M089-0002US

CONFIRMATION NO. 4941

29150
LEE & HAYES, PLLC
601 W. RIVERSIDE AVENUE
SUITE 1400
SPOKANE, WA 99201

POA ACCEPTANCE LETTER

OC000000062786619

Date Mailed: 07/25/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/27/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/sharris/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/401,338	03/26/2003	Kimmo Mylly	915-005.048

CONFIRMATION NO. 4941

POWER OF ATTORNEY NOTICE

4955
WARE, FRESSOLA, MAGUIRE & BARBER LLP
BRADFORD GREEN, BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

OC000000062786454

Date Mailed: 07/25/2013

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/27/2013.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/sharris/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101