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Apostol, Jr. et al.

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(54) **INTEGRATED CIRCUIT WITH UNIFIED MEMORY SYSTEM AND DUAL BUS ARCHITECTURE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Related U.S. Application Data

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(51) **Int. Cl.**[7] **G06F 13/00**

(52) **U.S. Cl.** **710/108**; 710/100; 710/240; 711/147; 711/149; 711/150

(58) **Field of Search** 711/149, 147, 711/150; 710/240, 100, 108

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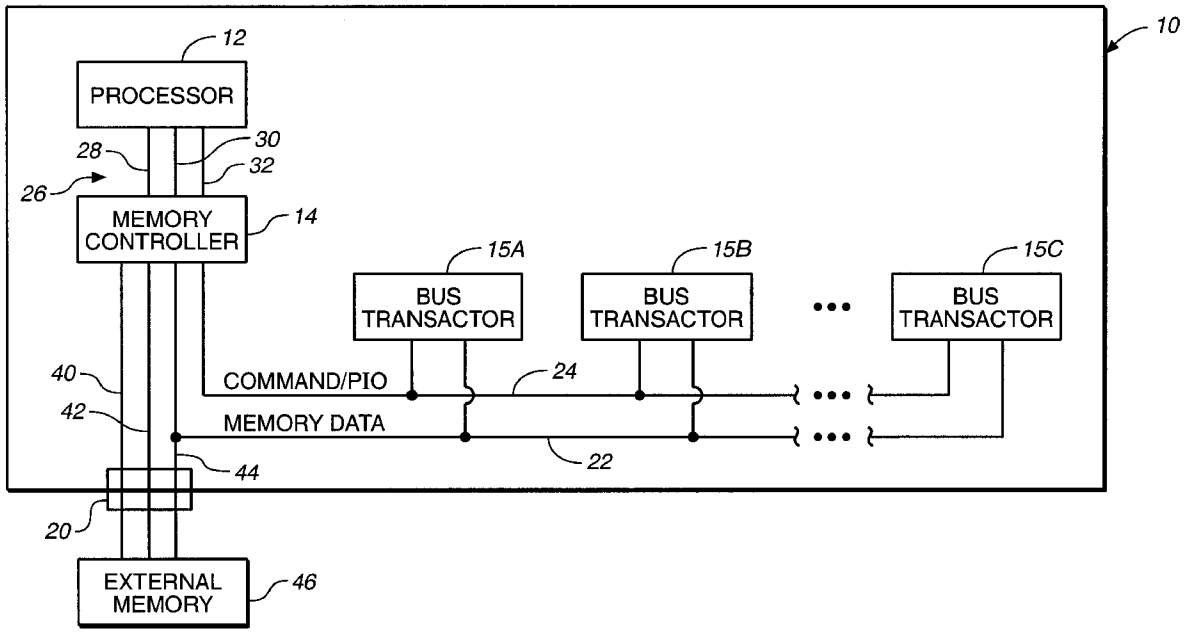
Primary Examiner—Rupal D. Dharia

(57) **ABSTRACT**

A unified memory system includes a processor, a memory controller, a plurality of bus transactor circuits and a shared memory port. A processor bus is coupled between the processor and the memory controller. A first multiple-bit, bidirectional system bus is coupled between the shared memory port, the memory controller and the plurality of bus transactor circuits. A second multiple-bit, bidirectional system bus is coupled between the memory controller and the plurality of bus transactor circuits.

19 Claims, 36 Drawing Sheets



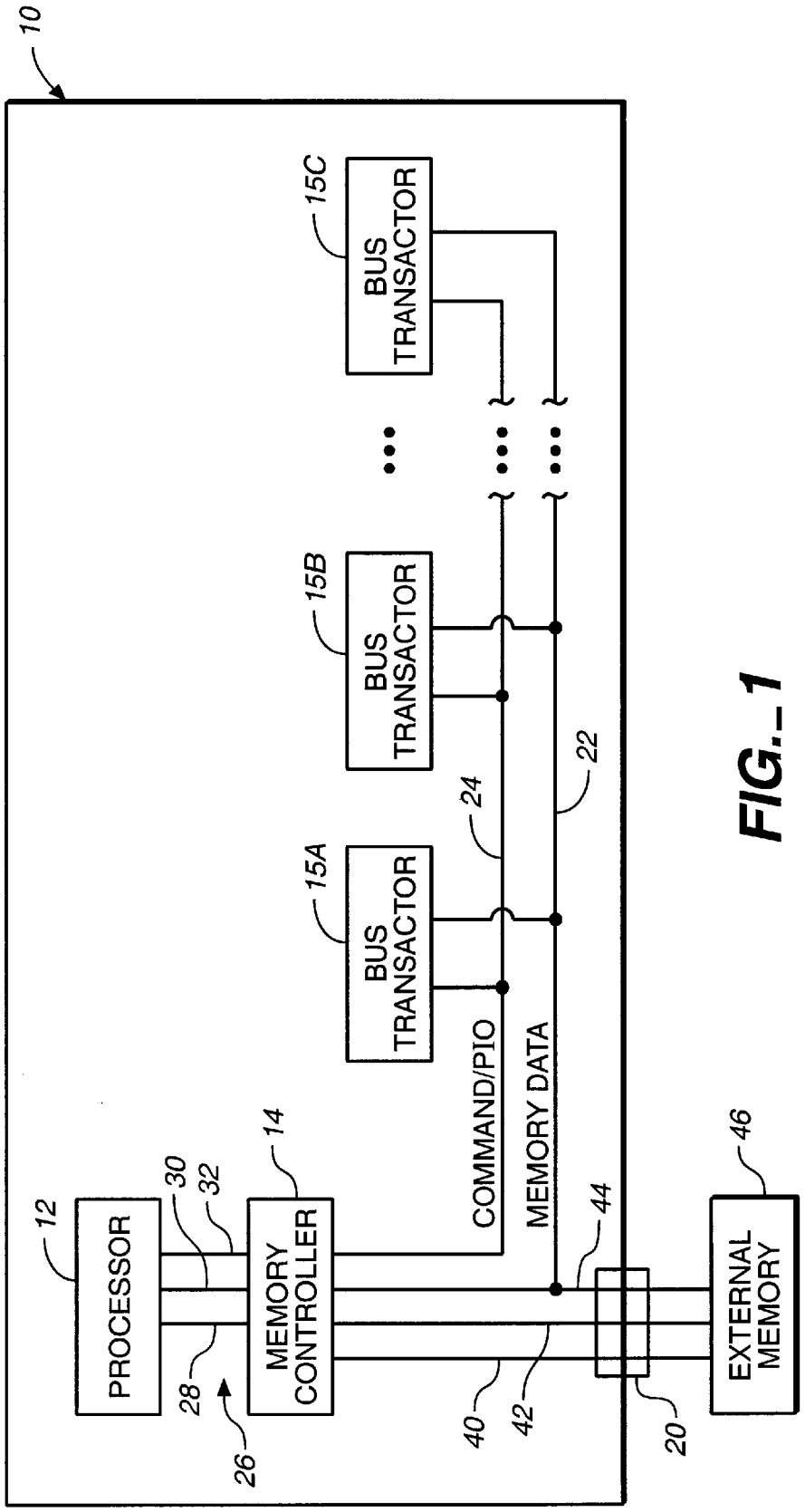


FIG._1

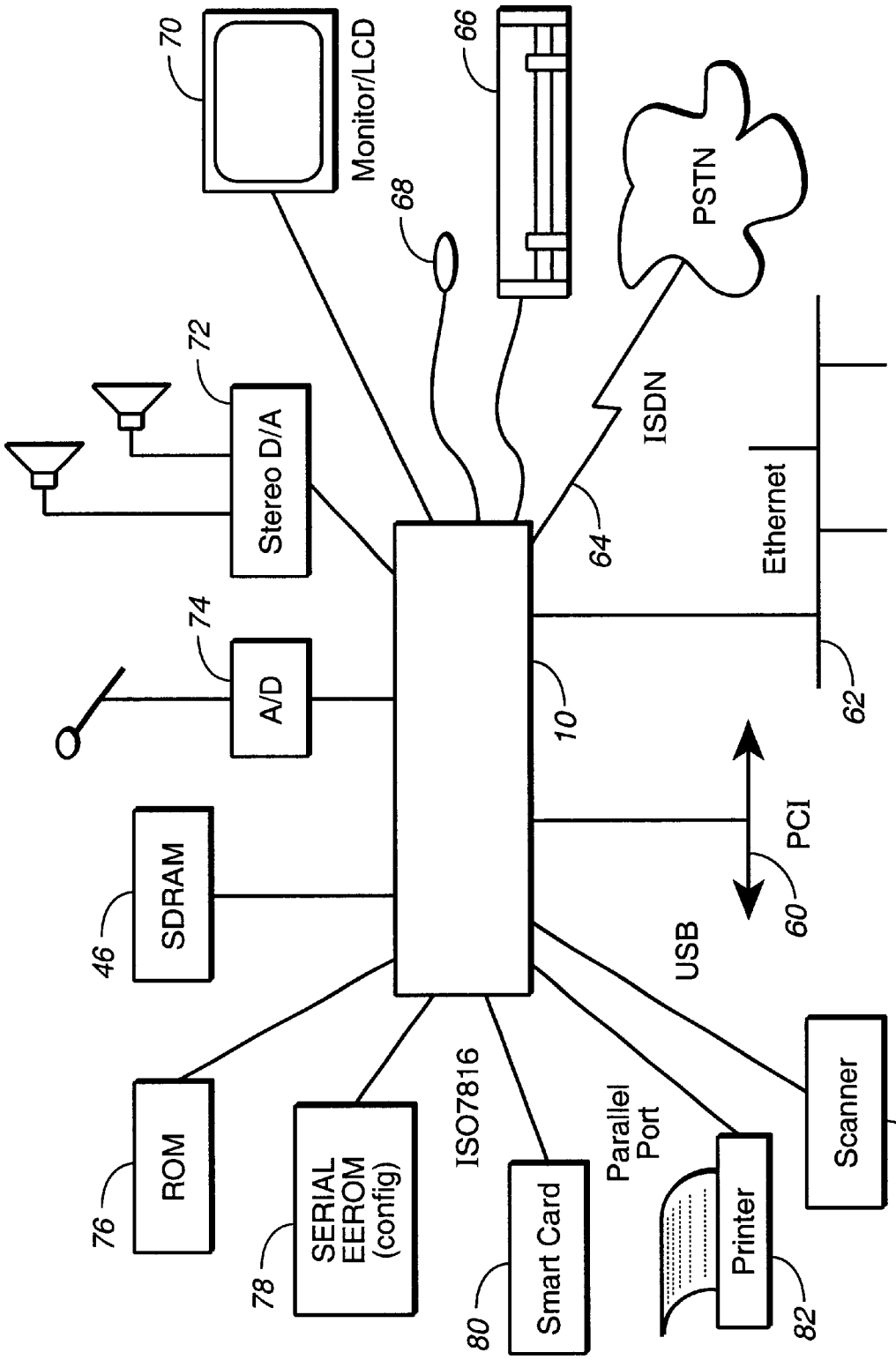


FIG._2

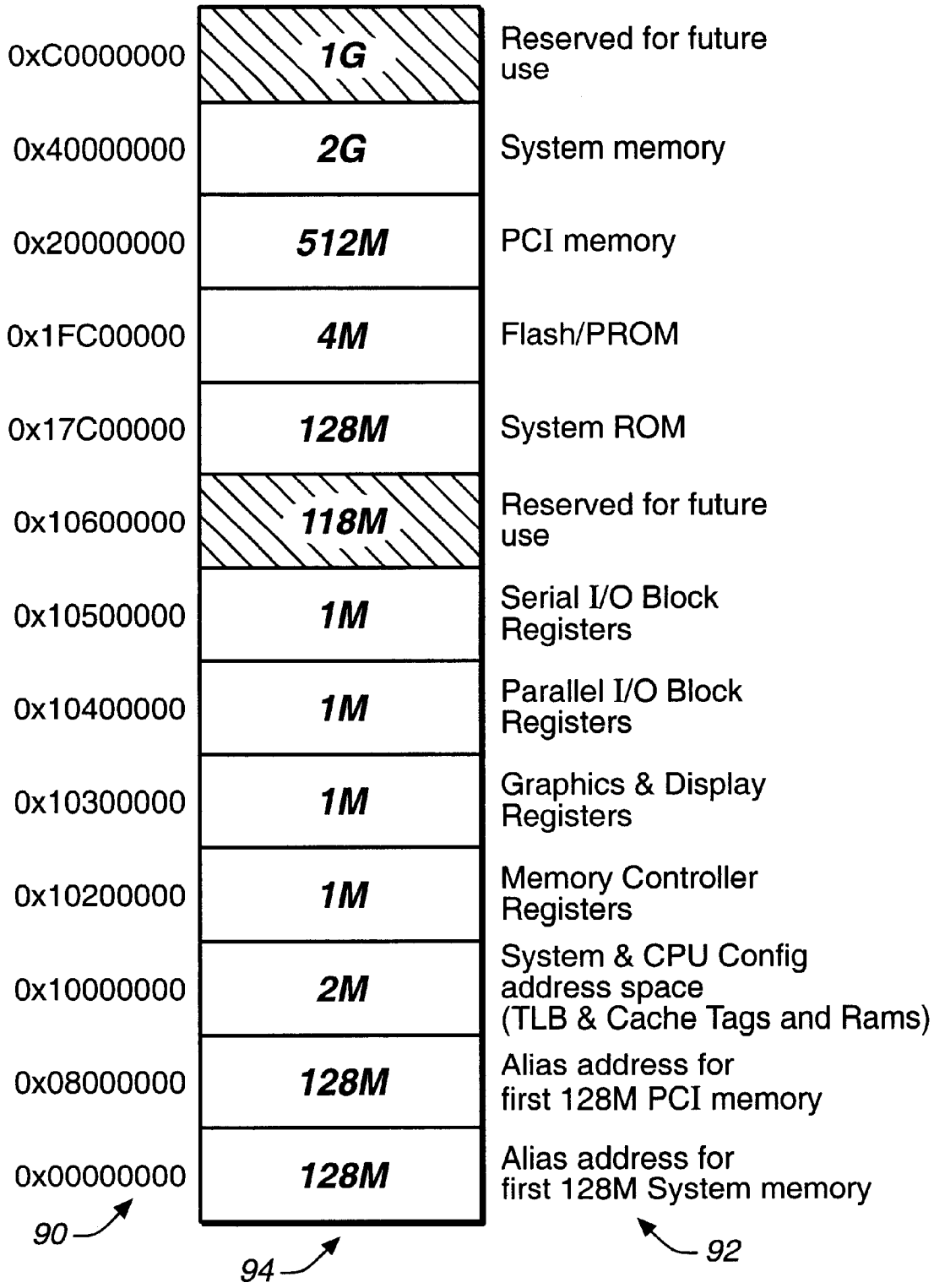


FIG._3

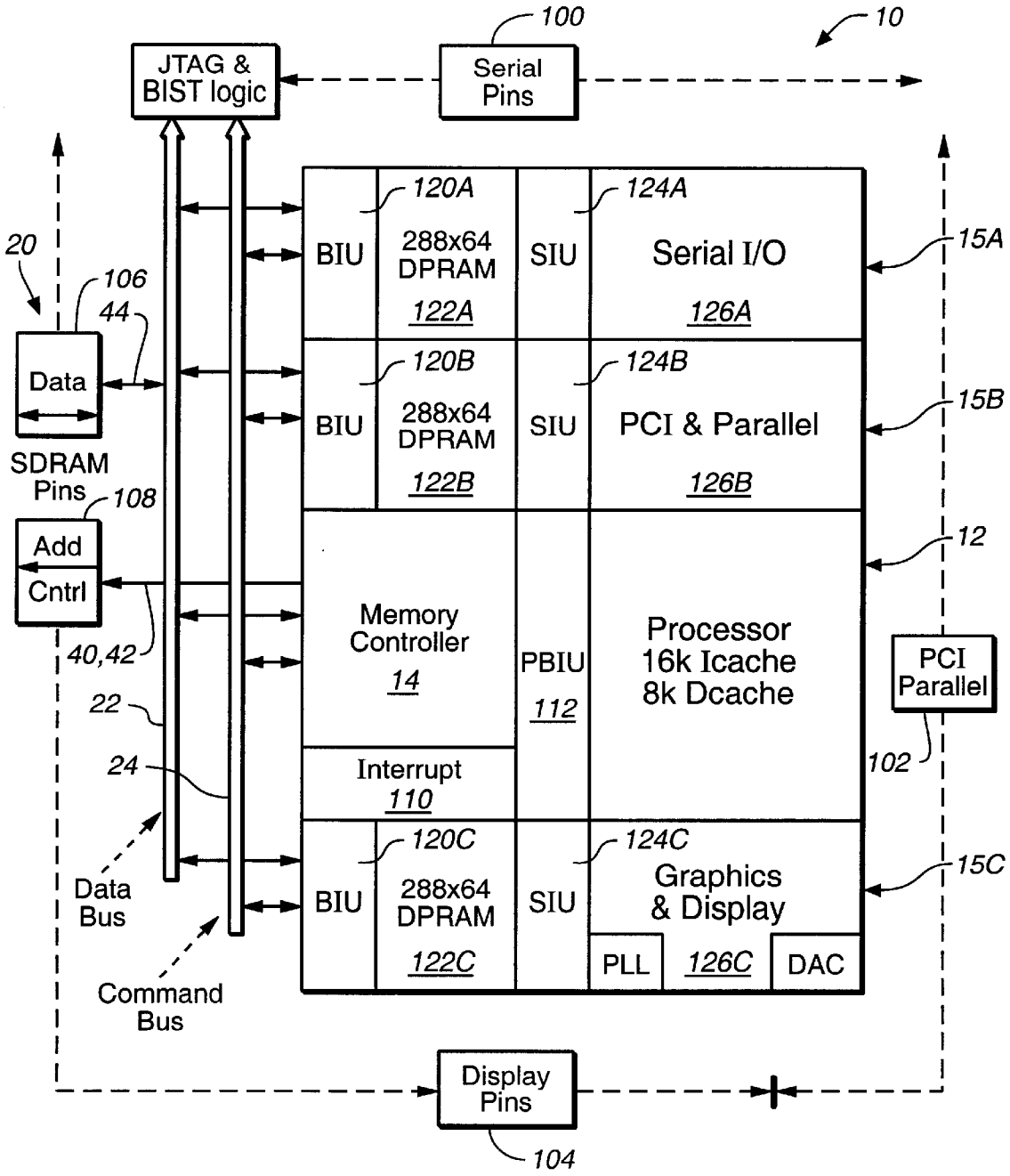


FIG._4

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