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Apostol, Jr. et al.

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(54) INTEGRATED CIRCUIT WITH UNIFIED MEMORY SYSTEM AND DUAL BUS **ARCHITECTURE**

(75) Inventors: George Apostol, Jr., Santa Clara; Peter

R. Baran, Fremont; Roderick J. McInnis, Milpitas, all of CA (US)

(73) Assignee: LSI Logic Corporation, Milpitas, CA

(US)

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Related U.S. Application Data

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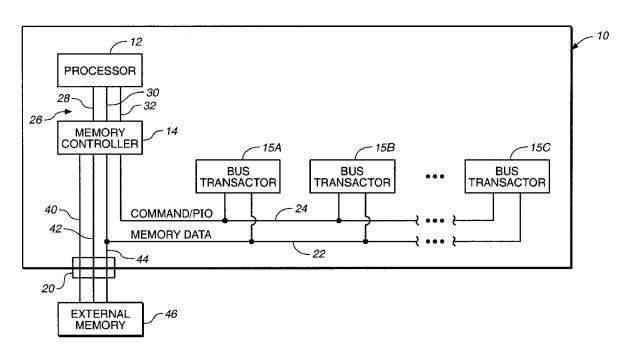
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Primary Examiner—Rupal D. Dharia

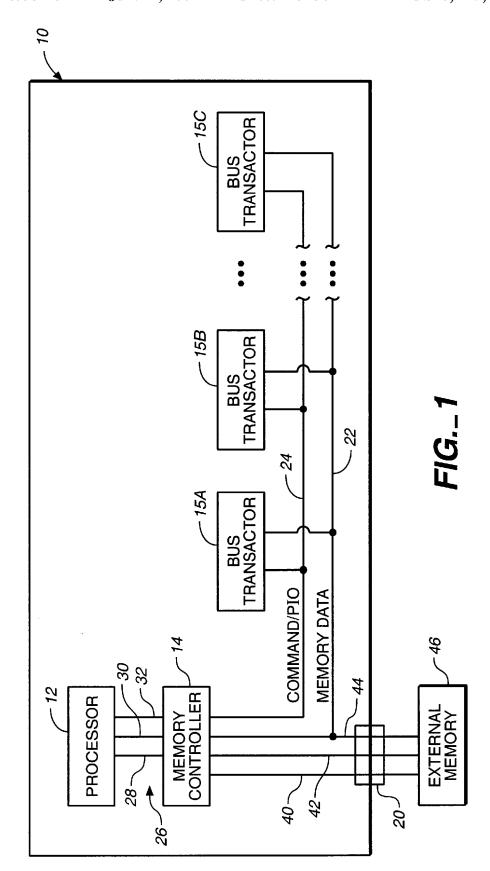
ABSTRACT

A unified memory system includes a processor, a memory controller, a plurality of bus transactor circuits and a shared memory port. A processor bus is coupled between the processor and the memory controller. A first multiple-bit, bidirectional system bus is coupled between the shared memory port, the memory controller and the plurality of bus transactor circuits. A second multiple-bit, bidirectional system bus is coupled between the memory controller and the plurality of bus transactor circuits.

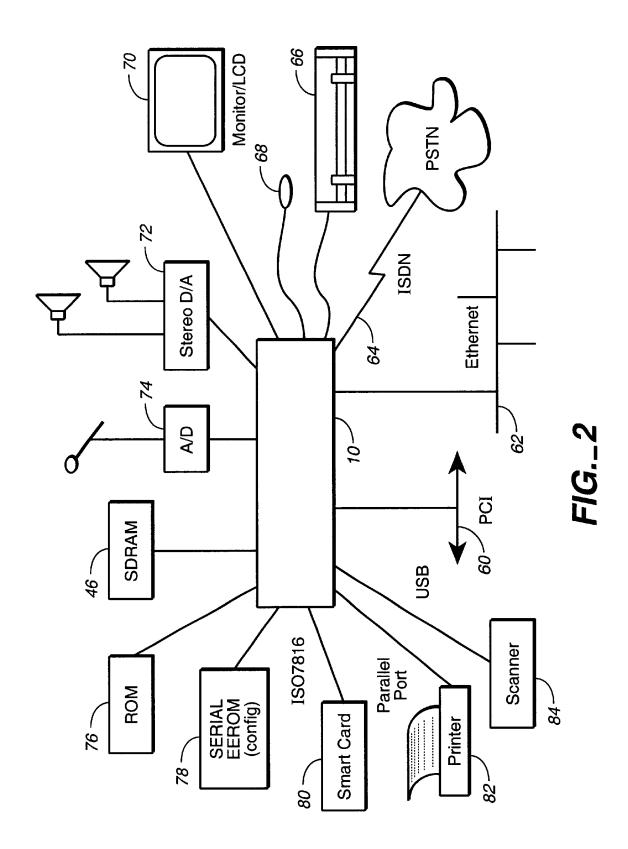
19 Claims, 36 Drawing Sheets













0xC0000000	1G	Reserved for future use
0x40000000	2G	System memory
0x20000000	512M	PCI memory
0x1FC00000	4M	Flash/PROM
0x17C00000	128M	System ROM
0x10600000	118M	Reserved for future use
0x10500000	1M	Serial I/O Block Registers
0x10400000	1M	Parallel I/O Block Registers
0x10300000	1M	Graphics & Display Registers
0x10200000	1M	Memory Controller Registers
0x10000000	2M	System & CPU Config address space (TLB & Cache Tags and Rams)
0x08000000	128M	Alias address for first 128M PCI memory
0x00000000	128M	Alias address for first 128M System memory
90	94	92

FIG._3



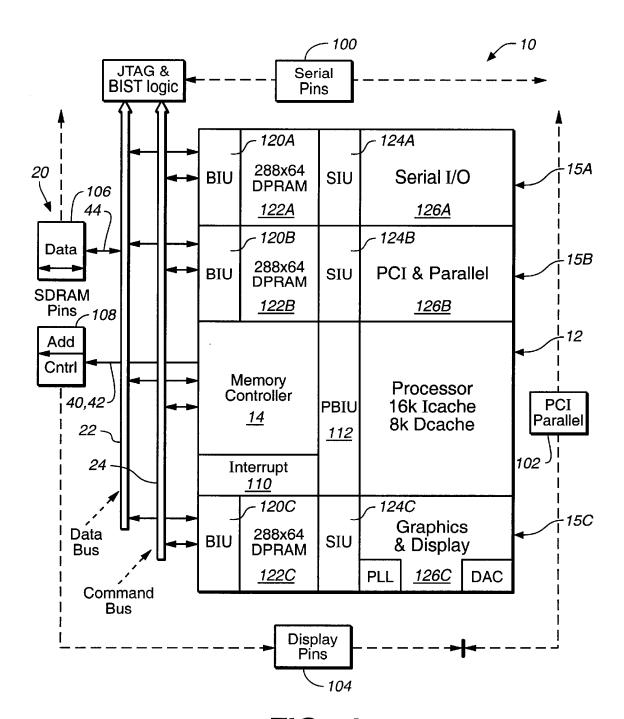


FIG._4

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