UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

MEMORY TECHNOLOGIES, LLC,
Patent Owner.

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Case IPR2019-00648
Patent 9,063,850 B2

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Before JAMESON LEE, J. JOHN LEE, and JASON M. REPKO,
Administrative Patent Judges.

LEE, J. JOHN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

INTRODUCTION

Kingston Technology Company, Inc.[1] ("Petitioner") filed a Petition
(Paper 1, "Pet.") requesting an *inter partes* review of claims 1–4, 9–13, 19–
22, and 27–31 ("the challenged claims") of U.S. Patent No. 9,063,850 B2
(Ex. 1001, "the '850 Patent").[2] Memory Technologies, LLC ("Patent
Owner") timely filed a Preliminary Response (Paper 6, "Prelim. Resp.").

We have authority to institute an *inter partes* review only if the
information presented in the Petition shows "there is a reasonable likelihood
that the petitioner would prevail with respect to at least 1 of the claims
challenged in the petition." 35 U.S.C. § 314(a). An *inter partes* review may
not be instituted on fewer than all claims challenged in the Petition. *SAS
Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

Upon consideration of the Petition and Preliminary Response, we
determine that the information presented shows there is a reasonable
likelihood that Petitioner would prevail in establishing the unpatentability of
the majority of the challenged claims, as discussed below. Accordingly, we
institute an *inter partes* review of the challenged claims of the '850 Patent.

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[1] Petitioner identifies Kingston Technology Corporation as an additional real
party-in-interest. Pet. 1.

[2] As Patent Owner points out (Prelim. Resp. 7), the Petition lacks a
certification under 37 C.F.R. § 42.104(a) that Petitioner "is not barred or
estopped from requesting an inter partes review" of the '850 Patent. We
granted leave to Petitioner to correct this error by filing the required
certification, which was filed on July 30, 2019. Paper 7.

A.   *Related Cases*

The parties identify as related to the present case the following pending district court case: *Memory Technologies, LLC v. Kingston Technology Co., Inc.*, 8:18-cv-00171 (C.D. Cal.). Pet. 2; Paper 4, 1. The parties further indicate a pending U.S. patent application and other cases before the Board may be related to the present case. Pet. 2; Paper 4, 1–2.

B.   *The '850 Patent*

The '850 Patent relates to "run-time configuration of mass memory devices." Ex. 1001, 1:13–15. The Specification describes that prior art memory devices typically are "optimized for one kind of application . . . with particular memory access characteristics." *Id.* at 1:36–38. "Due to this fixed optimization strategy, when a memory device is placed into a different environment with new access demands, it may fail to optimally perform under the requirements of the new environment." *Id.* at 1:41–44.

The claimed invention overcomes this deficiency via "run-time configuration" of memory devices. *Id.* at 1:58–60. The Specification describes "receiving one or more commands for activating one or more access profiles," and configuring access to the memory device in accordance with at least one of those profiles. *Id.* at 1:62–66. For example, the access profiles may "correspond to at least one of a random and a sequential mode of access." *Id.* at 1:66–2:1, 4:49–59. The active access profile "governs the current access operations to the memory device," so the device may be set to a different access configuration by changing the active profile. *Id.* at 4:59–5:11; *see id.* at 5:42–6:18, Fig. 3.

C. Challenged Claims

Petitioner challenges claims 1–4, 9–13, 19–22, and 27–31 of the '850 Patent. Claims 1, 10, 19, and 28 are independent claims. Claim 1 is illustrative and is reproduced below:

> 1. A memory device comprising:
>
> one or more registers to store one or more predefined access profiles associated with the memory device, the one or more predefined access profiles used to determine how access to the memory device is configured for at least one usage; and
>
> a controller configured to:
>
> > receive at least one first command to activate at least one of the one or more predefined access profiles; and
> >
> > receive at least one second command to designate the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage.

D. Asserted Grounds of Unpatentability and Asserted Prior Art

Petitioner asserts that the challenged claims are unpatentable based on the combinations of alleged prior art references below. Petitioner also relies on the Declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002).

References	Basis	Claims Challenged
CompactFlash[3]	§ 102(b)	1, 3, 9, 10, 12, 19, 21, 27, 28, 30

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[3] CompactFlash Association, *CF+ and CompactFlash Specification Revision 3.0*, dated Dec. 23, 2004 (Ex. 1003, "CompactFlash").

References	Basis	Claims Challenged
Ziv[4] and Vogt[5]	§ 103(a)	1, 3, 9, 10, 12, 19, 21, 27, 28, 30
Ziv, Vogt, and eMMC[6]	§ 103(a)	4, 13, 22, 31
CompactFlash and Elhamias[7]	§ 103(a)	2, 11, 20, 29
Ziv, Vogt, and Elhamias	§ 103(a)	2, 11, 20, 29
Sinclair[8]	§ 102(b)	1, 3, 9, 10, 12, 13, 19, 21, 27, 28, 30
Sinclair and eMMC	§ 103(a)	13

ANALYSIS

A. *Level of Ordinary Skill*

Based on the testimony of Dr. Baker, Petitioner asserts that a person of ordinary skill in the art would have had "at least a bachelor's degree in electrical engineering, computer engineering, or equivalent training, with at least two years of academic or industry experience in the field of memory system design." Pet. 4 (citing Ex. 1002 ¶ 65). Patent Owner contends that a

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[4] U.S. Patent No. 7,478,248 B2, filed Nov. 27, 2002, issued Jan. 13, 2009 (Ex. 1004, "Ziv").

[5] U.S. Patent No. 6,681,304 B1, issued Jan. 20, 2004 (Ex. 1005, "Vogt").

[6] JEDEC, *MultiMediaCard Association (MMCA) and the JEDEC Solid State Technology Association (JEDEC) Announce eMMC for Embedded Flash Memory Applications*, dated Dec. 20, 2006 (Ex. 1016, "eMMC").

[7] U.S. Patent Application Publication No. 2006/0022054 A1, published Feb. 2, 2006 (Ex. 1006, "Elhamias").

[8] U.S. Patent No. 7,409,489 B2, filed Oct. 25, 2005, issued Aug. 5, 2008 (Ex. 1017, "Sinclair").

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