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Paper 9
Entered: August 30, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

MEMORY TECHNOLOGIES, LLC,
Patent Owner.

Case IPR2019-00651
Patent 7,739,487 B2

Before JAMESON LEE, J. JOHN LEE,
and JASON M. REPKO, *Administrative Patent Judges*.

LEE, JAMESON, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

On January 31, 2019, Petitioner filed a Petition to institute *inter partes* review of claims 6, 7, 13, 20, 21, 26, 42, and 52 ("the challenged claims") of U.S. Patent No. 7,739,487 B2 (Ex. 1001, "the '487 patent"). Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

To institute an *inter partes* review, we must determine that the information presented in the Petition shows "that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Having considered all submissions of both parties, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in establishing the unpatentability of any of the challenged claims.

Accordingly, we do not institute review of any of claims 6, 7, 13, 20, 21, 26, 42, and 52 on any alleged grounds of unpatentability asserted in the Petition.

B. Related Matters

The parties identify a civil action involving the '487 patent: *Memory Techs., LLC v. Kingston Tech. Corp.,* No. 8-18-cv-00171 (C.D. Cal.). Pet. 2; Paper 4, 1. Petitioner has filed other Petitions for *inter partes* review of other patents involved in that civil action: IPR2019-00638, IPR2019-00642, IPR2019-00643, IPR2019-00644, IPR2019-00645, IPR2019-00648, and IPR2019-00654.

Patent Owner further identifies the following terminated litigation involving the '487 patent: *Memory Techs., LLC v. SanDisk LLC*, No. 8-16-

cv-02163 (C.D. Cal.). Paper 3, 1. Patent Owner additionally identifies another petition for *inter partes* review of claims in the '487 patent: IPR2017-00978 (terminated prior to institution decision). *Id.* The petitioner in IPR2017-00978 is not the petitioner in this proceeding.

C. The '487 Patent

The '487 patent is directed to a system and method for booting a host device from a peripheral device via a MultiMediaCard ("MMC") or Secure Digital ("SD") interface. Ex. 1001, Abstract, 2:35–37. The '487 patent discloses a conventional MMC/SD interface that comprises four terminals: a power terminal, a data (DAT) terminal, a clock (CLK) terminal, and a command (CMD) terminal. *Id.* at 2:29–40. Figure 5 of the '487 patent is reproduced below.

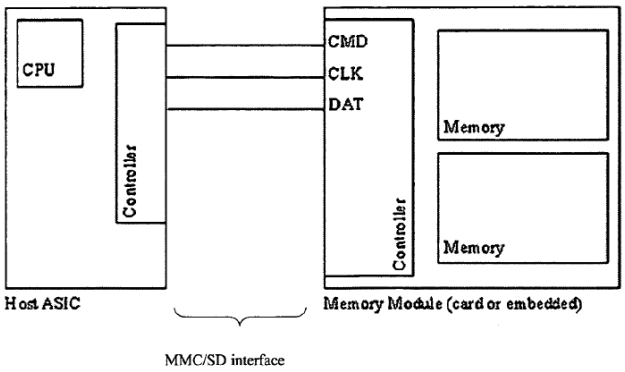

FIG. 5

Figure 5 shows a peripheral device that has a conventional MMC/SD interface and is coupled to a host device. *Id.* at 14:5–7. The host device includes a processing unit, i.e., a CPU, and a MMC/SD interface controller. *Id.* at 15:62–65. The MMC/SD interface of Figure 5 shows CMD, CLK, and DAT terminals. *Id.* at 15:65–67. The peripheral device (also termed memory module or MMC/SD memory card) includes a peripheral device

controller that serves "as a mediator between the interface and the memory module and serves to control all procedures to be performed between [the] MMC/SD interface and [the] memory module." *Id.* at 15:67 through 16:4. The '487 patent omits other details, such as the aforementioned power terminal, to avoid overcomplicating Figure 5. *Id.*

The '487 patent discloses a boot procedure that uses the MMC/SD interface to indicate to a memory component that it should fetch its first data sector during the power-up process of a host device. *Id.* at 3:45–50, 5:45–52, 5:63–67. Importantly, the disclosed methods may be performed with memory cards that have a conventional MMC/SD interface. *Id.* 2:16–25; *see also*, *e.g.*, *id.* at 6:40–43, 17:23–26; 2:19–34. The boot procedure does not require modifications to either the electrical interface or form factor used in the conventional MMC/SD interface. *Id.* Because the disclosed embodiments of the boot procedure use the pin configuration already used in an MMC/SD interface, the described methods do not require the addition of separate pins in order to indicate to a memory component that it should fetch a data sector during the power-up process of a host device. *Id.* In this manner, the boot procedure is compatible with existing MMC and SD cards and does not require changes to their interface. *Id.* at 2:22–25.

The '487 patent discloses three embodiments of the boot procedure, all of which involve the peripheral device detecting an "unexpected" signal at the CMD terminal, which in turn causes the peripheral device to transmit boot data to the host device in order to boot up the host device. *Id.* at 3:51–56, 5:53–59. Two embodiments consist of receiving from the host device a low signal via the CMD terminal at the peripheral device (*id.* at Figs. 1–2, 3:45–50, 3:63 through 4:2), and one embodiment consists of receiving from

the host device an argument via the CMD terminal at the peripheral device (*id.* at Fig. 3, 5:45–52). Figure 1 of the '487 patent is reproduced below.

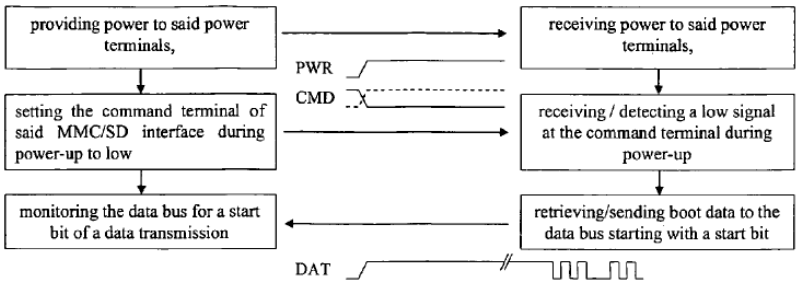

FIG. 1

Figure 1 is a flowchart that shows the actions performed at the host device and the peripheral device, according to one aspect of the invention. *Id.* at 14:23–27, 14:37–38. The flowchart on the left depicts those actions that occur at the host device. *Id.* at 14:23–27. The flowchart portion on the right depicts those actions that take place at the peripheral device having an MMC/SD interface. *Id.* The middle portion depicts the direction of signal transmissions (i.e., from host device to the peripheral device or vice versa) and the form of the transmitted signals at the corresponding terminal of the MMC/SD interface. *Id.* at Fig. 1.

The flowchart begins with the host device providing power to the power terminal of the MMC/SD interface, and thus the peripheral device receives said power signal at the MMC/SD interface. *Id.* at 14:41–45. Simultaneously or subsequently, the host device provides a low signal at the CMD terminal of the MMC/SD interface. *Id.* at 14:46–47. The peripheral device detects this low signal as an "unexpected" signal and interprets it as a boot request. *Id.* at 14:47–55. As a result, the peripheral device then retrieves boot data from a dedicated file or memory area and sends the boot data via the DAT terminal to the host device. *Id.* at 14:54–59. Accordingly,

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