UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

MEMORY TECHNOLOGIES, LLC,
Patent Owner.

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Case IPR2019-00654
Patent 7,565,469 B2

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Before JAMESON LEE, J. JOHN LEE,
and JASON M. REPKO, *Administrative Patent Judges*.

LEE, JAMESON, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

On January 31, 2019, Petitioner filed a Petition to institute *inter partes* review of claims 19 and 20 of U.S. Patent No. 7,565,469 B2 (Ex. 1001, "the '469 patent"). Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

To institute an *inter partes* review, we must determine that the information presented in the Petition shows "that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Having considered all submissions of both parties, we exercise discretion under 35 U.S.C. § 325(d) not to institute review, and further find, in the alternative, that Petitioner has not shown a reasonable likelihood that it would prevail in establishing the unpatentability of either claim 19 or claim 20 on any alleged ground of unpatentability.

B. Related Matters

The parties identify a civil action involving the '469 patent: *Memory Technologies, LLC v. Kingston Technology Corp., et al.,* No. 8-18-cv-00171 (C.D. Cal.). Pet. 2, Paper 3, 1. Patent Owner further identifies the following terminated litigations involving the '469 patent: *Memory Technologies, LLC v. SanDisk LLC et al.*, No. 8-16-cv-02163 (C.D. Cal.); *Certain Memory Devices and Components Thereof*, No. 337-TA-1034 (ITC). Paper 3, 1. Patent Owner additionally identifies another petition for *inter partes* review of claims in the '469 patent: IPR2017-00979 (terminated prior to institution decision). *Id.* The petitioner in IPR2017-00979 is not the petitioner in this proceeding.

C.   The '469 Patent

The '469 patent is directed to an interface over a bus between a first
unit and a second unit, where the bus includes a data signal line. Ex. 1001,
1:57–59. First information is driven over the data signal line from the first
unit to the second unit, and the second unit causes a change of state of the
data signal line to convey a first meaning. *Id.* at 1:59–63. In response to
that change of state of the data signal line, the first unit drives second
information to the second unit over the data signal line. *Id.* at 1:62–64.
Then the second unit causes a change of state of the data signal line to
convey a second meaning. *Id.* at 1:64–67. Thus, the meaning of a change of
state of the data signal line at the second unit varies depending on whether it
is first information or second information that is communicated from the
first unit to the second unit.

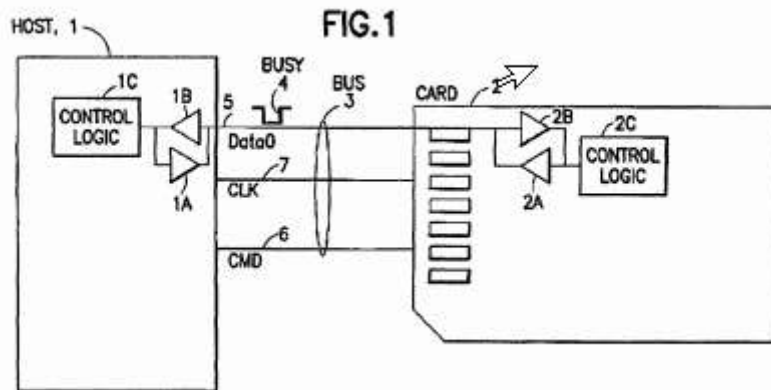Figure 1 of the '469 patent is reproduced below:

Figure 1 is a block diagram showing a first unit coupled to a second unit
over a bus. *Id.* at 3:39–40. The first unit is host 1, and the second unit is
memory card 2. *Id.* at 3:46–47. Connecting host 1 and memory card 2 is
bus 3 that includes data line 5, command line 6, and clock line 7. *Id.* at
3:46–50. Figure 1 illustrates busy signal 4 associated with data line 5. *Id.* at

3:47–48. Host 1 can be a cellular telephone, a digital camera, a PC, or any other suitable device that can use memory card 2. *Id.* at 3:60–62. Host 1 includes driver 1A and receiver 1B coupled to data line 5, and control logic 1C coupled to driver 1A and receiver 1B. *Id.* at 3:62–65. Memory card 2 includes driver 2A and receiver 2B coupled to data signal line 5, and control logic 2C coupled to driver 2A and receiver 2B. *Id.* at 3:66–4:3.

The '469 patent explains that because host devices typically implement a data block size, e.g., 16 k bytes, that is larger than the block size of data transferrable through an interface of a MultiMedia Card (MMC), e.g., 512 bytes, it is practical to use multiblock write commands. *Id.* at 1:32–39. The '469 patent further explains that in pre-existing operation of an MMC, busy signaling is used to indicate to the host device whether the buffers of the MMC are ready to receive next data. *Id.* at 1:24–28. The '469 patent also describes that generally there is only one busy signal line. *Id.* at 1:29–31. Based on this known configuration, the host device may transfer multiple 512 byte blocks of data to the MMC *without* having to poll the ready status of the MMC's buffers. *Id.* at 1:39–42.

The '469 patent describes a "problem" associated with sending the very last data block during execution of a multiblock write command. *Id.* at 1:43–44. When there are no more data blocks to be transferred, the host device has to learn whether the MMC has finished programming all of the received data blocks in the buffer, and thus needs to poll the MMC for its program ready status. *Id.* at 1:45–48. The '469 patent describes this need as "an inefficient use of the host's processing capacity." *Id.* at 1:48–50.

The '469 patent describes changing the meaning of busy signal 4 during command execution. *Id.* at 4:4–6. For instance, in a multiblock data

transfer operation of the MMC, for the first data blocks that are transmitted from the host device, busy signal 4 from the MMC is used by the MMC to indicate its "buffer busy/ready" status and is so interpreted by the host device, according to a pre-existing definition of busy signal 4. *Id.* at 4:6–9. For the last data block transferred, however, busy signal 4 is used by the MMC differently, to indicate its "programming ready/busy" status, which is not according to the pre-existing definition for busy signal 4. *Id.* at 4:9–10. The '469 patent describes that during the data transfer operation there may be data programming taking place within the MMC in connection with the transferred data, and this "programming busy/ready" status, as conveyed by busy signal 4, informs the host device when internal programming of the MMC is completed. *Id.* at 4:10–15.

The '469 patent explains that by using the invention described therein, there is no need for the host device to have to poll the internal "program busy/ready" status of the MMC, and thus the resources of the host device are conserved. *Id.* at 4:16–19.

Claims 19 and 20 are reproduced below:[1]

19. A memory device comprising:

[a] a bus interface configured to be coupled to a host through a bus having a data signal line,

[b] the bus interface further comprising a driver at said memory device coupled to said data signal line and a receiver at said memory device coupled to the data signal line, said receiver being operable to receive information comprising a first information portion and a second

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[1] The alphabetical labels for each limitation, in brackets, are added by Petitioner. Pet. 30–38.

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