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United States Patent [19]

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Russell

[45] Date of Patent: **Jul. 14, 1998**

[54] **OPEN DRAIN OUTPUT DRIVER HAVING DIGITAL SLEW RATE CONTROL**

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5,483,188	1/1996	Frodsham	327/170
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[57] ABSTRACT

[21] Appl. No.: **751,086**

An open drain driver circuit includes first and second NMOS driver transistors, a delay circuit, an OR gate and an AND gate. Each NMOS driver transistor has a drain coupled to an output terminal, a source coupled to a supply terminal, and a gate. The delay circuit has an input coupled to the input terminal and has an output. The OR gate has a first input coupled to the input terminal, a second input coupled to the output of the delay circuit and an output coupled to the gate of the first NMOS transistor. The AND gate has a first input coupled to the input terminal, a second input coupled to the output of the delay circuit and an output coupled to the gate of the second NMOS transistor.

[22] Filed: **Nov. 15, 1996**

[51] Int. Cl.⁶ **H03K 5/12; H03K 17/16**

[52] U.S. Cl. **327/170; 327/379; 327/108**

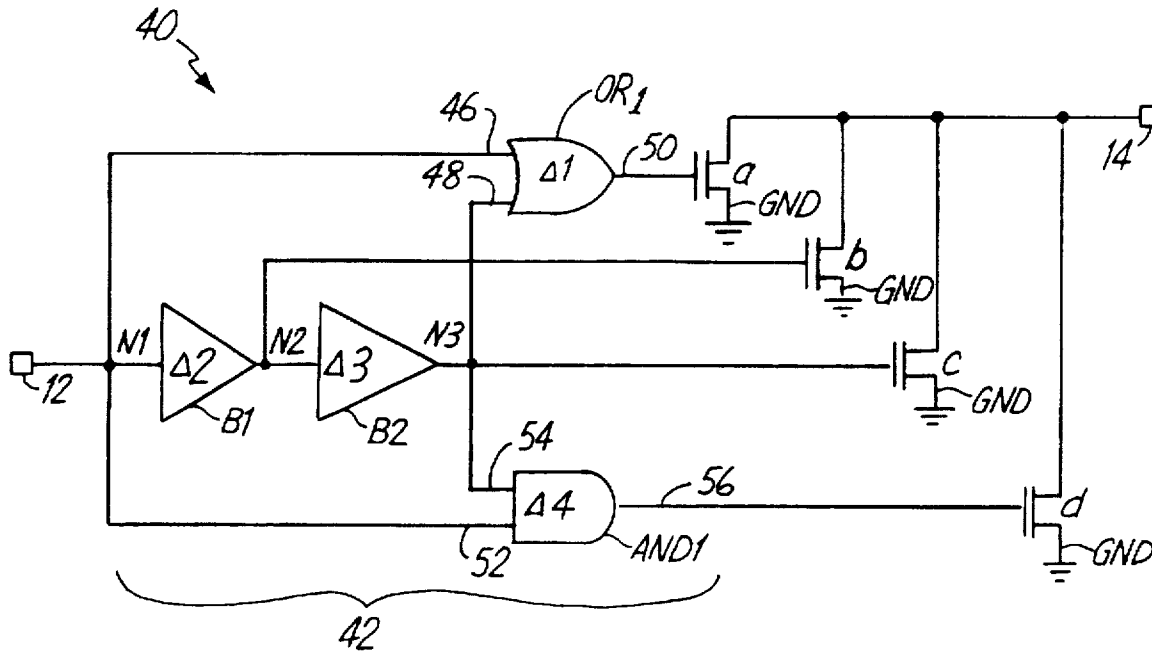
[58] Field of Search 327/134, 170, 327/379, 380, 381, 108, 109, 112; 326/26, 27

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12 Claims, 4 Drawing Sheets



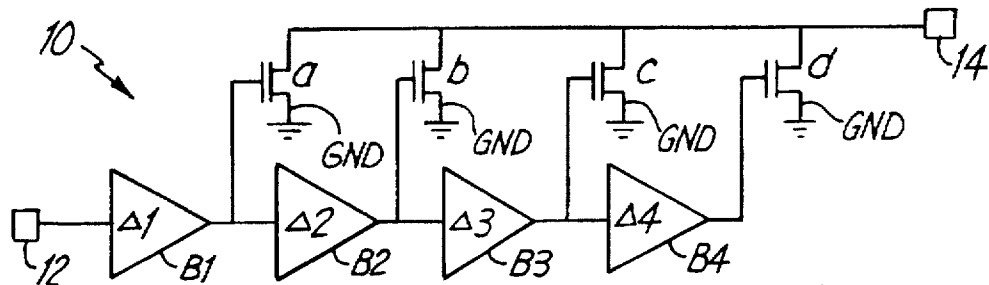


Fig. 1
(PRIOR ART)

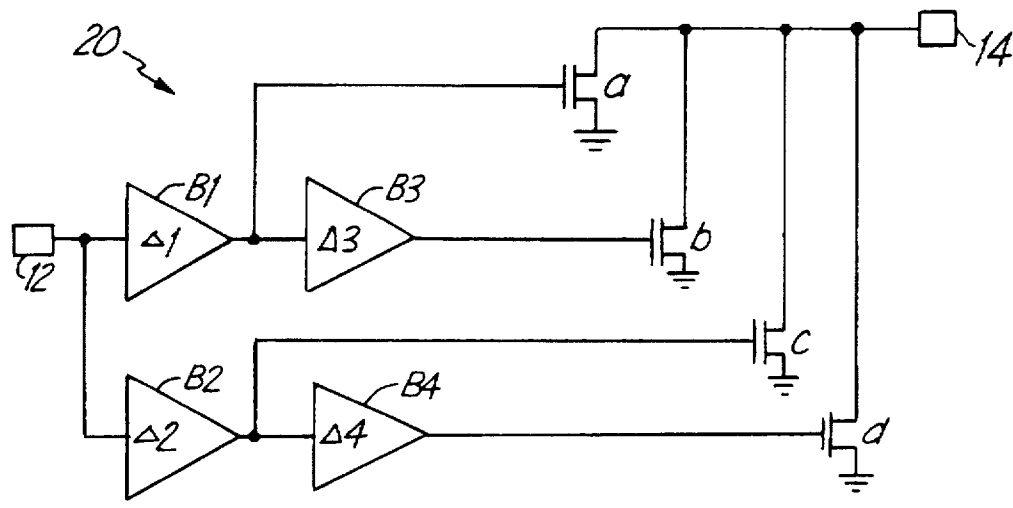


Fig. 2

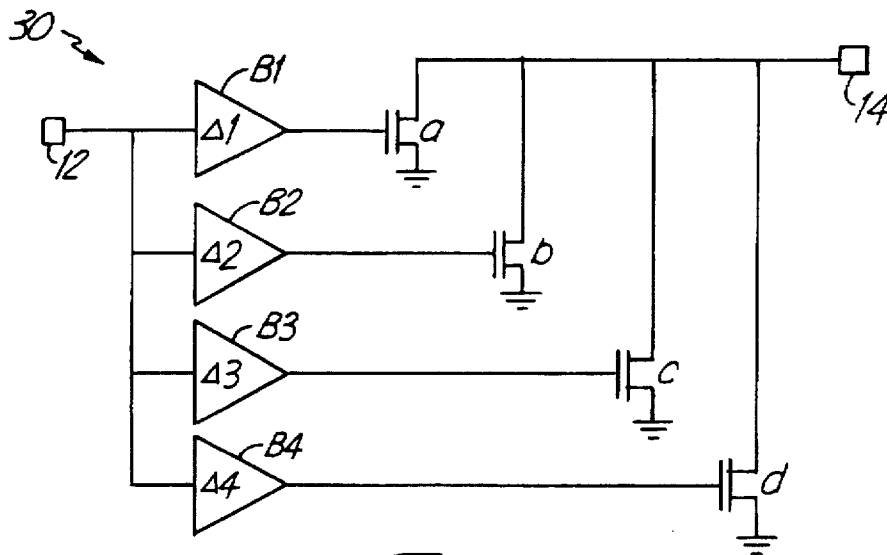


Fig. 3

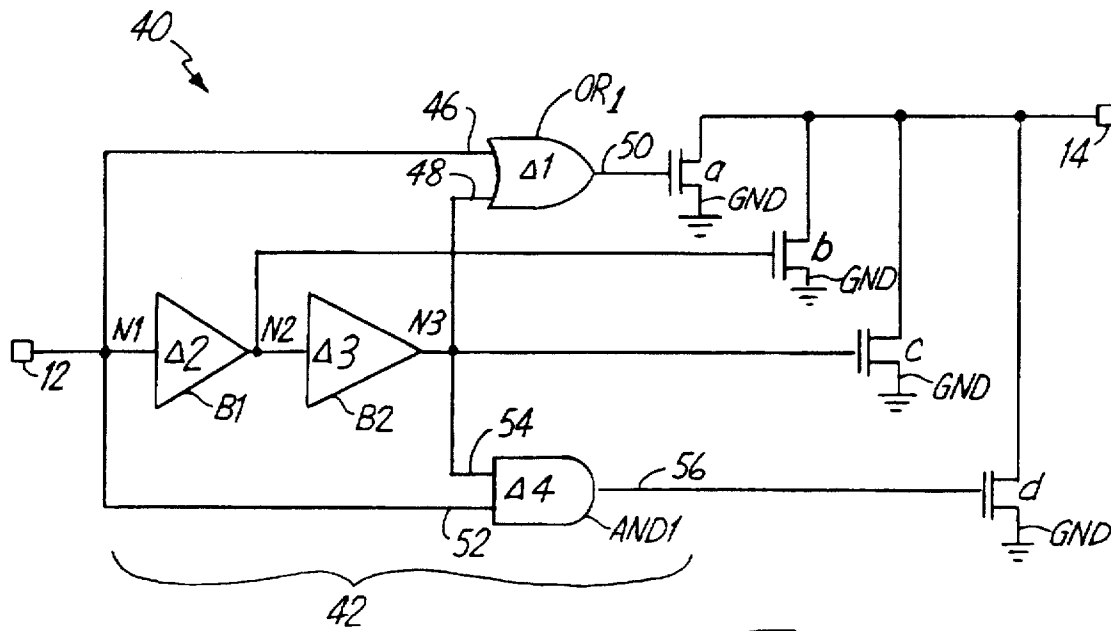


Fig. 4

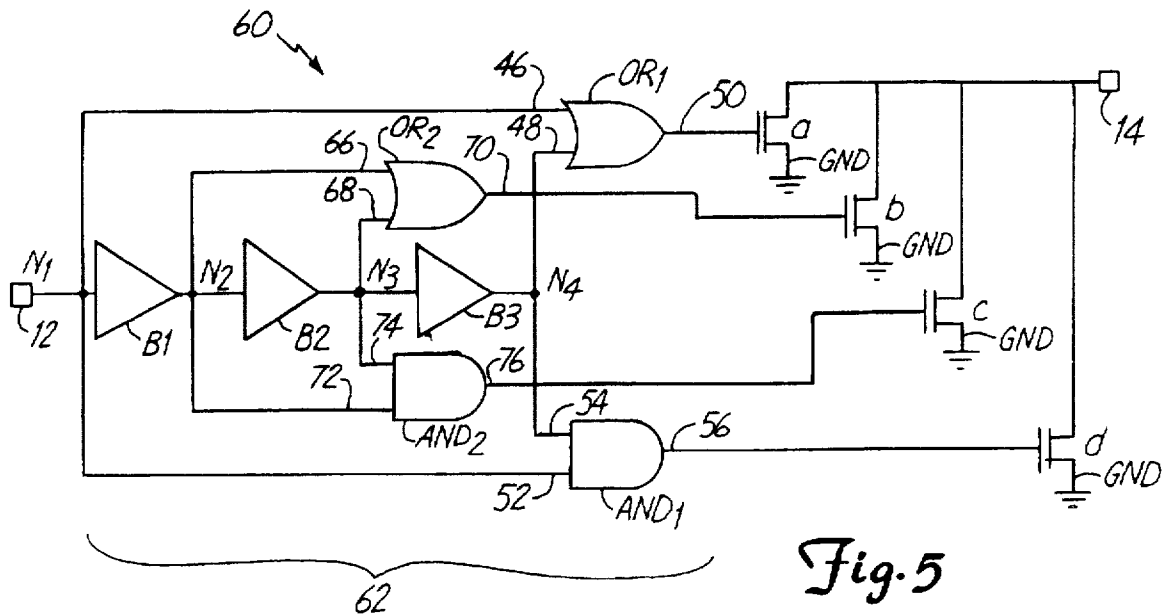


Fig. 5

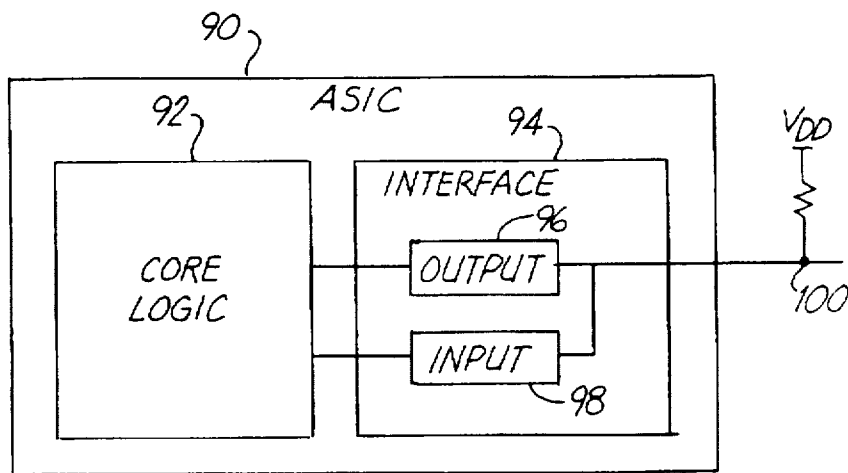


Fig. 7

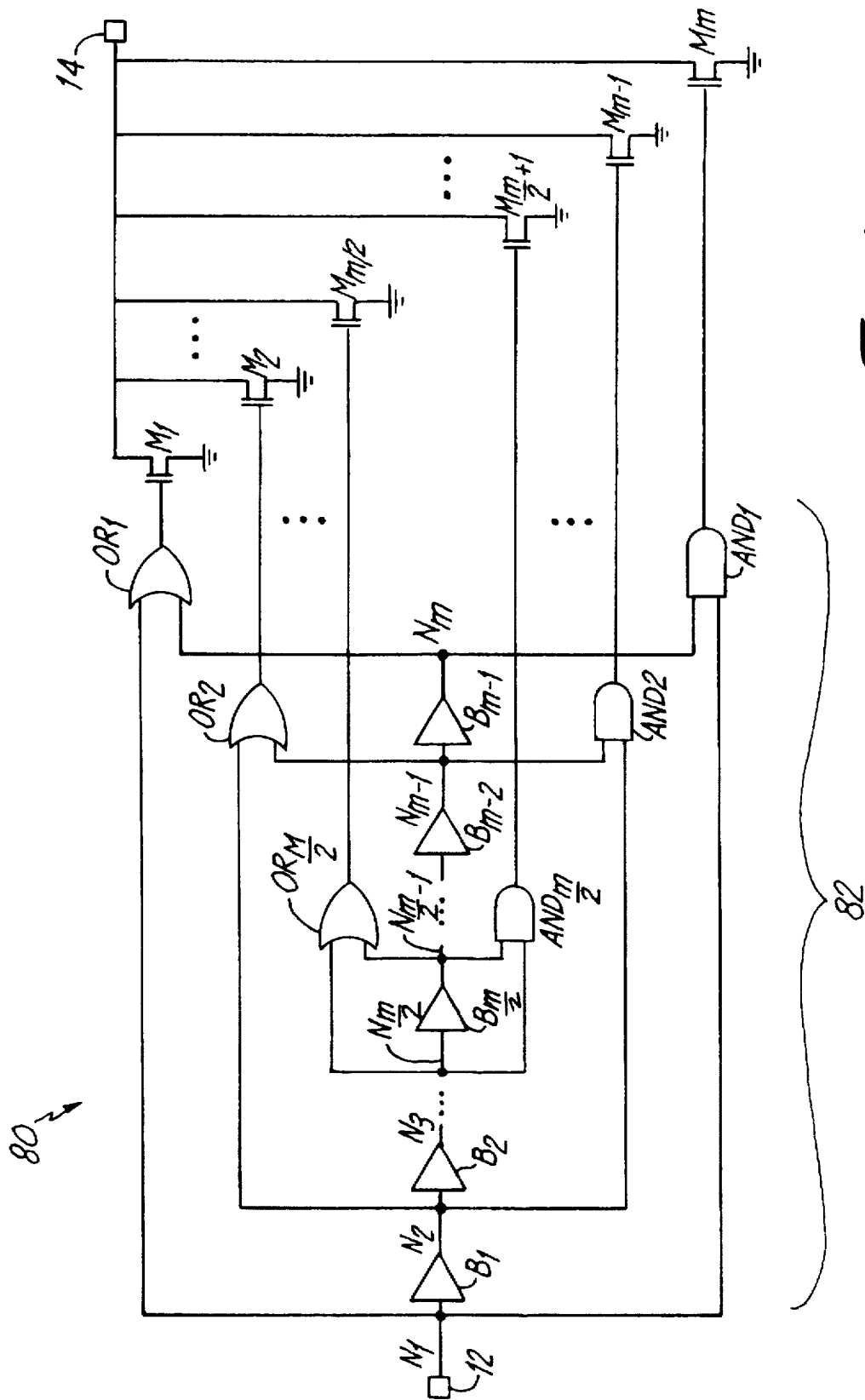


Fig. 6

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