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Paper 7
Entered: August 6, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNIFIED PATENTS INC.,
Petitioner,

v.

GE VIDEO COMPRESSION, LLC,
Patent Owner.

Case IPR2019-00726
Patent 6,943,710 B2

Before JONI Y. CHANG, JEFFREY W. ABRAHAM, and SCOTT B. HOWARD, *Administrative Patent Judges*.

HOWARD, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Unified Patents Inc. ("Petitioner") filed a Petition to institute an *inter partes* review of claims 25, 33, and 60–63 of U.S. Patent No. 6,943,710 B2 (Ex. 1001, "the '710 patent") pursuant to 35 U.S.C. §§ 311–319. Paper 2 ("Petition" or "Pet."). GE Video Compression, LLC ("Patent Owner") filed a Patent Owner Preliminary Response. Paper 6 ("Preliminary Response" or "Prelim. Resp.").

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). *Inter partes* review may not be instituted unless "the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). The Supreme Court held that a decision to institute under 35 U.S.C. § 314 may not institute on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

Based on the record before us, we are not persuaded that the information presented in the Petition demonstrates a reasonable likelihood that Petitioner would prevail in proving that at least one challenged claim would have been obvious under 35 U.S.C. § 103(a) based on the cited references. Accordingly, we deny the Petition and do not institute an *inter partes* review.

A. Real Party-In-Interest

Petitioner identifies Unified Patents Inc. as the real party-in-interest. Pet. 79.

B. Related Proceedings

The parties state that the '710 patent "is not the subject of any related administrative or judicial proceedings." *Id.*; Paper 5, 1.

C. The '710 Patent

The '710 patent is titled "Method and Arrangement for Arithmetic Encoding and Decoding Binary States and a Corresponding Computer Program and a Corresponding Computer-Readable Storage Medium" and is directed to improved arithmetic coding[1] method that determines a partial interval size without multiplication:

> A method and arrangement for arithmetic encoding/decoding is described, wherein the probability estimation is performed by a finite state machine FSM, wherein the generation of N representative states of the FSM is performed offline. Corresponding transition rules are filed in the form of tables. In addition, a pre-quantization of the interval width R to a number of K pre-defined quantization values is carried out. With suitable dimensioning of K and N, this allows the generation of a table containing all K×N combinations of pre-calculated product values $R \times P_{LPS}$ for a multiplication-free determination of R_{LPS}.

Ex. 1001, at [54], [57].

According to the '710 patent, Figure 1 illustrates "the basic operations for a binary arithmetic coding" as used by the prior art where "the current partial interval is represented by the two values L and R, wherein L indicates the offset point and R the size (width) of the partial interval, wherein both quantities are respectively illustrated using b-bit integers." *Id.* at 1:22–27. Figure 1 is reproduced below:

[1] Unless indicated otherwise, all references to coding encompass both coding and decoding.

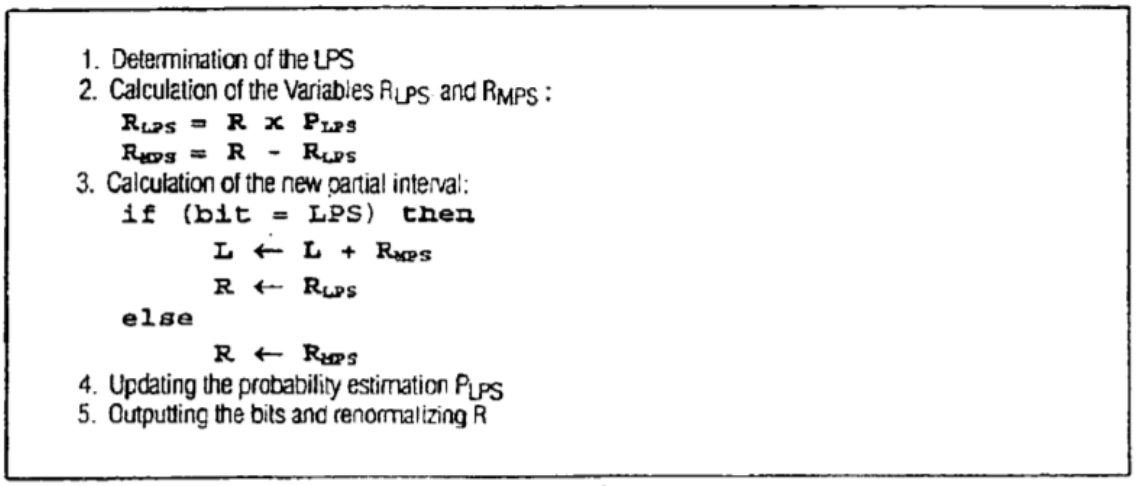

FIG. 1

Figure 1 "shows an illustration of the basic operations for a binary arithmetic coding." *Id.* at 9:59–60. As shown in Figure 1 above, the coding of a bit is performed in five steps:

> In the first step using the probability estimation the value of the less probable symbol is determined. For this symbol, also referred to as LPS (least probable symbol), in contrast to the MPS (most probable symbol), the probability estimation P_{LPS} is used in the second step for calculating the width R_{LPS} of the corresponding partial interval. Depending on the value of the bit to be coded L and R are updated in the third step. In the [fourth] step the probability estimation is updated depending on the value of the just coded bit and finally the code interval R is subjected to a so-called renormalization in the last step, i.e. R is for example rescaled so that the condition $R \in [2^{b-2}, 2^{b-1}]$ is fulfilled. Here, one bit is output with every scaling operation.

Id. at 2:29–41.

The '710 patent identifies a disadvantage associated with the prior art method of binary arithmetic coding. *Id.* at 2:43–48. According to the '710 patent, "the calculation of the interval width R_{LPS} requires a multiplication for every symbol to be coded" and that "multiplication operations, in

particular when they are realized in hardware, are cost- and time-intensive." *Id.*

The '710 patent states that it overcomes that disadvantage by performing arithmetic coding that "(a) do[es] not require a multiplication, (b) allow[s] a probability estimation without calculation effort and (c) simultaneously guarantee[s] a maximum coding efficiency over a wide range of typically occurring symbol probabilities." *Id.* at 3:14–23. In order to achieve these advantages, the '710 patent discusses using a modified scheme for a table-aided arithmetic coding, shown in Figure 2, reproduced below:

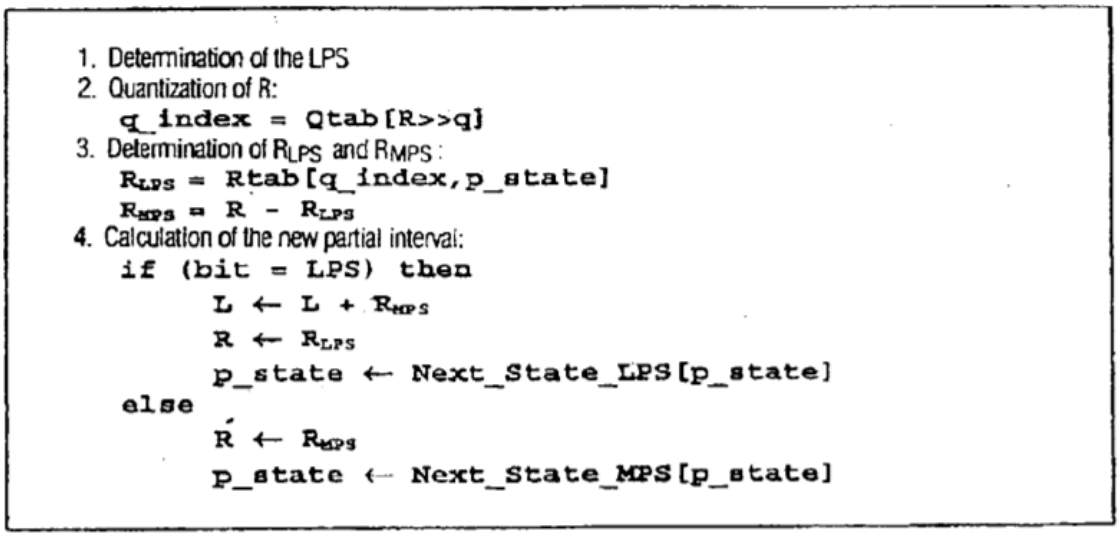

FIG. 2

Figure 2 "shows a modified scheme for a table-aided arithmetic encoding." *Id.* at 9:62–63. The modified scheme has four steps:

> After the determination of the LPS, first of all the given interval width R is mapped to a quantized value Q using a tabulated mapping Qtab and a suitable shift operation (by q bit)[.] Alternatively, the quantization may in special cases also be performed without the use of a tabulated mapping Qtab only with the help of a combination of shift and masking operations.

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