UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/078,150	03/11/2005	Marcus W. May	SIG000124

CONFIRMATION NO. 7355

146691
Daylight Law, P.C.
626 Jefferson Avenue
Suite 7
Redwood City, CA 94063

POA ACCEPTANCE LETTER

OC000000092558261

Date Mailed: 07/06/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/29/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nbekele/

INTEL 1006

UNITED STATES PATENT AND TRADEMARK OFFICE

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PO Box 1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/078,150	03/11/2005	Marcus W. May	SIG000124

CONFIRMATION NO. 7355

34399
GARLICK & MARKISON
106 E. 6th Street, Suite 900
AUSTIN, TX 78701

POWER OF ATTORNEY NOTICE

OC000000092558243

Date Mailed: 07/06/2017

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/29/2017.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nbekele/

PTO/AIA/80 (07-12)
Approved for use through 11/30/2018. OMB 0651-0035
U.S. Patent and Trademark Office: U.S DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 146691

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☐ The address associated with Customer Number:

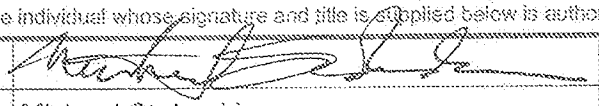
OR

☐	Firm or Individual Name			
	Address			
	City		State	Zip
	Country			
	Telephone		Email	

Assignee Name and Address: VLSI Technology LLC
1209 Orange Street
Wilmington, DE 19801

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	April 6, 2017
Name	Michael Stolarski	Telephone	
Title	CEO		

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: VLSI TECHNOLOGY LLC

Application No./Patent No.: 7,246,027 Filed/Issue Date: 07-17-2007

Titled: POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT

VLSI TECHNOLOGY LLC, a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. [✓] The assignee of the entire right, title, and interest.

2. [ ] An assignee of less than the entire right, title, and interest (check applicable box):

   [ ] The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   [ ] There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. [ ] The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. [ ] The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

A. [ ] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. [✓] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: MAY and FELDER To: SIGMATEL, INC., A DELAWARE CORPORATION

   The document was recorded in the United States Patent and Trademark Office at

   Reel 016380, Frame 0256, or for which a copy thereof is attached.

2. From: SIGMATEL, INC. To: SIGMATEL, LLC

   The document was recorded in the United States Patent and Trademark Office at

   Reel 039671, Frame 0293, or for which a copy thereof is attached.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: SIGMATEL, LLC To: VLSI TECHNOLOGY LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 039490, Frame 0680, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Eric Scheuerlein/	06-29-2017
Signature	Date
Eric Scheuerlein	61234
Printed or Typed Name	Title or Registration Number

[Page 2 of 2]

Electronic Acknowledgement Receipt

EFS ID:	29643117
Application Number:	11078150
International Application Number:	
Confirmation Number:	7355
Title of Invention:	POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Marcus W. May
Customer Number:	34399
Filer:	Ricky Quoc Lam
Filer Authorized By:	
Attorney Docket Number:	SIG000124
Receipt Date:	29-JUN-2017
Filing Date:	11-MAR-2005
Time Stamp:	05:59:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	20170629_VLSI_POA.pdf	1645121 ca4664d8dc68cd0f0da5efa1b2998363 2a20d6	no	1

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	20170629_VLSIP020_statement 37CFR.pdf	76276 09f0e6402ab12cb55f0584bbb6393276c41 3051e	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1721397	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/078,150	07/17/2007	7246027	SIG000124	7355

34399 7590 06/27/2007

GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Marcus W. May, Austin, TX;
Matthew D. Felder, Austin, TX;

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIBDATASHEET

CONFIRMATION NO. 7355

Bib Data Sheet

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/078,150	03/11/2005 RULE	702	2863	SIG000124

APPLICANTS

Marcus W. May, Austin, TX;
Matthew D. Felder, Austin, TX;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 04/07/2005

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☐ no	TX	10	24	4
35 USC 119 (a-d) conditions met	☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature Initials				

ADDRESS
34399

TITLE
POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT

FILING FEE RECEIVED		
1000	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

34399 7590 04/06/2007

GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/078,150	03/11/2005	Marcus W. May	SIG000124	7355

TITLE OF INVENTION: POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$0	$1000	07/06/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
SUN, XIUQIN	2863	702-130000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Garlick Harrison & Markison
2 Kevin L. Smith
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Sigmatel, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Austin, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-1415 (Sigmatel)(enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Kevin L. Smith/ Date June 12, 2007

Typed or printed name Kevin L. Smith, Reg. No. 38,620 Registration No. 38,620

Electronic Patent Application Fee Transmittal

Application Number:	11078150
Filing Date:	11-Mar-2005
Title of Invention:	POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Marcus W. May
Filer:	Kevin Lee Smith/Sherry Wolf McWhinnie
Attorney Docket Number:	SIG000124
Filed as Large Entity	

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1400	1400
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1700

Electronic Acknowledgement Receipt	
EFS ID:	1863586
Application Number:	11078150
International Application Number:	
Confirmation Number:	7355
Title of Invention:	POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Marcus W. May
Customer Number:	34399
Filer:	Kevin Lee Smith/Sherry Wolf McWhinnie
Filer Authorized By:	Kevin Lee Smith
Attorney Docket Number:	SIG000124
Receipt Date:	12-JUN-2007
Filing Date:	11-MAR-2005
Time Stamp:	14:34:21
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$1700
RAM confirmation Number	7430
Deposit Account	501415
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	SIG000124_Issue_fee_85B.pdf	1078852	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8328	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1087180		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

34399 7590 04/06/2007

GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
SUN, XIUQIN	
ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 04/06/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/078,150	03/11/2005	Marcus W. May	SIG000124	7355

TITLE OF INVENTION: POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$0	$1000	07/06/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

34399 7590 04/06/2007

GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/078,150	03/11/2005	Marcus W. May	SIG000124	7355

TITLE OF INVENTION: POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$0	$1000	07/06/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
SUN, XIUQIN	2863	702-130000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/078,150	03/11/2005	Marcus W. May	SIG000124	7355

34399 7590 04/06/2007

GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
SUN, XIUQIN	
ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 04/06/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/078,150	MAY ET AL.	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/06/2007*.

2. ☒ The allowed claim(s) is/are *1,3-9,11-16 and 18-24*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1, 3-9, 11-16 and 18-24 are allowed.

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

Please see applicant's response with respect to claims 1, 3-9, 11-16 and 18-24 received on 12/06/2007 for reasons for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

XS
March 30, 2007

John Barlow
Supervisory Patent Examiner
Technology Center 2800

Issue Classification	Application/Control No. 11/078,150	Applicant(s)/Patent under Reexamination MAY ET AL.
	Examiner Xiuqin Sun	Art Unit 2863

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
702	130	G	0	1	K 1	/00					/
CROSS REFERENCES						/					/
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					/					/
						/					/
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(Assistant Examiner) 08/31/07 (Date)

(Legal Instruments Examiner) 4/3/07 (Date)

John Barlow
Supervisory Patent Examiner
Technology Center 2800

(Primary Examiner) (Date) 3/30/07

Total Claims Allowed: 21

O.G. Print Claim(s)	O.G. Print Fig.
1	1

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181
	~~2~~		32		62		92		122		152		182
2	3		33		63		93		123		153		183
3	4		34		64		94		124		154		184
4	5		35		65		95		125		155		185
5	6		36		66		96		126		156		186
6	7		37		67		97		127		157		187
7	8		38		68		98		128		158		188
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10	12		42		72		102		132		162		192
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	~~17~~		47		77		107		137		167		197
15	18		48		78		108		138		168		198
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21	24		54		84		114		144		174		204
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	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
11/078,150	MAY ET AL.
Examiner	**Art Unit**
Xiuqin Sun	2863

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	3/31/07
1	1	=
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Claim	Date
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Claim	Date
Final	Original
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Bib Data Sheet

CONFIRMATION NO. 7355

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/078,150	03/11/2005 RULE	702	2863	SIG000124

APPLICANTS

Marcus W. May, Austin, TX;
Matthew D. Felder, Austin, TX;

** CONTINUING DATA ********** None

** FOREIGN APPLICATIONS ********** None

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 04/07/2005

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☑ no	TX	10	21 ~~24~~	4
35 USC 119 (a-d) conditions met	☐ yes ☑ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature / Initials XS				

ADDRESS
34399

TITLE

Power optimization of a mixed-signal system on an integrated circuit

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
700	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
11/078,150	MAY ET AL.	
Examiner	**Art Unit**	
Meagan S. Walling	2863	

SEARCHED			
Class	Subclass	Date	Examiner
702	130 117 121 124 60 64	9/1/2006	MW
377	19 20		
438	14 17 18		
Above updated		03/31/07	XS

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
702	130	03/31/07	XS

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search	9/1/2006	MW
702/130, 117 and word search		
377/19 and word search		
438/17 and word search		
East text search updated		XS
class search		
claims search		
702/130	03/31/07	XS

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	785	(702/130).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/27 14:15
S2	0	(adjust$3 or adjustment) with regulation with signal with converter with optimiz$3 with power with consumption and (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/28 10:16
S3	5	(adjust$3 or adjustment) with regulation with signal with converter with power and (integrated near4 circuit$3 or IC or chip or processor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/28 10:18
S4	2563	(702/130,117,121,64).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/27 14:19
S5	1304	(377/19,20).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/27 14:19
S6	6457	(438/14,17,18).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/27 14:19
S7	0	(S4 or S5 or S6) and (adjust$3 or adjustment) with regulation with signal with converter with optimiz$3 with power with consumption same (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/27 14:20
S8	0	(S4 or S5 or S6) and regulation with signal with converter with optimiz$3 with power with consumption same (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/28 10:20
S9	0	(S4 or S5 or S6) and regulation with signal with converter with power with consumption same (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/28 10:21

EAST Search History

S10	0	(S4 or S5 or S6) and regulation with signal with converter with power same (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/28 10:21
S11	0	(S4 or S5 or S6) and regulat$3 with signal with converter with power same (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/28 10:22
S12	0	(S4 or S5 or S6) and regulat$3 with signal with converter with power same (integrated with circuit or IC or chip or processor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/27 14:21
S13	0	(S4 or S5 or S6) and regulat$3 with signal with converter with power same (integrated with circuit$3 or IC or chip or processor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/27 14:22
S14	3	(S4 or S5 or S6) and DC with signal with converter with power same (integrated with circuit$3 or IC or chip or processor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/27 14:22
S15	1	(adjust$3 or adjustment) with regulation with signal with converter with power and (integrated near4 circuit$3 or IC or chip or processor or microprocessor or micro adj processor).clm.	US-PGPUB	OR	ON	2007/03/27 15:29
S16	0	(adjust$3 or adjustment) with regulation with signal with converter with optimiz$3 with power with consumption and (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/28 10:16
S17	8	(adjust$3 or adjustment) with regulation with signal with converter with power and (integrated near4 circuit$3 or IC or chip or processor or microprocessor or micro adj processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/28 10:18
S18	2563	(702/130,117,121,64).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 10:21
S19	1304	(377/19,20).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 10:21

EAST Search History

S20	6457	(438/14,17,18).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/28 10:21
S21	0	(S18 or S19 or S20) and regulation with signal with converter with optimiz$3 with power with consumption same (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/28 10:21
S22	0	(S18 or S19 or S20) and regulation with signal with converter with power with consumption same (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/28 10:21
S23	0	(S18 or S19 or S20) and regulation with signal with converter with power same (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/28 10:21
S24	0	(S18 or S19 or S20) and regulat$3 with signal with converter with power same (integrated with circuit or IC or chip o rprocessor or microprocessor or micro adj processor)	US-PGPUB	OR	ON	2007/03/28 10:22

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 11078150

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))			150			300	
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		x 25 =		OR	x 50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		x 100 =			x 200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
			TOTAL			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A (6-20-06)	Total (37 CFR 1.16(i))	24	Minus	24		x 25 =			x 50 =	
	Independent (37 CFR 1.16(h))	4	Minus	4		x 100 =			x 200 =	
	Application Size Fee (37 CFR 1.16(s))									
	First Presentation of Multiple Dependent Claim (37 CFR 1.16(j))									
					TOTAL ADD'L FEE					
AMENDMENT B	Total (37 CFR 1.16(i))		Minus			x =			x =	
	Independent (37 CFR 1.16(h))		Minus			x =			x =	
	Application Size Fee (37 CFR 1.16(s))									
	First Presentation of Multiple Dependent Claim (37 CFR 1.16(j))									
					TOTAL ADD'L FEE					

If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1 of a previous amendment or, if none, in column 2 of the last previous amendment.

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1 of a previous amendment or, if none, in column 2 of the last previous amendment.

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Send to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

DOCKET NO. SIG000124

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Marcus W. May
Serial No.	11/078,150
Filed:	March 11, 2005
For:	Power Optimization of a Mixed-Signal System on an Integrated Circuit
Group No.:	2863
Examiner:	Walling, Meagan S.

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICIAL ACTION UNDER 37 C.F.R. § 1.111

Sir:

Responsive to the Official Action having a mailed date of September 6, 2006, Applicant hereby makes the following arguments and remarks. As such, reconsideration of the action and allowance of the present application are respectfully requested and are believed to be appropriate in view of the following:

Amendment to the Specification – N/A

Amendment to the Claims begins on page 2 of this paper.

Amendment to the Drawings – N/A

Remarks begin on page 9 of this paper.

IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Currently Amended) A method for power supply optimization of an integrated circuit, comprising:

determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;

determining an operational temperature associated with the analog variation parameter; and

determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature; and

adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal to optimize power consumption of the integrated circuit~~, such that power consumption of the integrated circuit is optimized~~.

2. (Cancelled)

3. (Currently Amended) The method of ~~Claim 2~~ Claim 1 further comprises:

updating the adjustment signal by repeating at least one of the determination of the operational temperature and determining the adjustment signal.

4. (Currently Amended) The method of Claim 1, wherein the determining the adjustment signal further comprises:

determining a digital variation parameter; and

determining the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature.

5. (Original) The method of Claim 4 wherein the determining the adjustment signal comprises:

determining a first adjustment signal based on the analog variation parameter;

determining a second adjustment signal based on the digital variation parameter;

comparing the first adjustment signal to the second adjustment signal; and

when the first adjustment signal compares favorably with the second adjustment signal, selecting the first adjustment signal as the adjustment signal, else the second adjustment signal as the adjustment signal.

6. (Original) The method Claim 4, wherein determining a digital variation parameter comprises:

measuring processing speed of at least a portion of an integrated circuit to produce measured processing speed;

comparing the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit; and

when the measured processing speed compares favorably to the critical processing speed, correspondingly set a value of the digital variation parameter.

7. (Original) The method of Claim 4 further comprises:

adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal.

8. (Original) The method of Claim 7 further comprises:

updating the adjustment signal by repeating at least one of the determination of the operational temperature, the determination of the analog variation parameter, and of the digital variation parameter

9. (Currently Amended) An apparatus for increasing power supply efficiency of an integrated circuit comprises:

a processing module; and

a memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;

determine an operational temperature associated with the analog variation parameter; and

determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter and the operational temperature; and

adjust a regulation signal of a DC-to-DC converter based on the adjustment signal to optimize power consumption of the integrated circuit~~, such that power consumption of the integrated circuit is optimized~~.

10. (Cancelled)

11. (Currently Amended) The method of ~~Claim 10~~ Claim 9, wherein the memory further stores operational instructions that cause the processing module to:

update the adjustment signal by repeating at least one of the determination of the operational temperature and determine the analog variation parameter.

12. (Currently Amended) The apparatus of claim 9, wherein the memory further stores operational instructions that cause the processing module to determine the adjustment signal by:

determine a digital variation parameter; and

determine the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature.

13. (Original) The apparatus of claim 12, wherein the memory further stores operational instructions that cause the processing module to determine the digital variation parameter by:

measuring a processing speed of at least a portion of an integrated circuit to produce measured processing speed;

comparing the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit; and

when the measured processing speed compares favorably to the critical processing speed, set a corresponding value of the digital variation parameter.

14. (Original) The apparatus of claim 12, wherein the memory further stores operational instructions that cause the processing module to:

adjust a regulation signal of a DC-to-DC converter based on the adjustment signal.

15. (Original) The apparatus of claim 13, wherein the memory further stores operational instructions that cause the processing module to:

determine a first adjustment signal based on the analog variation parameter;

determine a second adjustment signal based on the digital variation parameter;

compare the first adjustment signal to the second adjustment signal; and

when the first adjustment signal compares favorably with the second adjustment signal, selecting the first adjustment signal as the adjustment signal, else selecting the second adjustment signal as the adjustment signal.

16. (Currently Amended) A comprehensive system-on-a-chip comprises:

a processing core operably coupled to process input digital data and produce therefrom output digital data;

digital interface circuitry operably coupled to provide the input digital data to the processing core and to receive the output digital data from the processing core;

mixed signal circuitry operably coupled to convert input analog signals into the input digital data and to convert the output digital data into output analog signals; and

battery optimization circuitry that includes a DC-to-DC converter and a power conservation circuit, wherein the DC-to-DC converter is operably coupled to convert a battery voltage into a supply voltage that supplies at least one of: the processing core, the digital interface circuitry, and the mixed signal circuitry, wherein the power conservation circuit includes:

processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;

determine an operational temperature associated with the analog variation parameter;

determine a digital variation parameter representative of a processing speed of the integrated circuit; and

determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature and the digital variation parameter; and

adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal to optimize power consumption of the integrated circuit~~, such that power consumption of the integrated circuit is optimized~~.

17. (Cancelled)

18. (Currently Amended) The comprehensive system-on-a-chip of ~~claim 17~~ Claim 16, wherein the memory further stores operational instructions that cause the processing module to:

update the regulation adjustment by repeating at least one of the determination of the operational temperature and the determination of the analog variation parameter.

19. (Original) The comprehensive system-on-a-chip of claim 16, wherein the memory further stores operational instructions that cause the processing module to measure the processing speed by:

enabling a function to be performed by the at least a portion of the comprehensive system-on-a-chip;

counting at least one of a number of cycles of a known clock during the performing of function by the at least a portion of the integrated circuit and a number of repetitions of the function during a cycle of the known clock to produce a count value; and

equating the count value to the processing speed.

20. (Original) The comprehensive system-on-a-chip of claim 18, wherein the memory further stores operational instructions that cause the processing module to adjust of the supply voltage by:

determining the digital variation parameter as a ratio between the measured processing speed and the critical processing speed; and

adjusting the supply voltage based on an operational sufficiency of either the digital variation parameter or the analog variation parameter with respect to the operational temperature.

21. (Currently Amended) A method for increasing power supply efficiency of an integrated circuit, comprising:

determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit; and

determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter; and

adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal to optimize power consumption of the integrated circuit~~, such that power consumption of the integrated circuit is optimized~~.

22. (Currently Amended) The method of ~~claim 21~~ Claim 21, wherein the determining the adjustment signal further comprises:

determining an operational temperature associated with the analog variation parameter; and

determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature, such that power consumption of the integrated circuit is optimized.

23. (Original) The method of Claim 22 further comprises:

determining a digital variation parameter; and

determining the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature.

24. (Original) The method of Claim 23 wherein the determining the adjustment signal comprises:

determining a first adjustment signal based on the analog variation parameter;

determining a second adjustment signal based on the digital variation parameter;

comparing the first adjustment signal to the second adjustment signal; and

when the first adjustment signal compares favorably with the second adjustment signal, selecting the first adjustment signal as the adjustment signal, else the second adjustment signal as the adjustment signal.

REMARKS

Claims 1-24 are pending in the application.

Claims 1-24 had been rejected.

Claims 1, 3, 4, 9, 11, 12, 16, 18, 21 and 22 have been amended.

Claims 2, 10, and 17 have been cancelled without prejudice.

Reconsideration of the Claims is respectfully requested.

1. Rejection under 35 U.S.C. § 101

Claims 1-24 were rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1, 9, 21, and 22 were amended accordingly to overcome the rejection.

2. Allowed and Allowable Subject Matter

Applicant notes with appreciation the allowability of its Claims 16-20 upon being rewritten to overcome the rejection under 35 U.S.C. § 101. Claim 16 has been amended accordingly. Claim 17 has been cancelled without prejudice.

The Office Action noted that Claims 2-8, 10-15, and 23-24 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant notes with appreciation this indication of allowability.

Claim 1 has been amended to incorporate Claim 2. Claim 9 has been amended to incorporate Claim 10. Claim 21 has been amended to clarify Applicant's claimed invention by adding the limitation of "adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal to optimize power consumption of the integrated circuit." Applicant respectfully submits that these amendments overcome the objection.

3. Conclusion

As a result of the foregoing, the Applicant respectfully submits that Claims 1, 3-9, 11-16, and 18-24, in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ksmith@texaspatents.com.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126.

Respectfully submitted,

Date: December 6, 2006

/Kevin L. Smith/

Kevin L. Smith, Reg. No. 38,620
Attorney for Applicant

Garlick Harrison & Markison
P.O. Box 160727
Austin, Texas 78716-0727
(972) 772-8836/office
(972) 772-5033/facsimile

Electronic Acknowledgement Receipt

EFS ID:	1357533
Application Number:	11078150
International Application Number:	
Confirmation Number:	7355
Title of Invention:	Power optimization of a mixed-signal system on an integrated circuit
First Named Inventor/Applicant Name:	Marcus W. May
Customer Number:	34399
Filer:	Kevin Lee Smith
Filer Authorized By:	
Attorney Docket Number:	SIG000124
Receipt Date:	06-DEC-2006
Filing Date:	11-MAR-2005
Time Stamp:	22:30:35
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1		SIG000124_Rsp_Non_Final_OA_EFS.pdf	140724	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment - After Non-Final Rejection	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	10
Warnings:			
Information:			
	Total Files Size (in bytes):	140724	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/078,150	03/11/2005	Marcus W. May	SIG000124	7355

34399 7590 09/06/2006

GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
WALLING, MEAGAN S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	11/078,150	MAY ET AL.	
	Examiner	Art Unit	
	Meagan S. Walling	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. Claims 1-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention must produce a "useful, concrete, and tangible result." *State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02.

Claims 1-24 do not produce a tangible result. In order to overcome the rejection, claim language should be added that includes outputting, displaying, storing, or otherwise conveying the result of the previous method steps.

For the official interim guidelines for examination of patent applications for patent subject matter eligibility, please see the US Patent and Trademark Organization Official Gazette Notices at http://www.uspto.gov/web/offices/com/sol/og/2005/week47/patgupa.htm.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 9, 21, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker et al. (US 5,563,928).

Regarding claim 1, Rostoker et al. teaches determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit (column 1, lines 25-33); determining an operational temperature associated with the analog variation parameter (column 1, lines 34-38); and determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to eh operational temperature, such that power consumption of the integrated circuit is optimized (column 2, lines 14-17).

Regarding claim 9, Rostoker et al. teaches a processing module (1002); and a memory (1004) operably coupled to the processing module, wherein the memory stores operation instructions that cause the processing module to: determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit (column 1, lines 25-33); determine an operational temperature associated with the analog variation parameter (column 1, lines 34-38); and determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to eh operational temperature, such that power consumption of the integrated circuit is optimized (column 2, lines 14-17).

Regarding claim 21, Rostoker et al. teaches determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit (column 1, lines 25-33); and determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter such that power consumption of the integrated circuit is optimized (column 2, lines 14-17).

Regarding claim 22, Rostoker et al. teaches determining an operational temperature associated with the analog variation parameter (column 1, lines 34-38); and determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to eh operational temperature such that the power consumption of the integrated circuit is optimized (column 2, lines 14-17).

Allowable Subject Matter

3. Claims 2-8, 10-15 and 23-24 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and to overcome the 35 U.S.C. 101 rejection.

Please see the previous office action for an indication of allowable subject matter.

4. Claims 16-20 would be allowable if rewritten to overcome the 35 U.S.C. 101 rejection.

Please see the previous office action for an indication of allowable subject matter.

Response to Arguments

Applicant's arguments filed 6/20/06 have been fully considered but they are not persuasive.

Aside from restating the claims, the only argument seems to be a single statement on page 9 of the remarks that states, "...Rostoker appears to control temperature and voltage parameters of its integrated circuit by power reduction, instead of monitoring the parameters for optimizing power consumption."

Although Rostoker teaches, in column 2, lines 10-13, that operating parameters *may* be adjusted (emphasis added), Rostoker further teaches, in column 2, lines 14-19, that an object of the invention is to determine optimal performance parameters over a wide range of temperatures and voltages encountered.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Meagan S. Walling whose telephone number is (571) 272-2283. The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

msw

John Barlow
Supervisory Patent Examiner
Technology Center 2800

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
11/078,150	MAY ET AL.	
Examiner	**Art Unit**	
Meagan S. Walling	2863	

SEARCHED			
Class	Subclass	Date	Examiner
702	130 117 121 124 60 64	9/1/2006	MW
377	19 20		
438	14 17 18		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search	9/1/2006	MW
702/130, 117 and word search		
377/19 and word search		
438/17 and word search		

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
11/078,150	MAY ET AL.
Examiner	**Art Unit**
Meagan S. Walling	2863

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	9/1/06
	1	√
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	variation near parameter same ((integrated near circuit) or ic) and temperature with variation near parameter and (adjust$3 adjustment) with signal with power with voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/13 17:13
S2	2	variation near parameter same ((integrated near circuit) or ic) and temperature with variation near parameter and (adjust$3 adjustment) with signal same power same voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/13 17:13
S3	1	(optimiz$3 optimization) with power with (ic or (integreated near circuit)) and variation with parameter same temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 11:52
S4	1	(optimiz$3 optimization) with power with (ic or (integreated near circuit)) and variation with parameter same temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 11:52
S5	0	S4 and signal	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 11:53
S6	12	power with consumption with optimiz$3 and (ic or (integrated near circuit)) and variation near parameter	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:29
S7	4	power with consumption with optimiz$3 and (ic or (integrated near circuit)) and variation near parameter and temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 11:54
S8	1980714	variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power adn voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 12:07
S9	41	variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S10	22	variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31

EAST Search History

S11	7	variation near parameter same temperature and (ic (integrated near circuit)) and optimiz$3 with power same voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 12:09
S12	3	variation near parameter same temperature and (ic (integrated near circuit)) and optimiz$3 with power same voltage and dc	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 12:09
S13	330	702/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S14	867	702/117.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S15	684	702/130.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S16	482	377/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S17	3894	438/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S18	0	S14 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S19	0	S15 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S20	0	S16 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S21	2	S17 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
S22	0	S14 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31

EAST Search History

S23	0	S15 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31
S24	0	S16 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31
S25	1	S17 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31

DOCKET NO. SIG000124

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Marcus W. May
Serial No.	11/078,150
Filed:	March 11, 2005
For:	Power Optimization of a Mixed-Signal System on an Integrated Circuit
Group No.:	2863
Examiner:	Walling, Meagan S.

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICIAL ACTION UNDER 37 C.F.R. § 1.111

Sir:

Responsive to the Official Action having a mailed date of March 20, 2006, Applicant hereby makes the following arguments and remarks. As such, reconsideration of the action and allowance of the present application are respectfully requested and are believed to be appropriate in view of the following:

Amendment to the Specification – N/A

Amendment to the Claims begins on page 2 of this paper.

Amendment to the Drawings – N/A

Remarks begin on page 9 of this paper.

IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Original) A method for power supply optimization of an integrated circuit, comprising:

determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;

determining an operational temperature associated with the analog variation parameter; and

determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature, such that power consumption of the integrated circuit is optimized.

2. (Original) The method Claim 1 further comprises:

adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal.

3. (Original) The method of Claim 2 further comprises:

updating the adjustment signal by repeating at least one of the determination of the operational temperature and determining the adjustment signal.

4. (Original) The method of Claim 1 further comprises:

determining a digital variation parameter; and

determining the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature.

5. (Original) The method of Claim 4 wherein the determining the adjustment signal comprises:

determining a first adjustment signal based on the analog variation parameter;

determining a second adjustment signal based on the digital variation parameter;

comparing the first adjustment signal to the second adjustment signal; and

when the first adjustment signal compares favorably with the second adjustment signal, selecting the first adjustment signal as the adjustment signal, else the second adjustment signal as the adjustment signal.

6. (Original) The method Claim 4, wherein determining a digital variation parameter comprises:

measuring processing speed of at least a portion of an integrated circuit to produce measured processing speed;

comparing the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit; and

when the measured processing speed compares favorably to the critical processing speed, correspondingly set a value of the digital variation parameter.

7. (Original) The method of Claim 4 further comprises:

adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal.

8. (Original) The method of Claim 7 further comprises:

updating the adjustment signal by repeating at least one of the determination of the operational temperature, the determination of the analog variation parameter, and of the digital variation parameter

9. (Original) An apparatus for increasing power supply efficiency of an integrated circuit comprises:

a processing module; and

a memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;

determine an operational temperature associated with the analog variation parameter; and

determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter and the operational temperature, such that power consumption of the integrated circuit is optimized.

10. (Original) The apparatus of claim 9, wherein the memory further stores operational instructions that cause the processing module to:

adjust a regulation signal of a DC-to-DC converter based on the adjustment signal.

11. (Original) The method of Claim 10, wherein the memory further stores operational instructions that cause the processing module to:

update the adjustment signal by repeating at least one of the determination of the operational temperature and determine the analog variation parameter.

12. (Original) The apparatus of claim 9, wherein the memory further stores operational instructions that cause the processing module to:

determine a digital variation parameter; and

determine the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature.

13. (Original) The apparatus of claim 12, wherein the memory further stores operational instructions that cause the processing module to determine the digital variation parameter by:

measuring a processing speed of at least a portion of an integrated circuit to produce measured processing speed;

comparing the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit; and

when the measured processing speed compares favorably to the critical processing speed, set a corresponding value of the digital variation parameter.

14. (Original) The apparatus of claim 12, wherein the memory further stores operational instructions that cause the processing module to:

adjust a regulation signal of a DC-to-DC converter based on the adjustment signal.

15. (Original) The apparatus of claim 13, wherein the memory further stores operational instructions that cause the processing module to:

determine a first adjustment signal based on the analog variation parameter;

determine a second adjustment signal based on the digital variation parameter;

compare the first adjustment signal to the second adjustment signal; and

when the first adjustment signal compares favorably with the second adjustment signal, selecting the first adjustment signal as the adjustment signal, else selecting the second adjustment signal as the adjustment signal.

16. (Original) A comprehensive system-on-a-chip comprises:

a processing core operably coupled to process input digital data and produce therefrom output digital data;

digital interface circuitry operably coupled to provide the input digital data to the processing core and to receive the output digital data from the processing core;

mixed signal circuitry operably coupled to convert input analog signals into the input digital data and to convert the output digital data into output analog signals; and

battery optimization circuitry that includes a DC-to-DC converter and a power conservation circuit, wherein the DC-to-DC converter is operably coupled to convert a battery voltage into a supply voltage that supplies at least one of: the processing core, the digital interface circuitry, and the mixed signal circuitry, wherein the power conservation circuit includes:

processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;

determine an operational temperature associated with the analog variation parameter;

determine a digital variation parameter representative of a processing speed of the integrated circuit; and

determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature and the digital variation parameter, such that power consumption of the integrated circuit is optimized.

17. (Original) The comprehensive system-on-a-chip of claim 16, wherein the memory further stores operational instructions that cause the processing module to:

adjust a regulation signal of a DC-to-DC converter based on the adjustment signal.

18. (Original) The comprehensive system-on-a-chip of claim 17, wherein the memory further stores operational instructions that cause the processing module to:

update the regulation adjustment by repeating at least one of the determination of the operational temperature and the determination of the analog variation parameter.

19. (Original) The comprehensive system-on-a-chip of claim 16, wherein the memory further stores operational instructions that cause the processing module to measure the processing speed by:

enabling a function to be performed by the at least a portion of the comprehensive system-on-a-chip;

counting at least one of a number of cycles of a known clock during the performing of function by the at least a portion of the integrated circuit and a number of repetitions of the function during a cycle of the known clock to produce a count value; and

equating the count value to the processing speed.

20. (Original) The comprehensive system-on-a-chip of claim 18, wherein the memory further stores operational instructions that cause the processing module to adjust of the supply voltage by:

determining the digital variation parameter as a ratio between the measured processing speed and the critical processing speed; and

adjusting the supply voltage based on an operational sufficiency of either the digital variation parameter or the analog variation parameter with respect to the operational temperature.

21. (Original) A method for increasing power supply efficiency of an integrated circuit, comprising:

determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit; and

determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter such that power consumption of the integrated circuit is optimized.

22. (Original) The method of claim 21 further comprises:

determining an operational temperature associated with the analog variation parameter; and

determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature, such that power consumption of the integrated circuit is optimized.

23. (Original) The method of Claim 22 further comprises:

determining a digital variation parameter; and

determining the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature.

24. (Original) The method of Claim 23 wherein the determining the adjustment signal comprises:

determining a first adjustment signal based on the analog variation parameter;

determining a second adjustment signal based on the digital variation parameter;

comparing the first adjustment signal to the second adjustment signal; and

when the first adjustment signal compares favorably with the second adjustment signal, selecting the first adjustment signal as the adjustment signal, else the second adjustment signal as the adjustment signal.

REMARKS

Claims 1-24 are pending in the application.

Claims 1, 9, 21, and 22 have been rejected.

Claims 16-20 are allowed.

Claims 2-8, 10-15, 23 and 24 have been objected to as depending from a rejected base claim, but would be allowable if rewritten accordingly.

Reconsideration of the Claims is respectfully requested.

1. Rejection under 35 U.S.C. § 102

Claims 1, 9, 21, and 22 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,563,928 to Rostoker et al. ("Rostoker").

For establishing anticipation, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. . . . The identical invention must be shown in as complete detail as is contained in the . . . claim." MPEP § 2131 at p. 2100-73 (8th ed., rev. 3, August 2005) (citations omitted).

Rostoker relates to "a method and apparatus for optimizing the performance of the digital systems by determining the optimal speed-power parameters for the components of the digital systems." (Rostoker Col. 1:18-22). Under the heading "Digital System" of Rostoker, "[w]hen a system requires a certain operating speed, the voltage and/or temperature parameters of the integrated circuits may be adjusted so as to realize a minimum appropriate relaxation oscillator frequency [parameter] for each integrated circuit. Conversely, when the integrated circuits of the system [have] much faster [clock rates] than necessary for desired operation, the voltage to these integrated circuits may be lowered to reduce power consumption of the system." (Rostoker Col. 12:56-63). Also, "[t]emperature and voltage [parameters] may be controlled . . . (Rostoker Col. 12:64-66; *see also, e.g.*, Col. 11:34-42 (a set point signal for temperature control); Claim 21). In other words, Rostoker appears to control temperature and voltage parameters of its integrated circuits by power reduction, instead of monitoring the parameters for optimizing power consumption.

In contrast, Applicant's Independent Claim 1 recites, *inter alia*, a "method for power supply optimization of an integrated circuit, comprising: determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit; . . .

and determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature, such that power consumption of the integrated circuit is optimized." (emphasis added).

Also, the method of Applicant's Independent Claim 20 recites, *inter alia*, a "method for increasing power supply efficiency of an integrated circuit, comprising: determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit; and determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter such that power consumption of the integrated circuit is optimized." (emphasis added).

Applicant respectfully submits that Rostoker does not provide each and every element as set forth in Applicant's method claims 1 and 20.

Also, the apparatus of Applicant's Independent Claim 9 recites, *inter alia*, an "apparatus for increasing power supply efficiency of an integrated circuit comprises: a processing module; and a memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to: determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit; . . . determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter and the operational temperature, such that power consumption of the integrated circuit is optimized." (emphasis added).

Applicant respectfully submits that Rostoker does not provide each and every element as set forth in Applicant's apparatus of Independent Claim 9.

Accordingly, Applicant respectfully submits that each and every element as set forth in Applicant's claimed invention of its Independent Claim 1, Independent Claim 9, and Independent Claim 21 and Claim 22 that depends therefrom, is not found in Rostoker. Applicant respectfully requests that the rejection to these claims be withdrawn.

2. Allowed and Allowable Subject Matter

Applicant notes with appreciation the allowance of its Claims 16-20.

The Office Action noted that Claims 2-8, 10-15, and 23-24 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant notes with appreciation this indication of allowability.

3. Conclusion

As a result of the foregoing, the Applicant respectfully submits that Claims 1-15 and 21-24, in addition to Claims 16-20, in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ksmith@texaspatents.com.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126.

Respectfully submitted,

Date: June 20, 2006

/Kevin L. Smith/

Kevin L. Smith, Reg. No. 38,620
Attorney for Applicant

Garlick Harrison & Markison
P.O. Box 160727
Austin, Texas 78716-0727
(972) 772-8836/office
(972) 772-5033/facsimile

Electronic Acknowledgement Receipt

EFS ID:	1085658
Application Number:	11078150
Confirmation Number:	7355
Title of Invention:	Power optimization of a mixed-signal system on an integrated circuit
First Named Inventor:	Marcus W. May
Customer Number:	34399
Filer:	Kevin Lee Smith
Filer Authorized By:	
Attorney Docket Number:	SIG000124
Receipt Date:	20-JUN-2006
Filing Date:	11-MAR-2005
Time Stamp:	18:41:58
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		Rsp_Non_Final_OA_SIG000124_EFS.pdf	145559	yes	11

	Multipart Description		
	Doc Desc	Start	End
	Amendment - After Non-Final Rejection	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	11
Warnings:			
Information:			
	Total Files Size (in bytes):	145559	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 11078150

APPLICATION AS FILED – PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
FOR							
BASIC FEE (37 CFR 1.16(a), (b), or (c))			150			300	
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =		x 25		OR	x 50	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =		x 100			x 200	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s)						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	6-20-06									
	Total (37 CFR 1.16(i))	* 24	minus	** 24	=	x .25		OR	x .50	
	Independent (37 CFR 1.16(h))	* 4	minus	*** 4	=	x .100		OR	x .200	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADDIT. FEE			TOTAL ADDIT. FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT B										
	Total (37 CFR 1.16(i))	*	minus	**	=	x		OR	x	
	Independent (37 CFR 1.16(h))	*	minus	***	=	x		OR	x	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADDIT. FEE			TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/078,150	03/11/2005	Marcus W. May	SIG000124	7355

34399 7590 03/20/2006

GARLICK HARRISON & MARKISON LLP
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
WALLING, MEAGAN S	
ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	11/078,150	MAY ET AL.
	Examiner	Art Unit
	Meagan S. Walling	2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-20* is/are allowed.

6)☒ Claim(s) *1,9,21 and 22* is/are rejected.

7)☒ Claim(s) *2-8,10-15,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 9, 21, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker et al. (US 5,563,928).

Regarding claim 1, Rostoker et al. teaches determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit (column 1, lines 25-33); determining an operational temperature associated with the analog variation parameter (column 1, lines 34-38); and determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to eh operational temperature, such that power consumption of the integrated circuit is optimized (column 2, lines 14-17).

Regarding claim 9, Rostoker et al. teaches a processing module (1002); and a memory (1004) operably coupled to the processing module, wherein the memory stores operation instructions that cause the processing module to: determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit (column 1, lines 25-33); determine an operational temperature associated with the analog variation parameter (column 1, lines 34-38); and determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect

to eh operational temperature, such that power consumption of the integrated circuit is optimized (column 2, lines 14-17).

Regarding claim 21, Rostoker et al. teaches determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit (column 1, lines 25-33); and determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter such that power consumption of the integrated circuit is optimized (column 2, lines 14-17).

Regarding claim 22, Rostoker et al. teaches determining an operational temperature associated with the analog variation parameter (column 1, lines 34-38); and determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to eh operational temperature such that the power consumption of the integrated circuit is optimized (column 2, lines 14-17).

Allowable Subject Matter

2. Claims 2-8, 10-15 and 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for the indication of allowability of claims 2 and 10 is the inclusion of the limitation of adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claims 4, 12, and 22 is the inclusion of the limitation of determining a digital variation parameter; and determining the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

3. Claims 16-20 are allowed.

The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claim 16 is the inclusion of the limitation of a processing core operably coupled to process input digital data and produce therefrom output digital data', digital interface circuitry operably coupled to provide the input digital data to the processing core and to receive the output digital data from the processing core; mixed signal circuitry operably coupled to convert input analog signals into the input digital data and to convert the output digital data into output analog signals; and battery optimization circuitry that includes a DC-to-DC converter and a power conservation circuit, wherein the DC-to-DC converter is operably coupled to convert a battery voltage into a supply voltage that supplies at least one of: the processing core, the digital interface circuitry, and the mixed signal circuitry, wherein the power conservation circuit includes: processing module; and memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit; determine an operational temperature associated with the analog variation parameter; determine a digital variation

parameter representative of a processing speed of the integrated circuit; and determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature and the digital variation parameter, such that power consumption of the integrated circuit is optimized. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

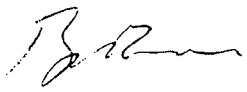
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Meagan S. Walling whose telephone number is (571) 272-2283. The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

msw

BRYAN BUI
PRIMARY EXAMINER



Notice of References Cited	Application/Control No. 11/078,150	Applicant(s)/Patent Under Reexamination MAY ET AL.	
	Examiner Meagan S. Walling	Art Unit 2863	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,563,928	10-1996	Rostoker et al.	377/20
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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CONFIRMATION NO. 7355

Bib Data Sheet

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/078,150	03/11/2005 RULE	702	2863	SIG000124

APPLICANTS

Marcus W. May, Austin, TX;

Matthew D. Felder, Austin, TX;

** CONTINUING DATA **********

none MW

** FOREIGN APPLICATIONS **********

none MW

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 04/07/2005

		STATE OR	SHEETS	TOTAL	INDEPENDENT
Foreign Priority claimed	☐ yes ☒ no	COUNTRY	DRAWING	CLAIMS	CLAIMS
35 USC 119 (a-d) conditions met	☐ yes ☒ no ☐ Met after Allowance	TX	10	24	4
Verified and Acknowledged	Examiner's Signature / Initials				

ADDRESS
34399
GARLICK HARRISON & MARKISON LLP
P.O. BOX 160727
AUSTIN , TX
78716-0727

TITLE
Power optimization of a mixed-signal system on an integrated circuit

FILING FEE	FEES: Authority has been given in Paper	☐ All Fees
RECEIVED 700	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue)

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
11/078,150	MAY ET AL.	
Examiner	Art Unit	
Meagan S. Walling	2863	

SEARCHED			
Class	Subclass	Date	Examiner
702	130 117 121 124 60 64	3/14/2006	MW
377	19 20		
438	14 17 18		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search	3/14/2006	MW
702/130, 117 and word search		
377/19 and word search		
438/17 and word search		

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	330	702/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
L2	867	702/117.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
L3	684	702/130.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
L4	482	377/19.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
L5	3894	438/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
L6	0	2 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
L7	0	3 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
L8	0	4 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
L9	2	5 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30
L10	0	2 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31
L11	0	3 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31

EAST Search History

L12	0	4 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31
L13	1	5 and (variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31
S1	0	variation near parameter same ((integrated near circuit) or ic) and temperature with variation near parameter and (adjust$3 adjustment) with signal with power with voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/13 17:13
S2	2	variation near parameter same ((integrated near circuit) or ic) and temperature with variation near parameter and (adjust$3 adjustment) with signal same power same voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/13 17:13
S3	1	(optimiz$3 optimization) with power with (ic or (integreated near circuit)) and variation with parameter same temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 11:52
S4	1	(optimiz$3 optimization) with power with (ic or (integreated near circuit)) and variation with parameter same temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 11:52
S5	0	S4 and signal	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 11:53
S6	12	power with consumption with optimiz$3 and (ic or (integrated near circuit)) and variation near parameter	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:29
S7	4	power with consumption with optimiz$3 and (ic or (integrated near circuit)) and variation near parameter and temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 11:54
S8	1980714	variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power adn voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 12:07
S9	41	variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power and voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:30

EAST Search History

S10	22	variation near parameter same temperature and (ic (integrated circuit)) and optimiz$3 with power same voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 14:31
S11	7	variation near parameter same temperature and (ic (integrated near circuit)) and optimiz$3 with power same voltage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 12:09
S12	3	variation near parameter same temperature and (ic (integrated near circuit)) and optimiz$3 with power same voltage and dc	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/03/14 12:09

PTO/SB/05 (09-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	SIG000124
First Inventor	Marcus W. May
Title	Power Optimization of Mixed-Signal System on an Integrated Circuit
Express Mail Label No.	EV725284205US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [✓] **Fee Transmittal Form** (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. [✓] **Applicant claims small entity status.** See 37 CFR 1.27.
3. [✓] **Specification** [*Total Pages* 36]
   Both the claims and abstract must start on a new page
   (For information on the preferred arrangement, see MPEP 608.01(a))
4. [✓] **Drawing(s)** (*35 U.S.C. 113*) [*Total Sheets* 10]
5. **Oath or Declaration** [*Total Sheets* 2]
   a. [✓] Newly executed (original or copy)
   b. [ ] A copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [ ] **Application Data Sheet.** See 37 CFR 1.76
7. [ ] **CD-ROM or CD-R** in duplicate, large table or Computer Program *(Appendix)*
   [ ] Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
   (if applicable, items a. – c. are required)
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
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ADDRESS TO: **P.O. Box 1450, Alexandria VA 22313-1450**

ACCOMPANYING APPLICATION PARTS

9. [✓] **Assignment Papers** (cover sheet & document(s))
   Name of Assignee _____
10. [ ] **37 CFR 3.73(b) Statement** *(when there is an assignee)* [✓] **Power of Attorney**
11. [ ] **English Translation Document** *(if applicable)*
12. [ ] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
13. [ ] **Preliminary Amendment**
14. [✓] **Return Receipt Postcard** (MPEP 503)
    (Should be specifically itemized)
15. [ ] **Certified Copy of Priority Document(s)**
    (if foreign priority is claimed)
16. [ ] **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
17. [ ] Other: _____

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: .....

Prior application information: *Examiner* _____ *Art Unit:* _____

19. CORRESPONDENCE ADDRESS

[✓] The address associated with Customer Number: 34,399 *OR* [ ] Correspondence address below

Name	Kevin L. Smith				
Address	P. O. Box 160727				
City	Austin	State	TX	Zip Code	78716
Country	US	Telephone	972-772-8836	Fax	972-772-5033

Signature	/Kevin L. Smith/	Date	3/11/05
Name (Print/Type)	Kevin L. Smith	Registration No. (Attorney/Agent)	38,620

PTO/SB/17 (12-04v2)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($)	740.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Marcus W. May
Examiner Name	
Art Unit	
Attorney Docket No.	SIG000124

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-1415 Deposit Account Name: Sigmatel, Inc.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	500.00
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
24 - 20 or HP =	4	x 25	= 100.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
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HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims Fee ($)	Fee Paid ($)
0	0

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
46 - 100 =	_____	/ 50 = _____ (round up to a whole number)	x 0	= 0

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Assignment Recordation Fee	40.00

SUBMITTED BY

Signature	/Kevin L. Smith/	Registration No. (Attorney/Agent) 38,620	Telephone 972-772-8836
Name (Print/Type)	Kevin L. Smith		Date 3/11/05

PTO/SB/05 (09-04)
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U.S. Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	SIG000124
First Inventor	Marcus W. May
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   Name of Assignee
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11. [ ] **English Translation Document** *(if applicable)*
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    [ ] Copies of citations attached
13. [ ] **Preliminary Amendment**
14. [✓] **Return Receipt Postcard** (MPEP 503)
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15. [ ] **Certified Copy of Priority Document(s)**
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16. [ ] **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
17. [ ] Other:

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First Named Inventor	Marcus W. May
Examiner Name	
Art Unit	
Attorney Docket No.	SIG000124

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☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-1415 Deposit Account Name: Sigmatel, Inc.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

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1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
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Plant	200	100	300	150	160	80	
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Multiple Dependent Claims Fee ($)	Fee Paid ($)
0	0

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Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
46 - 100 =		/ 50 = (round up to a whole number) x	0	= 0

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Assignment Recordation Fee	40.00

SUBMITTED BY

Signature	/Kevin L. Smith/	Registration No. (Attorney/Agent) 38,620	Telephone 972-772-8836
Name (Print/Type)	Kevin L. Smith		Date 3/11/05

POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT

TECHNICAL FIELD

[0001] This invention relates generally to portable electronic equipment and more particularly to a sensing digital and analog parameters of an integrated circuit to provide power supply optimization.

BACKGROUND

[0002] As is known, integrated circuits are used in a wide variety of electronic equipment, including portable, or handheld, devices. Such handheld devices include personal digital assistants (PDA), CD players, MP3 players, DVD players, AM/FM radio, a pager, cellular telephones, computer memory extension (commonly referred to as a thumb drive), etc. These handheld devices include one or more integrated circuits to provide the functionality of the device. For example, a thumb drive may include an integrated circuit for interfacing with a computer (for example, personal computer, laptop, server, workstation, etc.) via one of the ports of the computer (for example, Universal Serial Bus, parallel port, etc.) and at least one other memory integrated circuit (for example, flash memory). As such, when the thumb drive is coupled to a computer, data can be read from and written to the memory of the thumb drive. Accordingly, a user may store personalized information (for example, presentations, Internet access account information, etc.) on his/her thumb drive and use any computer to access the information.

[0003] As another example, an MP3 player may include multiple integrated circuits to support the storage and playback of digitally formatted audio (that is, formatted in accordance with the MP3 specification). As is known, one integrated circuit may be used for interfacing with a computer, another integrated circuit for generating a power supply voltage, another for processing the storage and/or playback of the digitally formatted audio data, and still another for rendering the playback of the digitally formatted audio.

[0004] Integrated circuit technology has led to a plethora of handheld devices; however, to be "wired" in today's electronic world, multiple handheld devices would be needed.

For example, one may own a cellular telephone for cellular telephone service, a PDA for scheduling, address book, etc., one or more thumb drives for extended memory functionality, an MP3 player for storage and/or playback of digitally recorded music, a radio, etc. Thus, even though a single handheld device may be relatively small, carrying multiple handheld devices on one's person can become quite burdensome.

[0005] Such handheld devices use a battery (or batteries) to supply power to the circuitry of the device. The greater the circuit power consumption, the shorter the battery life (that is, the length of time a device can be operated before having to replace or charge the battery).

[0006] With the goal of extending battery lifespan for portable devices, various techniques had been used. One technique has been to turn off circuitry that is not needed to support the present function and to put the device in a "sleep" mode when the entire device is not in use.

[0007] Another technique is related to improvements in integrated circuit fabrication that allows for smaller devices to be developed and to be operated at lower voltages, thus consuming less power. For example, 0.18 micron Complementary Metal Oxide Semiconductor ("CMOS") integrated circuit technology is currently the most accepted process, which uses supply voltages of 1.8 volts. Several years ago, however, 0.35 micron and 0.50 micron CMOS integrated circuit technologies were the prevalent processes, which could use supply voltages of about 3.3 volts. In the near future, 0.10 and 0.13 micron CMOS integrated circuit technology will likely become the technology of choice because of lower supply voltages of about 1.0 volts.

[0008] While these design techniques worked to reduce power consumption generally, they had been designed assuming the worst-case operation of an integrated circuit. As such, integrated circuit circuits would be consuming more power than needed because the power reducing techniques were under a worst-case assumption and not individually optimized on a chip-by-chip basis.

[0009] Generally, digital components and analog components are operated under different processes, techniques, or parameters for their desired functional results. Because digital component operation is based on clock speed, and analog component operation is based on bias factors such as threshold voltage, different operational parameters or conditions may be more favorable for one over the other. For example, lower operational temperatures raise the threshold voltage level for analog components, affecting signal performance, while favorable for digital component operation. Conversely, higher operational temperatures lower the threshold voltage level for analog components, while slowing digital gate response for digital components. Accordingly, power consumption considerations for each type of component would differ.

[0010] Therefore, a need exists for an integrated circuit that provides multiple functions through mixed-signal operation and architectures for handheld devices with appropriate optimized power-consumption and with a minimal requirement of external components.

SUMMARY

[0011] Provided is a method and apparatus for conserving power of a system-on-a-chip having analog circuitry. An aspect is a method and apparatus for increasing the power supply efficiency of an integrated circuit, by determining an analog variation parameter that is representative of an integrated circuit fabrication process variance of the integrated circuit. An operational temperature is determined, where the operational temperature is associated with the analog variation parameter. With the analog variation parameter and the operational temperature, an adjustment signal is determined for a power supply level of the integrated circuit, such that power consumption of the integrated circuit is optimized.

[0012] A further aspect involves determining a digital variation parameter, and determining the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature. The digital variation parameter is determined by using a speed sensing technique, which begins by measuring the processing speed of at least a portion of an integrated circuit ("IC") to produce measured processing speed. The portion of the IC may be a test circuit, a critical path of the IC, and/or a replica of the critical path of the IC. The processing continues by comparing the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit. The processing then continues by adjusting supply voltage to the integrated circuit to reduce power consumption of the integrated circuit when the measured processing speed compares favorably to the critical processing speed.

[0013] With such a method and apparatus, power consumption is optimized on an IC-by-IC basis, as well as over time.

DESCRIPTION OF THE DRAWINGS

[0014] Figure 1 is a schematic block diagram of a multiple function battery operated device that includes a battery-optimized system-on-a-chip in accordance with the present invention;

[0015] Figure 2 is a schematic block diagram of another multiple function battery operated device that includes a battery-optimized system-on-a-chip in accordance with the present invention;

[0016] Figure 3 is a schematic block diagram of a power conserving circuit in accordance with the present invention;

[0017] Figure 4 is a graph of supply voltage versus transistor speed in accordance with the present invention;

[0018] Figure 5 is a graph of integrated circuit power consumption versus supply voltage in accordance with the present invention;

[0019] Figure 6 is a logic diagram of a method for conserving power in accordance with the digital circuitry in accordance with the present invention;

[0020] Figure 7a is a schematic of a process sensing channel in accordance with the present invention;

[0021] Figure 7b illustrates a graph that plots interrelationships of fabrication parameter corners versus headroom voltage in accordance with the present invention;

[0022] Figure 8 is a schematic block diagram of an analog power conservation circuit in accordance with the present invention;

[0023] Figure 9 is a schematic diagram of the operational temperature sensor in accordance with the present invention;

[0024] Figure 10 is a graph of current versus temperature that illustrates the operation of the operational temperature sensor of Figure 9;

[0025] Figure 11 is a schematic block diagram of a power conserving circuit having a first component for assessing power conservation for a digital circuit, and a second component for assessing power conservation for an analog circuit in accordance with the present invention; and

[0026] Figures 12a, 12b, and 12c are a logic diagram for a method for conserving power for a mixed signal integrated circuit in accordance with the present invention.

DETAILED DESCRIPTION

[0027] Figure 1 is a schematic block diagram of a multiple function battery operated device 10 that includes a battery-optimized system-on-a-chip 12, a battery 14, an inductor 16, a display 18, a connector 20, and an input device 22. The multiple function battery operated device 10 may also be referred to as a handheld device. The connector 20 provides coupling between the battery-optimized system-on-a-chip 12 and external sources 34, which may be a host computer 36, a video decoder 38, a memory stick 40, a wireless modem 42, a camcorder image sensor 44. The battery-optimized system-on-a-chip 12 includes a multimedia module 24, a high-speed interface 28, a processing module 30, on-chip memory 32, and an on-chip DC-to-DC converter 26. In general, the multiple function battery operated device 10 may be, but is not limited to, an MP3 player/recorder, a thumb drive memory extension, a digital camera, a digital camcorder, a DVD player/recorder, video conferencing device, a personal digital assistant ("PDA"), a radio, a television, and/or a CD player/recorder.

[0028] The DC-to-DC converter 26 is operably coupled to the battery 14 and inductor 16 to produce at least one supply voltage (V_{DD}). In general, the DC-to-DC converter may be a buck converter, a boost converter, a fly-back converter, a half bridge converter, and/or a full bridge converter. Note that the DC-to-DC converter can also be an inductor-less configuration including a linear regulator and/or a switched-capacitor regulator. In one embodiment, the DC-to-DC converter is a boost converter that includes a sink transistor, at least one load transistor, and regulation circuitry. The regulation circuitry monitors the supply voltage (V_{DD}) with respect to a reference voltage and produces therefrom a regulation signal. The regulation signal, in one phase, enables the sink transistor to build up energy in the inductor and, in another phase, enables the load transistor to transfer the energy of the inductor to the supply voltage. The DC-to-DC converter 26 may be constructed in accordance with the teaching of U.S. Patent 6,204,651, entitled METHOD AND APPARATUS FOR REGULATING A DC VOLTAGE, which is hereby incorporated by reference, and provides the supply voltage the processing module 30, the on-chip memory 32, the high-speed interface 28, and/or the multimedia module 24. The

DC-to-DC converter 26 may also provide the supply voltage off-chip to power the display 18 and/or the input device 22.

[0029] The high-speed interface 28 is operably coupled to bus 25 within the system-on-a-chip 12 and externally via the connector 20. As such, the high-speed interface 28, which may be a universal serial bus ("USB") interface, a serial-to-deserial interface, or parallel interface, provides connectivity between one or more external sources 34 and the system-on-a-chip 12. For example, the host computer 36, which may be a personal computer, laptop, workstation, etc., provides digitized audio (for example, an MP3 file, WMA - Windows Media Architecture-, MP3 PRO, Ogg Vorbis, AAC - Advanced Audio Coding, a CD file, etc.) and/or digitized video signals (for example, an MPEG (motion picture expert group) file, a JPEG (joint photographic expert group) file, a DVD file, a video graphics file, a text file, etc.) to the high-speed interface 28. The high-speed interface 28 converts the format of the received data into a generic format of the system-on-a-chip, which is based on the type of processing module 30 and/or the type of on-chip memory 32.

[0030] The high-speed interface then provides the generic formatted data to the processing module 30, the on-chip memory 32, and/or the multimedia module 24. For instance, the digitalized audio and/or video data may be stored in the on-chip memory 32 for later playback, where the processing module 30 controls the storing of the data via a multimedia application 46. Note that processing module 30 may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, micro-controller, digital signal processor, microcomputer, central processing unit, field programmable gate array, programmable logic device, state machine, logic circuitry, analog circuitry, digital circuitry, and/or any device that manipulates signals (analog and/or digital) based on operational instructions.

[0031] The on-chip memory 32 may be a single memory device or a plurality of memory devices. Such a memory device may be a read-only memory, random access memory, volatile memory, non-volatile memory, static memory, dynamic memory, flash memory, cache memory, and/or any device that stores digital information. Note that when the

processing module 30 implements one or more of its functions via a state machine, analog circuitry, digital circuitry, and/or logic circuitry, the memory storing the corresponding operational instructions may be embedded within, or external to, the circuitry comprising the state machine, analog circuitry, digital circuitry, and/or logic circuitry. The memory 32 stores, and the processing module 30 executes, operational instructions corresponding to multimedia applications 46 that include, but are not limited to audio playback, audio record, video playback, video record, storing text, displaying text, storing video graphics, file system transfer, and/or displaying video graphics.

[0032] The data that is stored in the on-chip memory 32 may be subsequently retrieved under the control of the processing module 30 while executing a multimedia application 46 to render the data audible and/or visible. In this instance, the processing module 30 causes the data to be retrieved from the on-chip memory 32 and to be provided to the multimedia module 24. The multimedia module 24 processes the data to produce rendered output data 52, which may include analog audio signals, digital audio signals, analog video signals, digital video signals, text, and/or video graphics, and provides the rendered output data 52 to the display 18. The display 18, which may be a headphone jack, a speaker or speakers, a Liquid Crystal Display ("LCD") video graphics display, an electro-luminance backlight video graphics display, etc., converts the rendered output data 52 into audible and/or visual information.

[0033] In other examples, the high-speed interface 28 may exchange audio data, video data, video graphics data, and/or text data with the video decoder 38, the memory stick 40, the wireless modem 42, and/or the camcorder image sensor 44. As such, the multiple function battery operated device 10 may function as a portable MP3 player/recorder, a personal DVD player/recorder, a personal CD player/recorder, etc.

[0034] The multimedia module 24 may also receive input signals 54 from the input device 22, which may be a microphone, a keypad, a video capture device (for example, a digital camera or a digital camcorder), etc. Such input signals 54 may be video signals, audio signals, video graphics signals, and/or text signals. Upon receiving the input signals 54, the multimedia module 24, in conjunction with the processing module 30

executing a multimedia application, converts the input signals 54 into the generic digital format of the system-on-a-chip for storage in the on-chip memory or for providing to an external source via the high-speed interface 28.

[0035] As one of average skill in the art will appreciate, the system-on-a-chip may include a memory interface operably coupled to the bus 25, which is coupled to a flash memory, or the like, to extend the memory of the battery operated device 10. As such, in one embodiment, all of the video, video graphics, text, and/or audio data is stored in the on-chip memory and in another embodiment, the video, video graphics, text, and/or audio data is at least partially stored off-chip in the external memory and retrieved when needed.

[0036] As one of average skill in the art will further appreciate, when the battery operated, or handheld, device 10 is not coupled to the host device, (that is, it is in a battery powered mode) the processing module 30 executes a multimedia application 46 to detect the disconnection and to place the handheld device in a battery operation mode. In the battery operation mode, the processing module 30 retrieves, and subsequently executes, a set of operational instructions from the on-chip memory 32 to support the battery operational mode. For example, the battery operational mode may correspond to MP3 file playback, digital dictaphone recording, MPEG file playback, JPEG file playback, text messaging display, cellular telephone functionality, and/or AM/FM radio reception.

[0037] As one of average skill in the art will still further appreciate, due to the comprehensiveness of the system-on-a-chip 12, the battery-operated device 10 requires minimal additional components, thus reducing cost and complexity of the resulting device 10. Further, by including battery-optimizing techniques, the system-on-a-chip optimally consumes power to fully extend the life of the battery.

[0038] Figure 2 is a schematic block diagram of another multiple function battery operated device 60 that includes a battery-optimized system-on-a-chip 62, a plurality of external memories 86, the battery 14, an external power source 68, a video and/or text

display 78, a headphone jack 74, speaker(s) 76, a microphone 84, a keypad 82, and a video capture device 80.

[0039] The battery-optimized system-on-a-chip 62 includes a plurality of high-speed interfaces 28, a plurality of memory interfaces 64, a plurality of processing modules 30, the DC-to-DC converter 26, a battery charger 66, the on-chip memory 32, the multimedia module 24, a power conserving circuit 250 providing an adjust signal 252 (which will be described in greater detail with reference to Figures 3 through 12), and an electro-luminance backlighting drive circuitry 70. The multimedia module 24 includes a capacitor-less headphone driver 72. The on-chip memory 32 includes random access memory ("RAM") 90 and read only memory ("ROM") 88.

[0040] The plurality of high-speed interfaces 28-1 through 28-*n* allow the system-on-a-chip 62 to be simultaneously coupled to multiple external sources 34. The high-speed interfaces may utilize the same or different interface protocols. For example, all of the high-speed interfaces 28 may utilize a USB interface protocol, an Ethernet interface protocol, a fire-wire interface protocol, a serial/deserial interface protocol, etc. Alternatively, each high-speed interface 28-1 through 28-*n* may use a different interface protocol. For instance, high-speed interface 28-1 may support a USB interface, high-speed interface 28-2 may support Ethernet, and high-speed interface 28-*n* may support a fire-wire interface. One or more of the processing modules 30-1 through 30-*n* coordinates and arbitrates the high-speed interfaces 28 access to the bus 25.

[0041] The plurality of memory interfaces 64-1 through 64-*n* allow the system-on-a-chip 62 to be coupled to a plurality of external memory devices 86-1 through 86-*n*. The external memory devices 86-1 through 86-*n* may be NAND flash memory devices, NOR flash memory devices, and/or any other type of random access memory devices or read only memory devices.

[0042] While executing one or more multimedia applications, one or more of the processing modules 30 coordinates the reading and/or writing of multimedia data to and from the external memory devices 86. For instance, one of the external memory devices 86 may store MP3 files for subsequent playback, another external memory device 86,

may store video files (for example, MPEG, JPEG, etc.) for subsequent playback, and another external memory device may store text and/or video graphics relating to operation of the device 60 and/or related to inputted data via the keypad 82, the video capture device 80, and/or one of the external sources 34 (*see* Figure 1).

[0043] Each of the external memory devices 86 may or may not be compliant with a memory interface standard. As such, the memory interfaces 64 include a flexible topology to accommodate the various types of external memory devices 86 that may be coupled to the system-on-a-chip 62. For a detailed discussion of the functionality of the memory interfaces 64 refer to U.S. patent application entitled FLEXIBLE MEMORY INTERFACE SYSTEM, having serial no. 10/865,585 and a filing date of June 10, 2004, which is hereby incorporated by reference.

[0044] The multimedia module 24 is operably coupled to receive input signals 54 from a microphone 84, a keypad 82, and/or a video capture device 80. The video capture device 80 may be a digital camera and/or a digital camcorder that supplies MPEG files, JPEG files, and/or other standardized format for still and/or motion digital images. The multimedia module 24 receives the digital video images from the video capture device 80 and either converts them into the generic format of the system-on-a-chip to produce generic video that are stored either in the on-chip memory 32 and/or in the external memory 86 or provides the digital video images to the bus 25 for storage in the on-chip memory 32 and/or in the external memory 86. One or more of the processing modules 30 coordinates the storing of the digital video images and whether the data will be converted to the generic format or not. The generic format may involve portioning packets of the video image into data words of a size corresponding to the bus width of the processing modules 30, storage word size of the on-chip or off-chip memory, and/or of the bus width of the bus 25.

[0045] The multimedia module 24 is also coupled to receive input signals 54 from the keypad 82. The keypad 82 may be a touch screen pad, a keyboard, voice recognition module, and/or any device that produces text messages. The multimedia module 24 receives the text messages from the keypad 82 and either processes them for display on

the video and/or text display 78 or for storage in the RAM 90 and/or in the external memory 86. The processing of the text message may involve routing it to the video and/or text display 78, converting it to the generic format for storing in the RAM 90 or the external memory 86, or rendering it for display (that is, converting text information into pixel information).

[0046] The multimedia module 24 is further coupled to receive input signals 54 from the microphone 84. The multimedia module 24 converts the analog audio input signals from the microphone 84 into digital audio input signals using an encoding scheme, such as pulse code modulation ("PCM"). The multimedia module 24 provides the digital audio signals to the RAM 90 and/or the external memory 86 for storage under the control of the processing module 30, which is executing an audio recording multimedia application 46. Accordingly, in this mode, the multiple function battery operated device 60 may function as a dictaphone.

[0047] The multimedia module 24 is operably coupled to provide analog audio signals to the speaker(s) 76 and/or to the headphone jack 74. The multimedia module 24 may generate the analog audio signals by performing a PCM decoding of digital audio signals stored in the on-chip memory 32 and/or stored in the external memory 86. The multimedia module 24 includes a driver, or multiple drivers, to supply the analog audio signals to the speaker(s) 76. The multimedia module 24 also includes the capacitor-less headphone driver 72 to supply the analog audio signals to the headphone jack. The capacitor-less headphone driver 72 reduces the number of external components by eliminating the need for coupling capacitors from the on-chip drivers to the headphone jack, wherein the coupling capacitors enabled level shifting of the analog audio signals from the driver level of 0.9-volts (for example, an alternating current ("AC") ground for the left channel and right channel drivers) to 0-volts for the headphones. By reducing the number of required external components, the cost of producing a multiple function battery operated device 60 is reduced without sacrificing features and/or functionality.

[0048] The multimedia module 24 is further coupled to the video and/or text display 78, which may be an electro-luminance backlight display, an LCD display, or any other type

of display that displays text, video graphics, and/or video images (still or motion). The multimedia module 24 receives digital video data from the on-chip memory and/or an external memory 86 under the control of the processing module 30, which is executing a text and/or video playback multimedia application. Upon receiving the digital video data, the multimedia module 24 converts it into pixel information (for example, RGB, YUV, YCrCb, etc.), which is provided to the video an/or text display 78.

[0049] If the display 78 is an electro-luminance backlight display, the system-on-a-chip includes the electro-luminance backlighting drive circuitry 70. In general, the electro-luminance backlighting drive circuitry 70 provides the control signals for the power transistors of the electro-luminance backlight display, thus eliminating the need for an extra integrated circuit to generate the control signals. By eliminating the need for an extra integrated circuit, the cost of producing a multiple function battery operated device 60 is reduced without sacrificing features and/or functionality.

[0050] The battery charger 66 is operably coupled to charge the battery 14 when the external source 68 is coupled to the device 10. The external source 68 may be a 5 volt supply that is received via a USB connection to a host computer or other external source having a USB connection. The details of the battery charger 66 are described in U.S. patent application entitled METHOD AND APPARATUS TO PERFORM BATTERY CHARGING USING A DC-DC CONVERTER CIRCUIT, having serial no. 10/675,116, and a filing date of September 30, 2003, and U.S. patent application entitled OVERVOLTAGE AND BACKFLOW CURRENT PROTECTION FOR A BATTERY CHARGER, having serial no. 10/675,101, and having filing date September 30, 2003, both of which are hereby incorporated by reference.

[0051] Each of the processing modules 30-1 through 30-*n* may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, micro-controller, digital signal processor, microcomputer, central processing unit, field programmable gate array, programmable logic device, state machine, logic circuitry, analog circuitry, digital circuitry, and/or any device that manipulates signals (analog and/or digital) based on operational instructions. Further,

each of the processing modules may be performing separate multimedia applications and/or co-process a single multimedia application. Such multimedia applications 46 include, but are not limited to, audio playback, audio record, video playback, video record, storing text, displaying text, storing video graphics, file system transfer, and/or displaying video graphics.

[0052] The on-chip memory 32 is shown to include ROM 88 and RAM 90. The ROM 88 may store a boot algorithm to initiate the battery-optimized system-on-a-chip 62, video graphics data, and/or any other system level data that should not be overwritten. The RAM 90 may be used as a first and/or second level cache memory for the processing modules 30 and may range from a few hundred kilobits to several hundreds megabits of storage capacity.

[0053] Figure 3 is a schematic block diagram of a digital power conserving circuit 92 of a power conservation unit 250 (*see* Figure 2) that includes a portion of an IC 100, a sensing circuit 102, and a comparator 116. The portion of the IC 100 may be a speed test circuit (for example, a plurality of gates interoperably coupled, an adder, a multiplier, ring oscillator, etc.), a critical path within the IC (for example, the path in the IC have the greatest amount of delay), and/or a replica of the critical path within the IC. The power conserving circuit 92 is provided through power conserving circuit 250, shown in Figure 2.

[0054] In operation, the portion of the IC 100 receives a test input 106, which may be a single bit of data, an enable signal, and/or multiple bits of data having a known pattern. The sensing circuit 102 determines when the portion of the IC 100 receives the test input 106 with respect to a known clock 104. The sensing circuit 102 monitors the output of the portion of the IC 100 to determine when the test output 108 is produced. When the test output 108 is detected, the sensing circuit 102 determines the number of cycles of the known clock 104 that has passed between the portion of the IC 100 receiving the test input 106 and it producing the test output 108 to produce a count value. Alternatively, the sensing circuit 102 counts the number of iterations of performing the function during

a clock cycle (for example, how many oscillations of a ring oscillator occur during a clock cycle) to determine a count value.

[0055] The sensing circuit 102 converts the count value into a measured processing speed 110 of the portion of the IC 100. For example, if the test circuit is a ring oscillator, that is, a plurality of inverters coupled in cascaded fashion, the rise and fall times can be determined based on the number of iterations in a clock cycle, where the rise and fall times can be used to determine the processing speed. The comparator 116 compares the measured processing speed 110 with a critical processing speed 112 to determine whether the supply voltage can be adjusted 114 and by how much. In general, the critical processing speed 112 corresponds to the time during which the portion of the IC must perform its function in order to avoid a timing error in the system-on-a-chip. If the measured processing time is less than the critical processing time, the supply voltage may be decreased, which slows the processing speed of the portion of the IC 100 but also reduces power consumption of the IC. This is graphically illustrated in Figures 4 and 5.

[0056] Figure 4 illustrates a graph that plots supply voltage versus transistor speed, which is a key factor in determining the speed of the portion of the IC 100. As shown, from IC to IC and/or over temperature, the transistor speed with respect to supply voltage will vary. Ideally, it is desired to set the supply voltage such that the speed of the transistor (for example, rise and fall times) is at the critical speed or slightly above the critical speed. As shown, however, the speed to supply voltage may vary from IC to IC and within the same IC as the operating temperature of the IC changes. For instance, many ICs will have the nominal temperature , while a few will experience the minimum temperature, and a few will experience the maximum temperature. Without the power conserving circuit 92 (*see* Figure 3), the supply voltage for all of the all ICs in this lot and in other lots would have to be set to handle the worst-case condition, where the critical processing speed is only achieved with a maximum supply voltage. As such, even though most of the ICs have a better speed to supply voltage ratio, they are operated based on the worst-case condition. Thus, they consume more power than necessary to perform their specific function since IC power consumption increases non-linearly as the supply voltage increases as shown in Figure 5.

[0057] The power conserving circuit 92 provides an adjust signal 114 for a supply voltage on a chip-by-chip basis such that the speed of a transistor is maintained at a rate just above the critical speed. Thus, some ICs will require the supply voltage to be set at or near the maximum level, some ICs will be able to have the supply voltage set at or near the minimum level, while most will have the supply voltage set somewhere between the maximum and minimum values. Accordingly, by lowering the supply voltage for an individual IC, the power consumption for the IC is minimized.

[0058] Figure 6 is a logic diagram of a method for conserving power of a system-on-a-chip that begins at step 120 where processing speed of at least a portion of an integrated circuit is measured to produce measured processing speed. The at least a portion of the integrated circuit includes a speed test circuit, a critical path of the integrated circuit, and/or a replicated circuit of the critical path of the integrated circuit. The measuring of the processing speed may be done as shown in steps 130 through 134. At step 130, the at least a portion of the integrated circuit performs a function, which may be, but is not limited to, an add function, a delay line function, a ring oscillation function, a memory retrieval function, and/or a multiplication function. The process then proceeds to step 132 where a number of cycles of a known clock are counted during the performing of function by the at least a portion of the integrated circuit or the number of iterations, or repetitions, of performing the function during a clock cycle to produce a count value. The process then proceeds to step 134 where the count value is equated to the processing speed.

[0059] Returning to the main path of the logic diagram, the process continues at step 122 where the measured processing speed is compared with a critical processing speed for the at least a portion of the integrated circuit. The process then proceeds to step 124 where a determination is made as to whether the comparison was favorable. If not, the process proceeds to step 126 where the supply voltage is maintained at its current setting, which initially may be set at its maximum value.

[0060] If the measured processing speed compared favorably to the critical processing speed, the process proceeds to step 128 where the supply voltage to the integrated circuit

is adjusted to reduce power consumption of the integrated circuit. In one embodiment, the adjusting of the supply voltage may be done by determining a ratio between the measured processing speed and the critical processing speed and proportionally adjusting the supply voltage based on the ratio. In another embodiment, the adjusting of the supply voltage may be done by adjusting the feedback of the supply voltage for regulation of an on-chip DC-to-DC converter that produces the supply voltage, or adjusting a reference voltage used for regulation of the on-chip DC-to-DC converter that produces the supply voltage. As one of average skill in the art will appreciate, the measuring, comparing, and adjusting to update the supply voltage may be periodically performed.

[0061] Figure 7a is a schematic diagram illustrating a process sensing channel 200 for measurement or assessment of an analog variation parameter of a portion of an IC 100 resulting from various fabrication parameters – that is, providing the ability to account for fabrication variations autonomously through the lifespan of the device. It is noted that the portions of an IC referred to herein are not to be construed as being the same, but may be other locations on the totality of the integrated circuit, and that the term "portion," as used, is to refer to something less than the entirety of the integrated circuit.

[0062] A suitable value used for assessing the analog variation parameter is the threshold voltage Vt of the IC. As shown, a diode-type field effect transistor ("FET") 202 with a known-current source 204 provides a measurement node 206, which allows measurement of the voltage of the diode-configured FET 202. This diod-type configuration can be implemented with *n* and *p*-type devices. The analog variation parameter is assessed by measuring the gate voltage of the transistor 202 at a point where a specific small drain current flows. An operational temperature is determined that is associated with the analog variation parameter (as discussed later in detail).

[0063] Accordingly, by assessing the analog variation parameter for the IC, the headroom voltage relating to the IC 100 is "sensed." This information regarding the analog circuitry headroom can be used in determining an adjust V_{DD} signal 252 (*see* Figure 2). The term "headroom voltage" is understood to be the available signal swing in analog circuitry before a performance loss becomes unacceptable, such as in signal

distortion via signal size, signal quality, etc. The AV_{DD} adjust signal 218 provides a mechanism for adjustment of the DC-to-DC converter 26. In this manner, the external power source 68 is optimized, thereby extending the useful lifespan of a power source to service the multiple function battery operated device 10 of Figure 1 or the multiple function battery operated device 60 of Figure 2.

[0064] Figure 7b illustrates a graph that plots interrelationships of fabrication parameter corners versus headroom voltage. The illustration is general in nature, and is set forth to convey the interrelationships that are represented by the analog variation parameter for assessing the magnitude of available headroom voltage. The fabrication parameter corners generally having greater influence on device operation are generally poly sheet ρ and temperature T (through the Vt voltage). The operational temperature T and voltage V_{DD} are conditional on the operational environment of the device 10 (*see* Figure 1) or of the device 60 (*see* Figure 2).

[0065] The analog circuitry operates within a headroom voltage, represented as the voltage between the gate and source terminals of the diode-type FET 202. With respect to the graph of Figure 7b, the gate length L, generally does not affect the headroom voltage of the analog devices when long L devices are used. Accordingly, whether the length L is 1, or 1.1, the degree of influence to the headroom voltage is minimized in view of other factors having greater influence to the headroom voltage.

[0066] The absolute value of the threshold voltage |Vt|, as discussed above, is a fabrication process corner. As an example, presume a fabrication process has the capability of providing an IC with an absolute threshold voltage value |Vt| being 0.4 volts $\pm$ 0.1 volts. If the resulting value of |Vt| is at the higher range (as a result of fabrication or environmental influences such as temperature), then the transistor turns "on" at 0.5 volts instead of the 0.4 volt value. The higher the threshold voltage |Vt|, then the smaller range the drain voltage has to "swing." Also, as the threshold voltage value |Vt| increases, the available headroom voltage decreases. In other words, if an analog device can be fabricated on an integrated circuit having a lower threshold voltage |Vt|, then a higher headroom voltage is achievable.

[0067] As shown, poly sheet ρ is inversely proportional to the device bias current. Poly sheet ρ is the sheet resistance of poly silicon in units of ohms-per-square. Poly sheet is used for several things in an integrated circuit fabrication process, including resistor applications. Bias currents to the analog circuits of an integrated circuit are typically the band-gap voltage divided by a poly resistor. That is, the current *I* equals the band-gap voltage divided by a resistance R, where resistance R is poly sheet ρ times length divided by width. The bias currents are inversely proportional to poly sheet ρ. The relationship to the headroom voltage for the analog circuitry is that increase bias currents in turn can limit the headroom voltage.

[0068] Though the poly sheet ρ parameter does not have a large influence to the performance of the digital circuits of an integrated circuit, it does affect the headroom voltage for analog operation. Accordingly, if poly sheet ρ is low, there is more current, and the biasing of each device is larger, diminishing the headroom voltage.

[0069] With the operational temperature T, the absolute value of the threshold voltage |Vt| trends downward as the as the operational temperature T increases. The opposite effect results as the operational temperature T decreases, causing the absolute value of the threshold voltage |Vt| to increase. Thus, for low temperature, a higher threshold voltage |Vt| results, leaving less capacity for headroom voltage.

[0070] Figure 8 is a schematic block diagram of an analog power conserving circuit 209 that includes a portion of an IC 100, a process sense module 208, an operational temperature sensor 210, and an analog V_{DD} (AV_{DD}) look-up table 214. The portion of the IC 100, for example, may be an operational amplifier circuit.

[0071] In operation, the process sense module 208 senses the analog variation parameter of the IC 100 portion, and provides an analog parameter signal 215. The operational temperature sensor 210 senses the operational temperature of an IC 100 portion. This value is associated with the analog variation parameter determination of the process sense module 208. The operational temperature sensor 210 provides a temperature signal 216. The AV_{DD} look-up table 214 has inputs that receive the analog variations parameter signal 215 and the temperature signal 216.

[0072] The analog variations parameter signal 215 provides a signal representation interaction of the fabrication parameters and the operational parameters with the magnitude of available headroom voltage. The operational parameters being represented in the analog variations parameter signal 215 are generally those set out in the graph of Figure 7b that plots interrelationships of fabrication parameter corners versus headroom voltage, including the poly sheet ρ.

[0073] The AV_{DD} look-up table 214, based on inputs from the analog variations parameter signal 215 and the operational temperature signal input 216, provides an analog V_{DD} (AV_{DD}) adjust signal 218. The AV_{DD} look-up table 214 may also be provided as a memory device operably connected to a microprocessor, or provided as a logic circuit, that contains information and data representing the represents the threshold voltage curve, the operational temperature curve, and voltage V_{DD} curve with respect to the headroom voltage plot shown in Figure 7b. With this information, an AV_{DD} adjust signal 218 is generated responsive to the analog variations parameter signal 215, based on the operational temperature signal 216.

[0074] With respect to analog circuitry on the IC 100, the AV_{DD} adjust signal 218 is accepted by a DC-to-DC converter 26, which is operably coupled to the battery 14 and inductor 16 (*see* Figure 2) to produce at least one supply voltage for analog circuitry (V_{DD}). In general, the DC-to-DC converter 26 may be a buck converter, a boost converter, a fly-back converter, a half bridge converter, and/or a full bridge converter. Note that the DC-to-DC converter can also be an inductor-less configuration including a linear regulator and/or a switched-capacitor regulator.

[0075] Through normal use and operation, the multiple function battery operated device 10 or device 60 is subjected to varying environmental conditions. Accordingly, the adjustment signal 218 can be updated by repeating the determination of at least one of the operational temperature T and the analog variation parameter conveyed by the analog parameter signal 215, which can be conducted by the operational temperature sensor 210, and the process sense module 208, respectively.

[0076] Figure 9 illustrates a schematic block diagram of an operational temperature sensor 210 for deployment on a portion of an integrated circuit 100. The operational temperature sensor 210 determines the operational temperature T associated with an analog variation parameter for the integrated circuit 100.

[0077] Due to the supply voltage optimization, the temperature sensor configuration used should be sensitive to temperature but sufficiently immune to other deviations, including power supply voltage variation. Sufficient immunity to deviations can be provided via reference structures such as that of Figure 9, or variable-compensation techniques or other suitable techniques that account for variable deviation.

[0078] The temperature sensor 210 has a proportional-to-absolute-temperature ("PTAT") generator module 220, and a digital control module 222. Generally, the temperature sensor 210 of Figure 9 provides a temperature signal 216 that is based on a comparison conducted between current sources I_{PTAT} and I_{ref} provided at node 224. The comparison is provided by the comparator module 226.

[0079] The PTAT generator module 220 provides a current source I_{PTAT}. The current source I_{PTAT}, as suggested, has a magnitude that is proportional to absolute temperature that changes as the temperature T of the portion of the IC 100 changes. The digital control module 222 provides a temperature signal 216. Also, the digital control module 222 provides a reference current source I_{ref}, which is a fixed current that is independent of temperature, thus providing a constant reference current function having the property of never increasing and of never decreasing as the value of the temperature T increases or otherwise changes. The digital control module 222 contains a register that outputs, through the temperature signal 216, a value representative of an operational temperature T of the portion of the IC 100.

[0080] Figure 10 is a graph that plots current versus temperature for illustrating the operation of the operational temperature sensor 210 and via the relationship of the reference current I_{REF} and the variable current I_{PTAT}. As shown in Figure 10, reference current I_{REF} is substantially constant with respect to temperature T. Reference to Figure 9 will be made for discussion of the graph of Figure 10.

[0081] To begin, the current source I_{REF} is less than the magnitude of the variable current I_{PTAT}. An output of the comparator module 226 provides a logic "low" value to the digital control module 222 via a temp_sense signal 228. The digital control module 222 operates at a speed designated by a clock signal.

[0082] The digital control module 222 senses the temp_sense signal 228, and updates an up/down counter to reflect the status of the temp_sense signal 228 with respect to iterations of the clock signal. The digital control module 222 incrementally increases the reference current I_{REF} for sampling at the next clock cycle of the clock signal the temp_sense signal 228. This process of incrementing the reference current I_{REF} continues until a trip point is achieved. The trip point occurs when the reference current I_{REF} intersects the variable current I_{PTAT}. In other words, where the reference current I_{REF} is substantially equal to the variable current I_{PTAT} at node 224, causing the comparator module 226 to trip. Upon tripping, the temp_sense signal 228 of the comparator module 226 transitions to a logic "high" value, indicating "temperature found" to the digital control module 222.

[0083] With a logic high value provided by the temp_sense signal 228, the up/down counter of the digital control module 222 stops incrementing with respect to the logic low value of the temp_sense signal 228 and iterations of the clock signal, . The contents of the up/down counter are latched and are provided to the look-up table 214 (*see* Figure 8) by the temperature signal 216. The digital control module 222 then powers down the PTAT generator module 220 through power control signal 230.

[0084] As can be readily appreciated, other circuits or configurations can be implemented for assessment of the operational temperature T. As a further alternative, operational temperature T may be estimated based upon a difference of the values of the analog parameter signal 215 over time. That is, the estimate, or inference, can be used as an indicator of temperature or temperature difference. These inferences can be processed with the analog parameter signal 215 for generation of an AV_{DD} adjust signal 218 from the AV_{DD} look-up table 214. Such an inference of the operational temperature, however,

would not provide the level of accuracy otherwise available through the operational temperature sensor 210 of Figure 9.

[0085] Figure 11is a schematic block diagram showing a power conserving circuit 250 that provides an adjust supply voltage signal 252 for a shared voltage source supplying power to the analog and the digital circuitry of the battery-optimized system-on-chip 62 (*see* Figure 2).

[0086] The power conserving circuit 250 has a component addressing digital circuitry power optimization - power conserving circuit 92, and a second component addressing analog circuitry power optimization - analog power conservation circuit 209. Each optimization circuit provides respective inputs to the comparator 260. The comparator provides an adjust supply voltage signal 252.

[0087] In operation, the comparator 260 determines the greater of the input values provided. That is, a selection of the digital adjust supply voltage 217 representing the digital variation parameter, or of the AV_{DD} adjust signal 218 representing the analog variation parameter with respect to the operational temperature T. In other words, the determination is that when the first, or digital, adjust supply voltage signal 114 compares favorably with the second, or AV_{DD}, adjust signal 218, then the first, or digital, adjustment signal is selected as the adjust supply voltage signal 252. Otherwise, the second, or AV_{DD}, adjustment signal is selected as the adjust supply voltage signal 252.

[0088] The adjust supply voltage signal 252 is accepted by a DC-to-DC converter 26, which is operably coupled to the battery 14 and inductor 16 to produce a supply voltage V_{DD} to the circuitry of the battery-optimized system-on-chip 62. In general, the DC-to-DC converter may be a buck converter, a boost converter, a fly-back converter, a half bridge converter, and/or a full bridge converter. Note that the DC-to-DC converter can also be an inductor-less configuration including a linear regulator and/or a switched-capacitor regulator.

[0089] Through use and operation, the multiple function battery operated device 10 is subjected to varying environmental conditions. Accordingly, the adjustment signal 252

can be updated by repeating the determination of at least one of the operational temperature T and the analog variation parameter, which can be conducted by the operational temperature sensor 210, and the process sense module 208, respectively.

[0090] Figures 12a, 12b, and 12c provide a logic diagram of a method for conserving power of a system-on-a-chip that begins at step 302 where the analog variation parameter is determined, representing fabrication process variations to the IC. Step 304 determines the operational temperature T of the integrated circuit. At step 306, determination of the analog voltage level (AV_{DD}) signal is conducted based on the analog variation parameter with respect to the operational temperature T.

[0091] At step 308, if a digital component is present on the integrated circuit, or present for a shared power supply with the analog component of the integrated circuit, then the method proceeds to step 352 (*see* Figure 12b). If not, indicating that either there is no digital component for the power supply to allocate appropriate energy resources (either by not being present, or the digital component has a devoted power channel), the method proceeds to step 310 where the power consumption of the IC is optimized by adjusting the supply voltage V_{DD} to the analog voltage level AV_{DD} signal. The process then can be repeated by returning to step 302.

[0092] If a digital component is present, as determined at step 308 at Figure 12a, the method continues to step 352 of Figure 12b where processing speed of at least a portion of an integrated circuit is measured to produce measured processing speed. The at least a portion of the integrated circuit includes a speed test circuit, a critical path of the integrated circuit, and/or a replicated circuit of the critical path of the integrated circuit. The measuring of the processing speed may be done as shown in Figure 12c as steps 376 through 380. At step 376, the at least a portion of the integrated circuit performs a function, which may be, but is not limited to, an add function, a delay line function, a ring oscillation function, a memory retrieval function, and/or a multiplication function. The process then proceeds to step 378 where a number of cycles of a known clock are counted during the performing of function by the at least a portion of the integrated circuit or the number of iterations, or repetitions, of performing the function during a clock cycle to

produce a count value. The process then proceeds to step 380 where the count value is equated to the processing speed.

[0093] Returning to the main path of the logic diagram of Figure 12b, the process continues at step 354 where the measured processing speed is compared with a critical processing speed for the at least a portion of the integrated circuit. The process then proceeds to step 356 where a determination is made as to whether the comparison was favorable. If not, the process proceeds to step 358 where the digital variation parameter is maintained at its current setting.

[0094] If the comparison is favorable, then in step 360 the digital variation parameter is the favorable comparison result from step 356. In one embodiment, the adjusting of the supply voltage may be done by determining a ratio between the measured processing speed and the critical processing speed and proportionally adjusting the supply voltage based on the ratio. In another embodiment, the adjusting the supply voltage may be done by adjusting the feedback of the supply voltage for regulation of an on-chip DC-to-DC converter that produces the supply voltage, or adjusting a reference voltage used for regulation of the on-chip DC-to-DC converter that produces the supply voltage.

[0095] In step 362 determination of an adjustment signal as based on the analog variation parameter with respect to the operational temperature against the digital variation parameter. In this instance a comparison is made between the analog variation parameter and the digital variation parameter. The adjustment signal is the favorable result. At step 364 optimization, or reduction, of power consumption of the integrated circuit is accomplished by adjusting the supply voltage via the adjustment signal selected as the favorable result.

[0096] As one of average skill in the art will appreciate, the measuring, comparing, and adjusting to update the supply voltage may be repeatedly performed, as indicated by the return of the method to step 302 (*see* Figure 12a).

[0097] The preceding discussion presents a method and apparatus for conserving power on an IC-by-IC, or chip-by-chip, basis, and over time. In a first aspect, this is achieved

by measuring the processing speed of the IC, comparing the measured processing speed with a critical processing speed, and if the measured processing speed is faster than the critical processing speed, decreasing the supply voltage such that the actual processing speed approaches the critical processing speed. In another aspect, power optimization, or conservation, is achieved by determining an analog variation parameter with respect to an operational temperature, decreasing the supply voltage such that a sufficient headroom voltage for analog signal performance is provided. In yet another aspect, the digital variation parameter – as set out as the value representative of the actual processing speed approaches the critical processing speed, is compared with the analog variation parameter. The resulting favorable comparison provides a basis to decrease or optimize the supply voltage. As one of average skill in the art will appreciate, other embodiments may be derived from the teachings of the present invention without deviating from the scope of the claims.

[0098] As one of average skill in the art will appreciate, the term "substantially" or "approximately", as may be used herein, provides an industry-accepted tolerance to its corresponding term. Such an industry-accepted tolerance ranges from less than one percent to twenty percent and corresponds to, but is not limited to, component values, integrated circuit process variations, temperature variations, rise and fall times, and/or thermal noise. As one of average skill in the art will further appreciate, the term "operably coupled", as may be used herein, includes direct coupling and indirect coupling via another component, element, circuit, or module where, for indirect coupling, the intervening component, element, circuit, or module does not modify the information of a signal but may adjust its current level, voltage level, and/or power level. As one of average skill in the art will also appreciate, inferred coupling (that is, where one element is coupled to another element by inference) includes direct and indirect coupling between two elements in the same manner as "operably coupled". As one of average skill in the art will further appreciate, the term "compares favorably", as may be used herein, indicates that a comparison between two or more elements, items, signals, etc., provides a desired relationship. For example, when the desired relationship is that signal 1 has a greater magnitude than signal 2, a favorable comparison may be achieved when the

magnitude of signal 1 is greater than that of signal 2 or when the magnitude of signal 2 is less than that of signal 1 (*see* Figure 1).

CLAIMS

What is Claimed is:

1. A method for power supply optimization of an integrated circuit, comprising:

determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;

determining an operational temperature associated with the analog variation parameter; and

determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature, such that power consumption of the integrated circuit is optimized.

2. The method Claim 1 further comprises:

adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal.

3. The method of Claim 2 further comprises:

updating the adjustment signal by repeating at least one of the determination of the operational temperature and determining the adjustment signal.

4. The method of Claim 1 further comprises:

determining a digital variation parameter; and

determining the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature.

5. The method of Claim 4 wherein the determining the adjustment signal comprises:

determining a first adjustment signal based on the analog variation parameter;

determining a second adjustment signal based on the digital variation parameter;

comparing the first adjustment signal to the second adjustment signal; and

when the first adjustment signal compares favorably with the second adjustment signal, selecting the first adjustment signal as the adjustment signal, else the second adjustment signal as the adjustment signal.

6. The method Claim 4, wherein determining a digital variation parameter comprises:

measuring processing speed of at least a portion of an integrated circuit to produce measured processing speed;

comparing the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit; and

when the measured processing speed compares favorably to the critical processing speed, correspondingly set a value of the digital variation parameter.

7. The method of Claim 4 further comprises:

adjusting a regulation signal of a DC-to-DC converter based on the adjustment signal.

8. The method of Claim 7 further comprises:

updating the adjustment signal by repeating at least one of the determination of the operational temperature, the determination of the analog variation parameter, and of the digital variation parameter

9. An apparatus for increasing power supply efficiency of an integrated circuit comprises:

a processing module; and

a memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;

determine an operational temperature associated with the analog variation parameter; and

determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter and the operational temperature, such that power consumption of the integrated circuit is optimized.

10. The apparatus of claim 9, wherein the memory further stores operational instructions that cause the processing module to:

adjust a regulation signal of a DC-to-DC converter based on the adjustment signal.

11. The method of Claim 10, wherein the memory further stores operational instructions that cause the processing module to:

update the adjustment signal by repeating at least one of the determination of the operational temperature and determine the analog variation parameter.

12. The apparatus of claim 9, wherein the memory further stores operational instructions that cause the processing module to:

determine a digital variation parameter; and

determine the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature.

13. The apparatus of claim 12, wherein the memory further stores operational instructions that cause the processing module to determine the digital variation parameter by:

measuring a processing speed of at least a portion of an integrated circuit to produce measured processing speed;

comparing the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit; and

when the measured processing speed compares favorably to the critical processing speed, set a corresponding value of the digital variation parameter.

14. The apparatus of claim 12, wherein the memory further stores operational instructions that cause the processing module to:

adjust a regulation signal of a DC-to-DC converter based on the adjustment signal.

15. The apparatus of claim 13, wherein the memory further stores operational instructions that cause the processing module to:

determine a first adjustment signal based on the analog variation parameter;

determine a second adjustment signal based on the digital variation parameter;

compare the first adjustment signal to the second adjustment signal; and

when the first adjustment signal compares favorably with the second adjustment signal, selecting the first adjustment signal as the adjustment signal, else selecting the second adjustment signal as the adjustment signal.

16. A comprehensive system-on-a-chip comprises:

a processing core operably coupled to process input digital data and produce therefrom output digital data;

digital interface circuitry operably coupled to provide the input digital data to the processing core and to receive the output digital data from the processing core;

mixed signal circuitry operably coupled to convert input analog signals into the input digital data and to convert the output digital data into output analog signals; and

battery optimization circuitry that includes a DC-to-DC converter and a power conservation circuit, wherein the DC-to-DC converter is operably coupled to convert a battery voltage into a supply voltage that supplies at least one of: the processing core, the digital interface circuitry, and the mixed signal circuitry, wherein the power conservation circuit includes:

processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

determine an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;

determine an operational temperature associated with the analog variation parameter;

determine a digital variation parameter representative of a processing speed of the integrated circuit; and

determine an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature and the digital variation parameter, such that power consumption of the integrated circuit is optimized.

17. The comprehensive system-on-a-chip of claim 16, wherein the memory further stores operational instructions that cause the processing module to:

adjust a regulation signal of a DC-to-DC converter based on the adjustment signal.

18. The comprehensive system-on-a-chip of claim 17, wherein the memory further stores operational instructions that cause the processing module to:

update the regulation adjustment by repeating at least one of the determination of the operational temperature and the determination of the analog variation parameter.

19. The comprehensive system-on-a-chip of claim 16, wherein the memory further stores operational instructions that cause the processing module to measure the processing speed by:

enabling a function to be performed by the at least a portion of the comprehensive system-on-a-chip;

counting at least one of a number of cycles of a known clock during the performing of function by the at least a portion of the integrated circuit and a number of repetitions of the function during a cycle of the known clock to produce a count value; and

equating the count value to the processing speed.

20. The comprehensive system-on-a-chip of claim 18, wherein the memory further stores operational instructions that cause the processing module to adjust of the supply voltage by:

determining the digital variation parameter as a ratio between the measured processing speed and the critical processing speed; and

adjusting the supply voltage based on an operational sufficiency of either the digital variation parameter or the analog variation parameter with respect to the operational temperature.

21. A method for increasing power supply efficiency of an integrated circuit, comprising:

determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit; and

determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter such that power consumption of the integrated circuit is optimized.

22. The method of claim 21 further comprises:

determining an operational temperature associated with the analog variation parameter; and

determining an adjustment signal for a power supply voltage level of the integrated circuit based on the analog variation parameter with respect to the operational temperature, such that power consumption of the integrated circuit is optimized.

23. The method of Claim 22 further comprises:

determining a digital variation parameter; and

determining the adjustment signal based on the digital variation parameter and the analog variation parameter with respect to the operational temperature.

24. The method of Claim 23 wherein the determining the adjustment signal comprises:

determining a first adjustment signal based on the analog variation parameter;

determining a second adjustment signal based on the digital variation parameter;

comparing the first adjustment signal to the second adjustment signal; and

when the first adjustment signal compares favorably with the second adjustment signal, selecting the first adjustment signal as the adjustment signal, else the second adjustment signal as the adjustment signal.

POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT

ABSTRACT OF THE DISCLOSURE

A method and apparatus for conserving power of a mixed-signal system-on-a-chip having analog circuitry, involving determination of an analog variation parameter that is representative of an integrated circuit fabrication process variance of the integrated circuit, and an operational temperature associated with the analog variation parameter. With the analog variation parameter and the operational temperature, an adjustment signal is determined for a power supply level of the integrated circuit, such that power consumption of the integrated circuit is optimized. Further, in mixed-signal integrated circuits with digital and analog circuitry, a digital variation parameter is determined, where the adjustment signal determination is based on the digital variation parameter and the analog variation parameter with respect to the operational temperature. With such a method and apparatus, power consumption is optimized on an IC-by-IC basis such that power consumption of each IC is optimized.

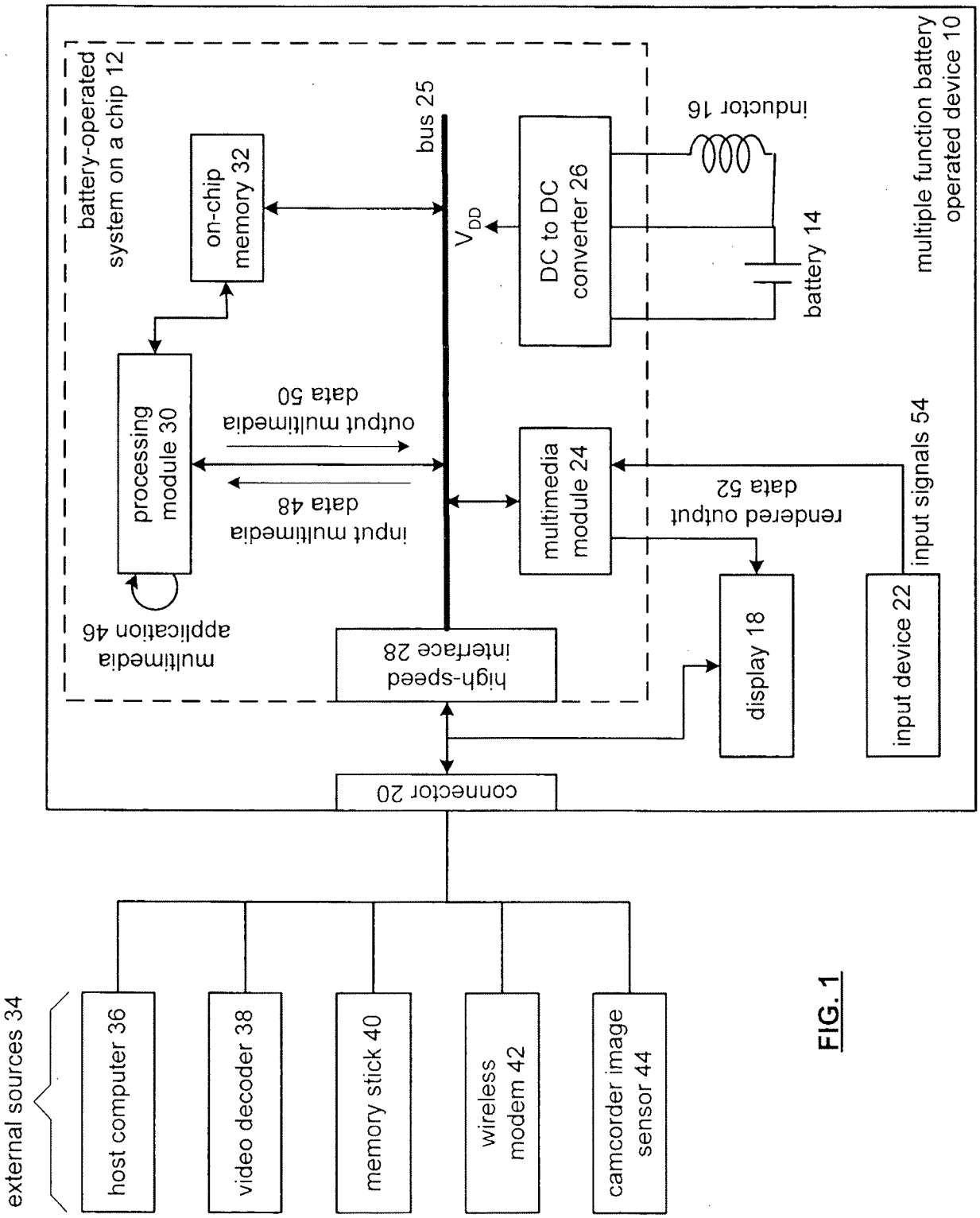

multiple function battery operated device 10
battery-operated system on a chip 12
bus 25
on-chip memory 32
V_{DD}
DC to DC converter 26
inductor 16
battery 14
processing module 30
output multimedia data 50
input multimedia data 48
multimedia application 46
multimedia module 24
rendered output data 52
input signals 54
high-speed interface 28
display 18
input device 22
connector 20
external sources 34
host computer 36
video decoder 38
memory stick 40
wireless modem 42
camcorder image sensor 44

FIG. 1

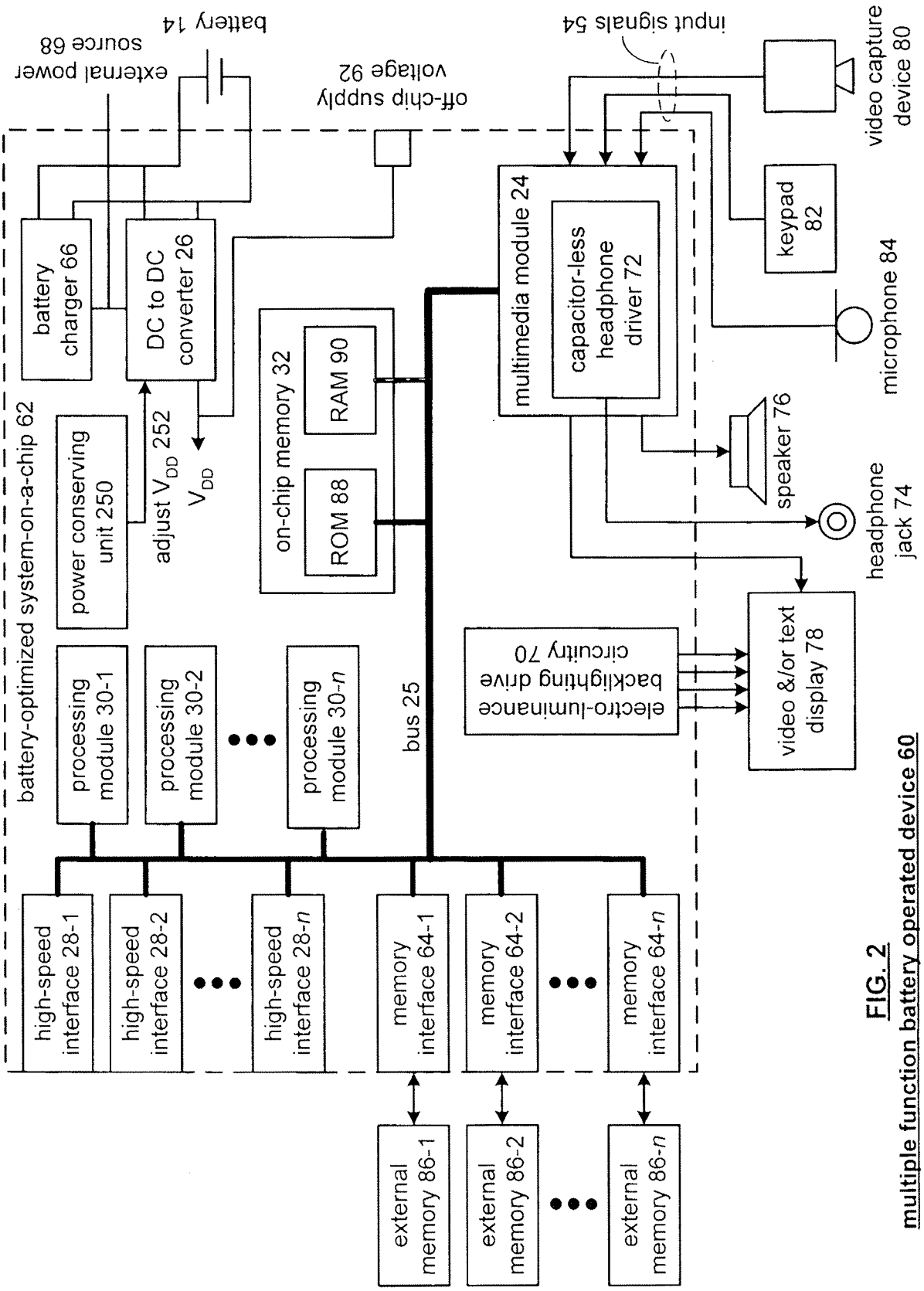


FIG. 2
multiple function battery operated device 60

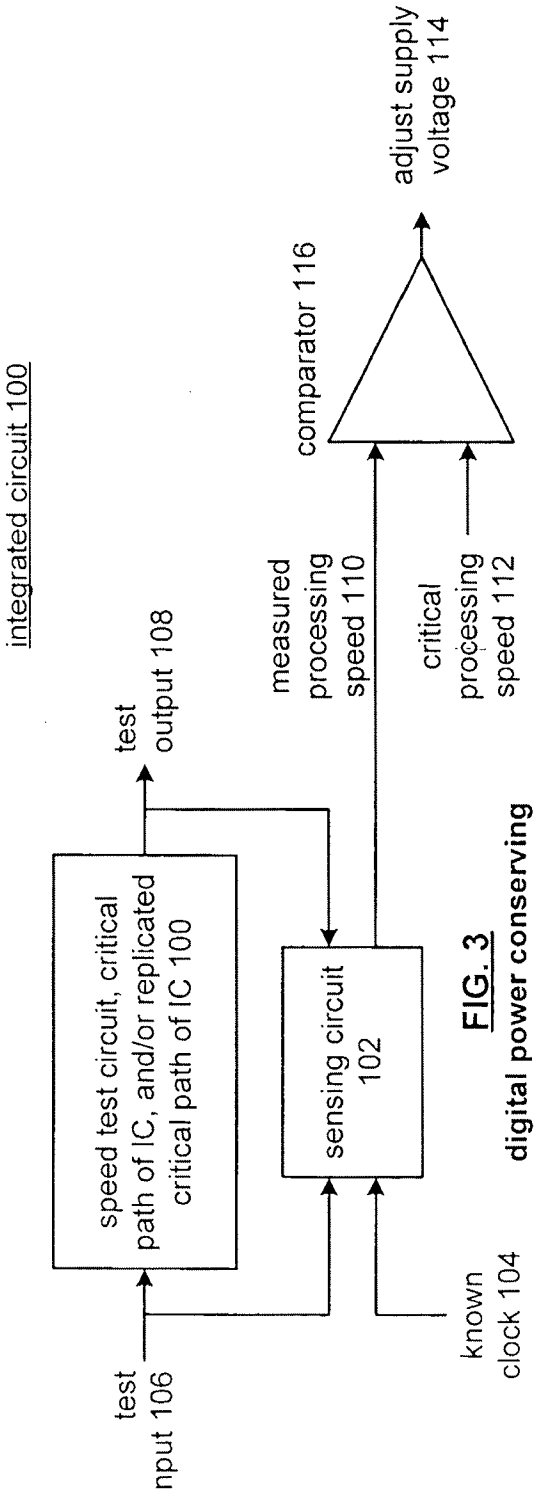


FIG. 3 digital power conserving circuit 92

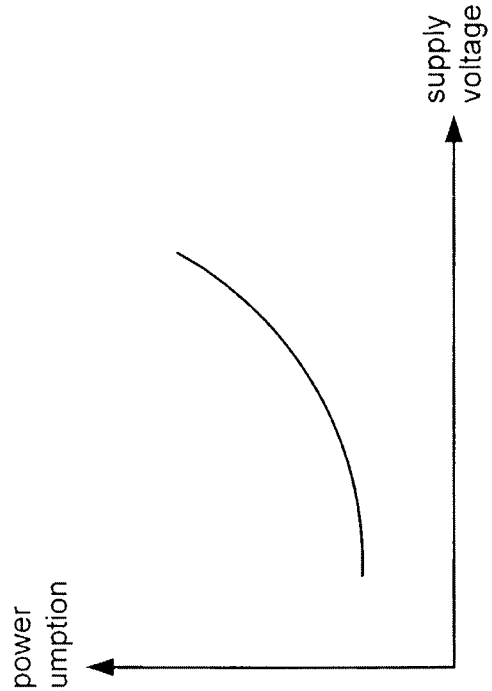


FIG. 5

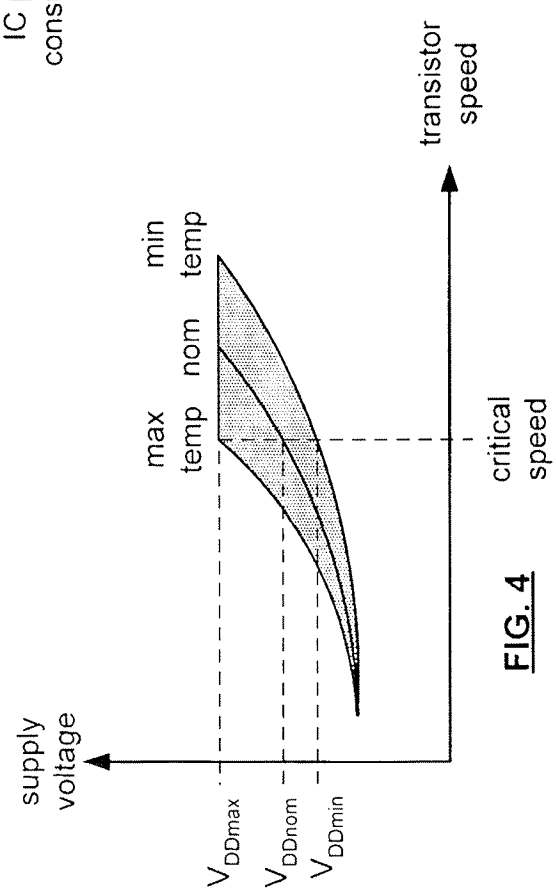


FIG. 4

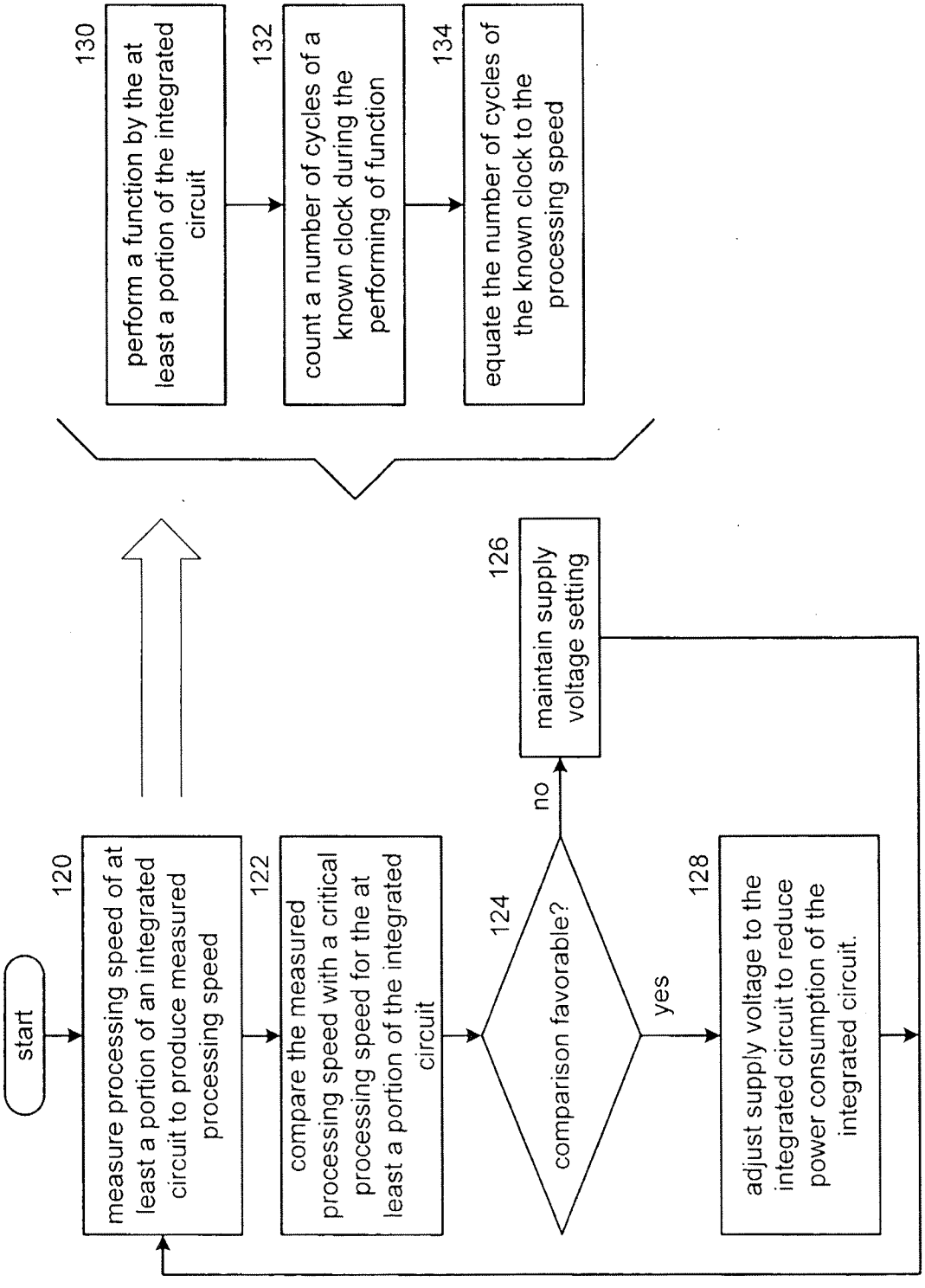

start
120
measure processing speed of at least a portion of an integrated circuit to produce measured processing speed
122
compare the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit
124
comparison favorable?
no
126
maintain supply voltage setting
yes
128
adjust supply voltage to the integrated circuit to reduce power consumption of the integrated circuit.
130
perform a function by the at least a portion of the integrated circuit
132
count a number of cycles of a known clock during the performing of function
134
equate the number of cycles of the known clock to the processing speed

FIG. 6

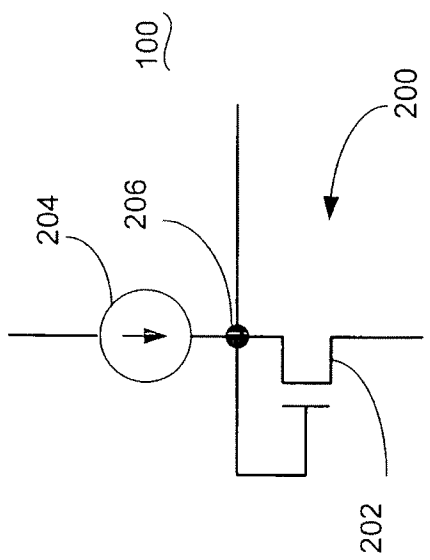


FIG. 7a

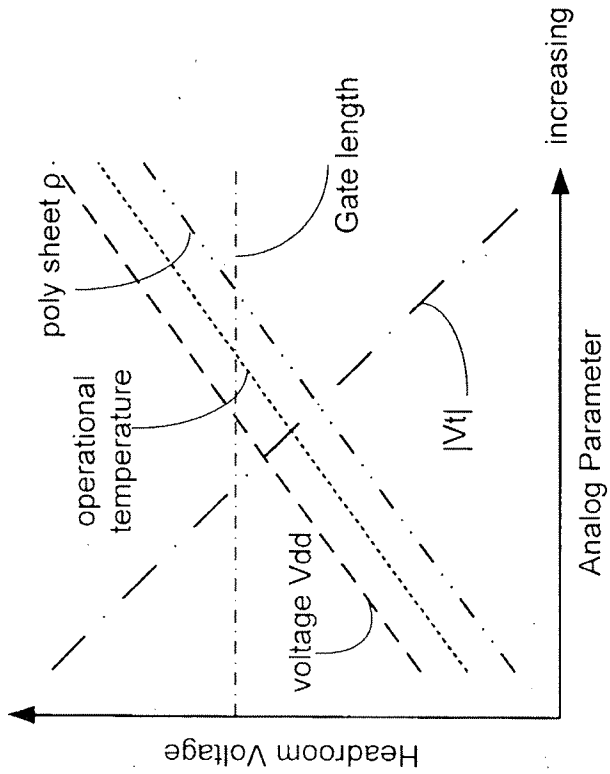


FIG. 7b

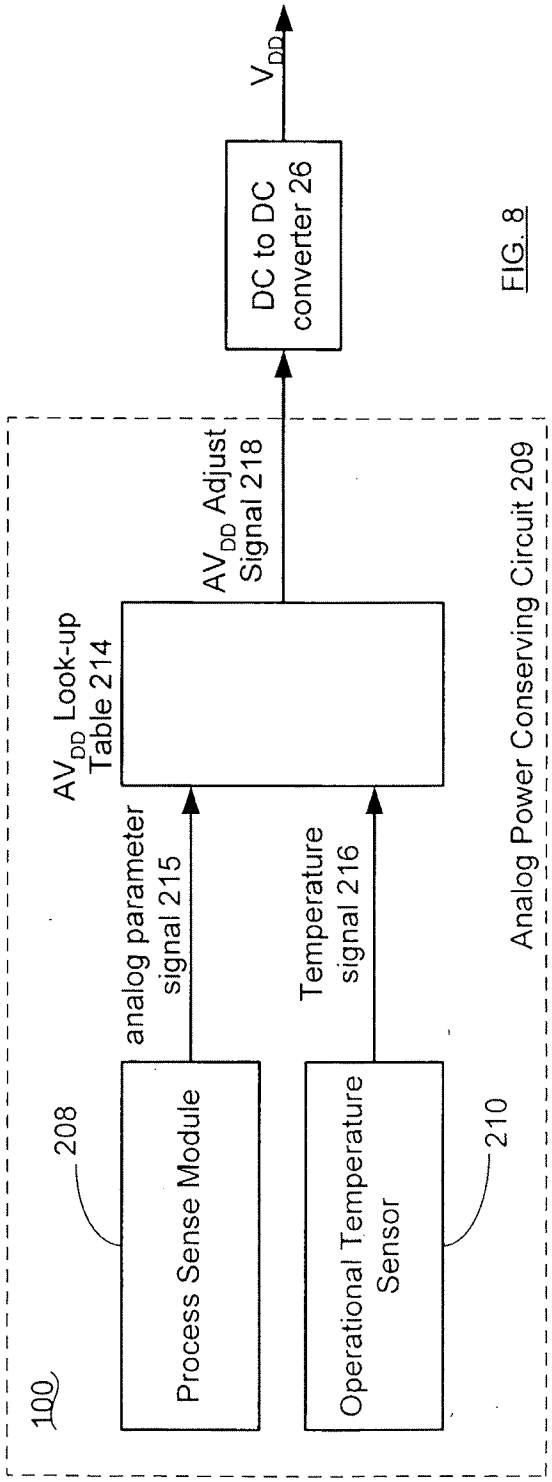


FIG. 8

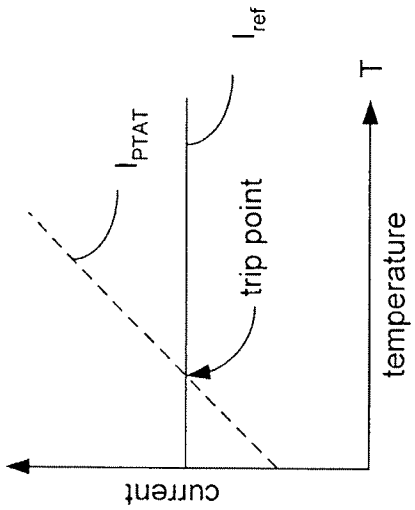
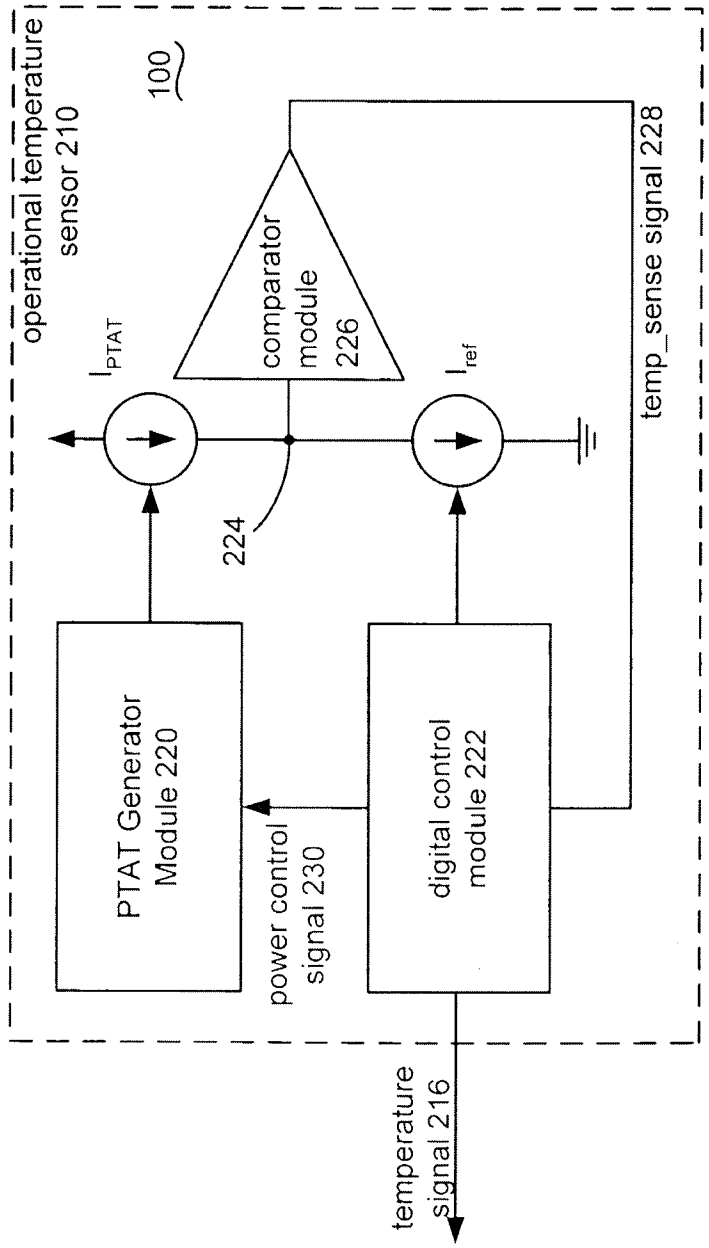

I_{ref}
I_{PTAT}
trip point
T
temperature
current

FIG. 10

FIG. 9


operational temperature sensor 210
100
I_{PTAT}
comparator module 226
I_{ref}
temp_sense signal 228
224
PTAT Generator Module 220
power control signal 230
digital control module 222
temperature signal 216

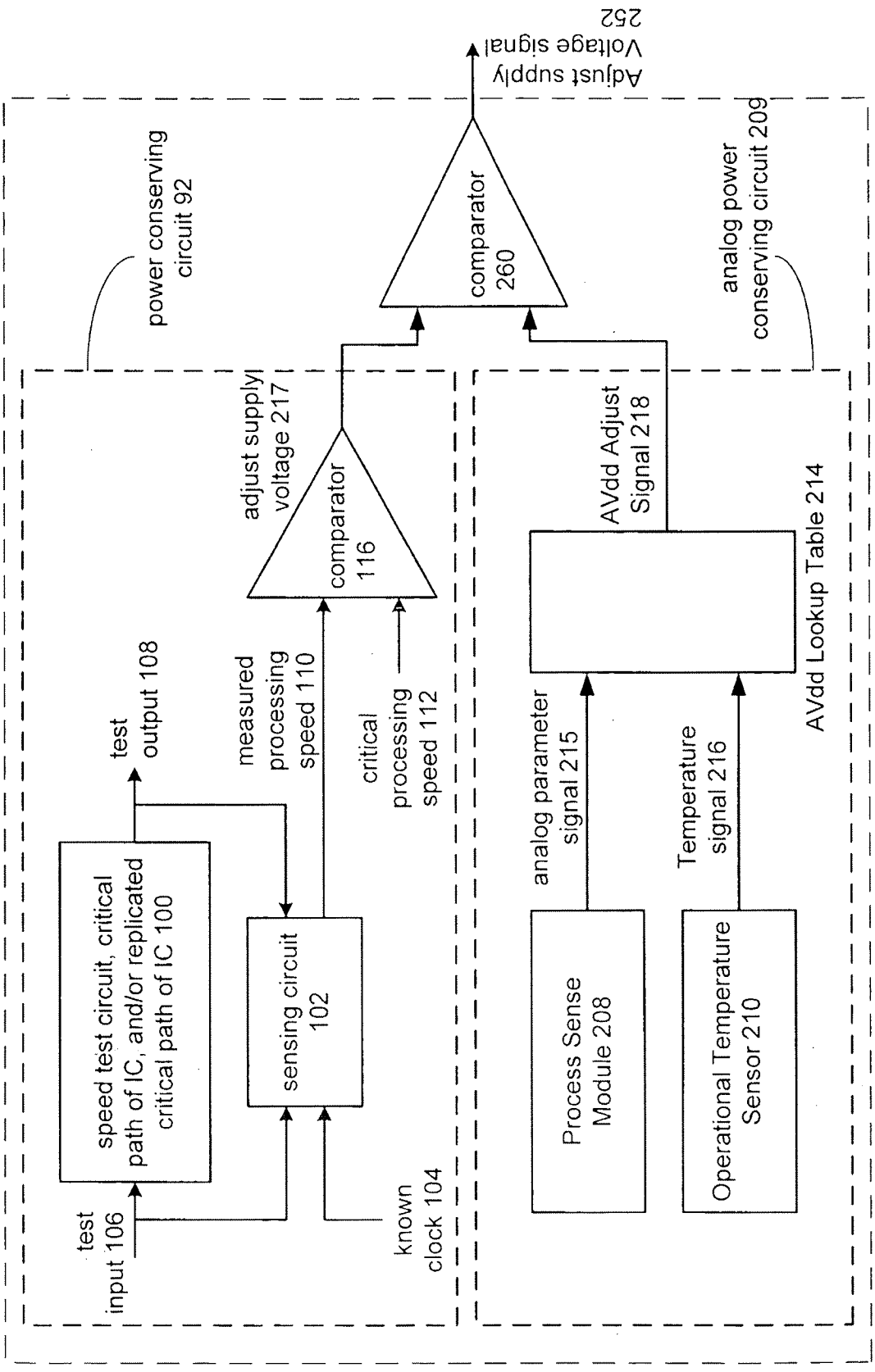


FIG. 11
power conserving circuit 250

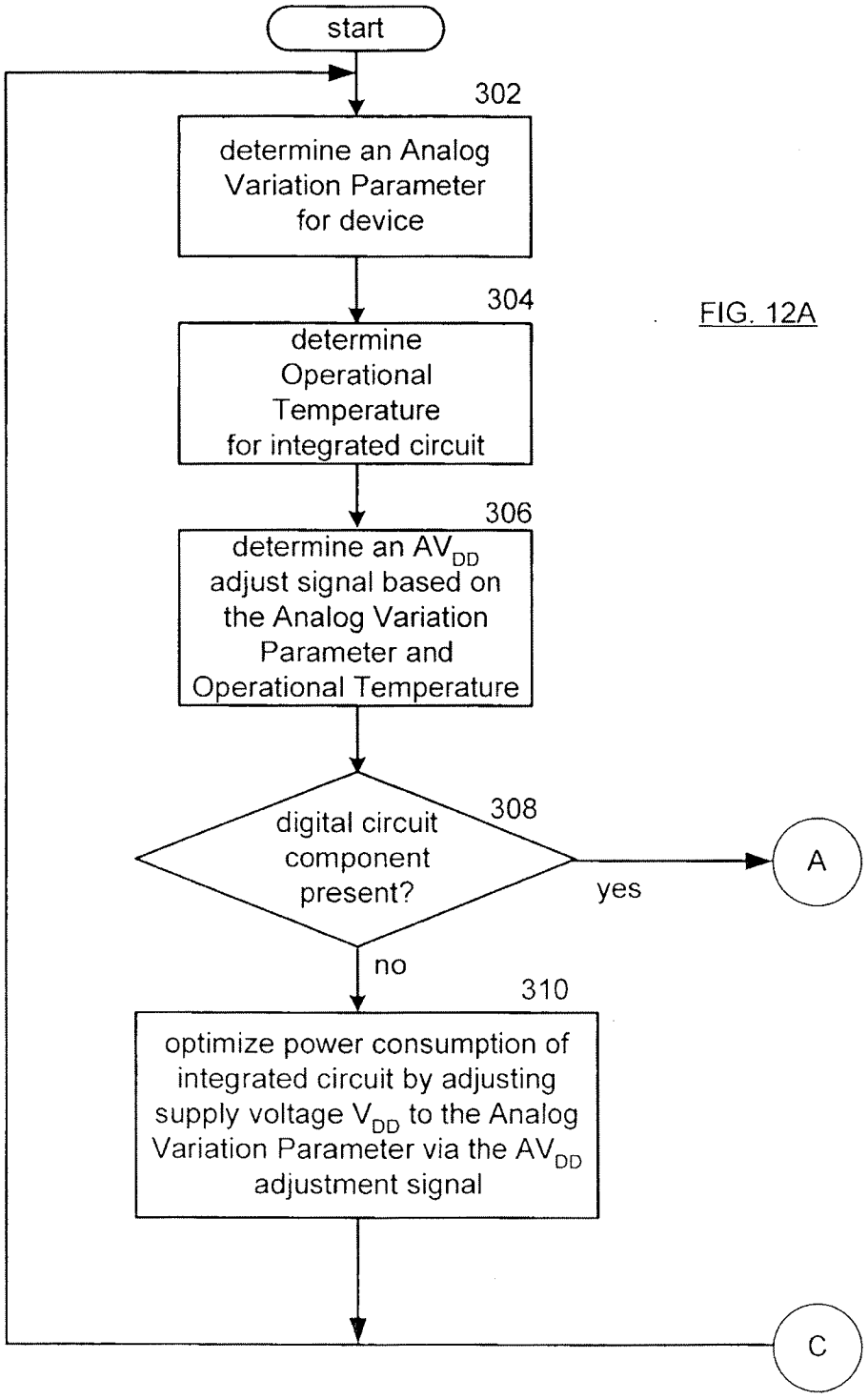

start
302
determine an Analog Variation Parameter for device
304
determine Operational Temperature for integrated circuit
306
determine an AV_{DD} adjust signal based on the Analog Variation Parameter and Operational Temperature
308
digital circuit component present?
yes
A
no
310
optimize power consumption of integrated circuit by adjusting supply voltage V_{DD} to the Analog Variation Parameter via the AV_{DD} adjustment signal
C

FIG. 12A

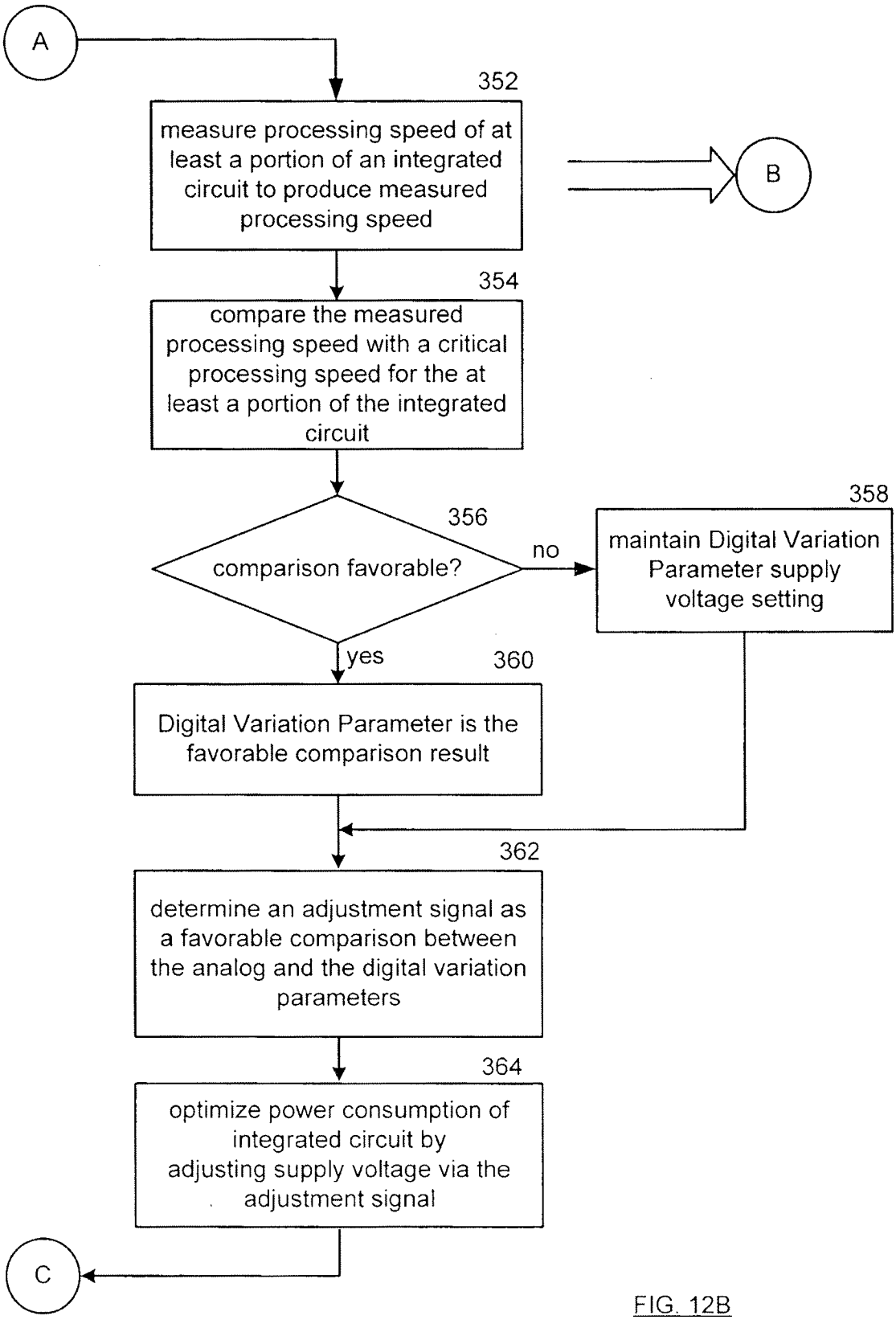

A
352
measure processing speed of at least a portion of an integrated circuit to produce measured processing speed
B
354
compare the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit
356
comparison favorable?
no
358
maintain Digital Variation Parameter supply voltage setting
yes
360
Digital Variation Parameter is the favorable comparison result
362
determine an adjustment signal as a favorable comparison between the analog and the digital variation parameters
364
optimize power consumption of integrated circuit by adjusting supply voltage via the adjustment signal
C

FIG. 12B

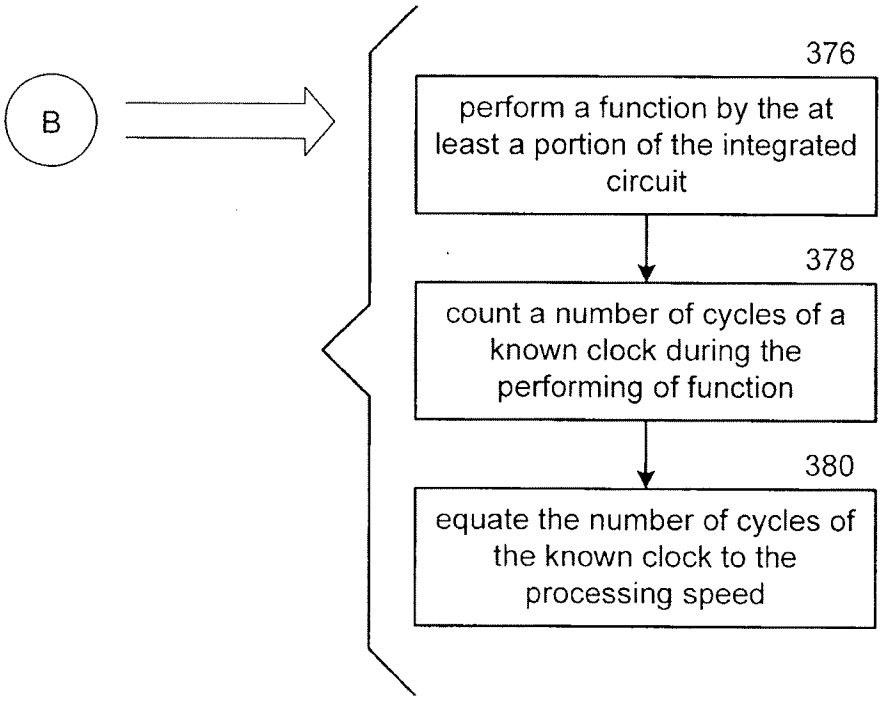

B
376
perform a function by the at least a portion of the integrated circuit
378
count a number of cycles of a known clock during the performing of function
380
equate the number of cycles of the known clock to the processing speed

FIG. 12C

Please type a plus sign (+) inside this box → [+]

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Application Number	
Filing Date	
First Named Inventor	Marcus W. May
Group Art Unit	
Examiner Name	
Attorney Docket Number	SIG000124

I hereby appoint:

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OR

[ ] Practitioner(s) named below:

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Name	Registration Number
Kevin L. Smith	38,620
Timothy W. Markison	33,534
Bruce E. Garlick	36,520
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Address	P.O. Box 160727				
Address					
City	Austin	State	TX	Zip	78716
Country	USA				
Telephone	(972) 772-8836	Fax	(972) 772-5033		

I am the:

[X] Applicant/Inventor.

[ ] Assignee of record of the entire interest. See 37 CFR 3.71
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

SIGNATURE of Applicant or Assignee of Record

Name	Matthew D. Felder
Signature	Matthew D Felder
Date	3/9/05

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[ ] *Total of forms are submitted. | SEND TO: Assistant Commissioner for Patents,

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Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

SIGNATURE of Applicant or Assignee of Record

Name	Marcus W. May
Signature	Marcus W. May
Date	03/09/05

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[X] Declaration Submitted with Initial Filing OR [ ] Declaration Submitted after initial Filing (surcharge (37 CFR 1.16(e)) required)

Attorney Docket Number	SIG000124
First Named Inventor	Marcus W. May
COMPLETE IF KNOWN	
Application Number	
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

POWER OPTIMIZATION OF MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT

(Title of the Invention)

the specification of which
[X] is attached hereto

OR
[ ] was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checkign the box, any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications Numbers(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]

[ ] Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119 (e), 120, or 365 (c) of any U.S. or PCT application(s) listed below.

Application Numbers(s)	Filing Date (MM/DD/YYYY)	
		[ ] Additional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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DECLARATION - Utility or Design Patent Application

Direct all correspondence to: [X] Customer Number or Bar Code Label	34,399	OR [ ] Correspondence address below	
Name	Kevin L. Smith		
Address	P.O. Box 160727		
Address			
City Austin		State TX	ZIP 78716
Country USA	Telephone (972) 772-8836		FAX (972) 772-5033

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.c. 1001 and that such willful false statements may jeorpardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR: [ ] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) Marcus W.		Family Name or Surname May	
Inventor's Signature Marcus W May			Date 03/09/05
Residence: City Austin	State TX	Country USA	Citizenship USA
Mailing Address 3111 Mistyglen Circle			
Mailing Address			
City Austin	State TX	ZIP 78746	Country USA

NAME OF SECOND INVENTOR: [ ] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) Matthew D.		Family Name or Surname Felder	
Inventor's Signature Matthew D. Felder			Date 3/9/05
Residence: City Austin	State TX	Country USA	Citizenship USA
Mailing Address 12109 Barrel Bend			
Mailing Address			
City Austin	State TX	ZIP 78748	Country USA

[ ] Additional inventors are being named on the _____ supplemental Additional Inventor(s) sheets(s) PTO/SB/02A attached hereto.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

03/16/2005 MMEKONEN 00000005 501415 11078150

01 FC:2011	150.00	DA
02 FC:2111	250.00	DA
03 FC:2311	100.00	DA
04 FC:2201	100.00	DA
05 FC:2202	100.00	DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/59033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

SI-C-000120

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	20	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	150.00	OR	BASIC FEE	300.00
X$ 25=	100	OR	X$50=	
X100=	100	OR	X200=	
+180=		OR	+360=	
TOTAL	350	OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.