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Paper 11
Entered: January 7, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

VLSI TECHNOLGY LLC,
Patent Owner.

IPR2019-01196
Patent 7,246,027 B2

Before BART A. GERSTENBLITH, MINN CHUNG, and KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

Petitioner, Intel Corporation, filed a Petition (Paper 3, "Pet.") for *inter partes* review of claims 1–3, 5–12, and 18–20 of U.S. Patent No. 7,246,027 B2 (Ex. 1001, "the '027 patent"), supported by the Declaration of David Harris (Ex. 1005, "Harris Declaration"). Patent Owner, VLSI Technology LLC, filed a Preliminary Response (Paper 7, "Prelim. Resp.") supported by the Declaration of Engin Ipek, Ph.D. (Ex. 2001, "Ipek Declaration"). Thereafter, Petitioner filed an authorized Reply (Paper 9 "Pet. Reply") to which Patent Owner filed an authorized Sur-reply (Paper 10, "PO Sur-reply"). Applying the standard set forth in 35 U.S.C. § 314(a), which authorizes institution of an *inter partes* review when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition," we deny institution of an *inter partes* review of the challenged claims of the '027 patent.

A. Real Parties-in-Interest

Petitioner identifies Intel Corporation as the real party-in-interest for Petitioner. Pet. 1. Patent Owner identifies VLSI Technology LLC and CF VLSI Holding LLC as the real parties-in-interest for Patent Owner. Paper 6, 2.

B. Related Matters

The parties represent that the '027 patent is at issue in *VLSI Technology LLC v. Intel Corp.*, Case No. 18-966 (D. Del.). Pet. 1; Prelim. Resp. 9.

C. The '027 Patent

The '027 patent, titled "Power Optimization of a Mixed-Signal System on an Integrated Circuit," was filed on March 11, 2005. Ex. 1001, Title, code [22]. The '027 patent issued on July 17, 2007. *Id.* at code [45].

The '027 patent states that one difficulty of optimizing power consumption of an integrated circuit ("IC") having mixed signals (i.e., analog and digital) is that analog and digital components operate under different parameters for their desired functional results. *See id.* at 2:16–18. For example, "lower operational temperatures raise the threshold voltage level for analog components, affecting signal performance, while favorable for digital component operation." *Id.* at 2:22–25. Conversely, "higher operational temperatures lower the threshold voltage level for analog components, while slowing digital gate response for digital components." *Id.* at 2:25–28. Accordingly, power consumption considerations for each type of component (i.e., analog and digital components) would differ. *Id.* at 2:28–30. The '027 patent states that although there were design techniques to reduce power consumption generally, these techniques were designed assuming the worst-case operation of an integrated circuit. *Id.* at 2:9–11. As a result, these techniques resulted in "integrated circuits [that would] consume more power than needed because the power reducing techniques were under a worst-case assumption and not individually optimized on a chip-by-chip basis. *Id.* at 2:11–15.

The '027 patent provides a solution "for conserving power of a system-on-a chip having analog circuitry." *Id.* at 2:40–41. With the methods described in the '027 patent, "power consumption is optimized on an IC-by-IC basis, as well as over time." *Id.* at 3:1–2.

Figure 11, reproduced below is a block diagram of a power conservation circuit in accordance with the invention of the '027 patent. *Id.* at 3:36–40.

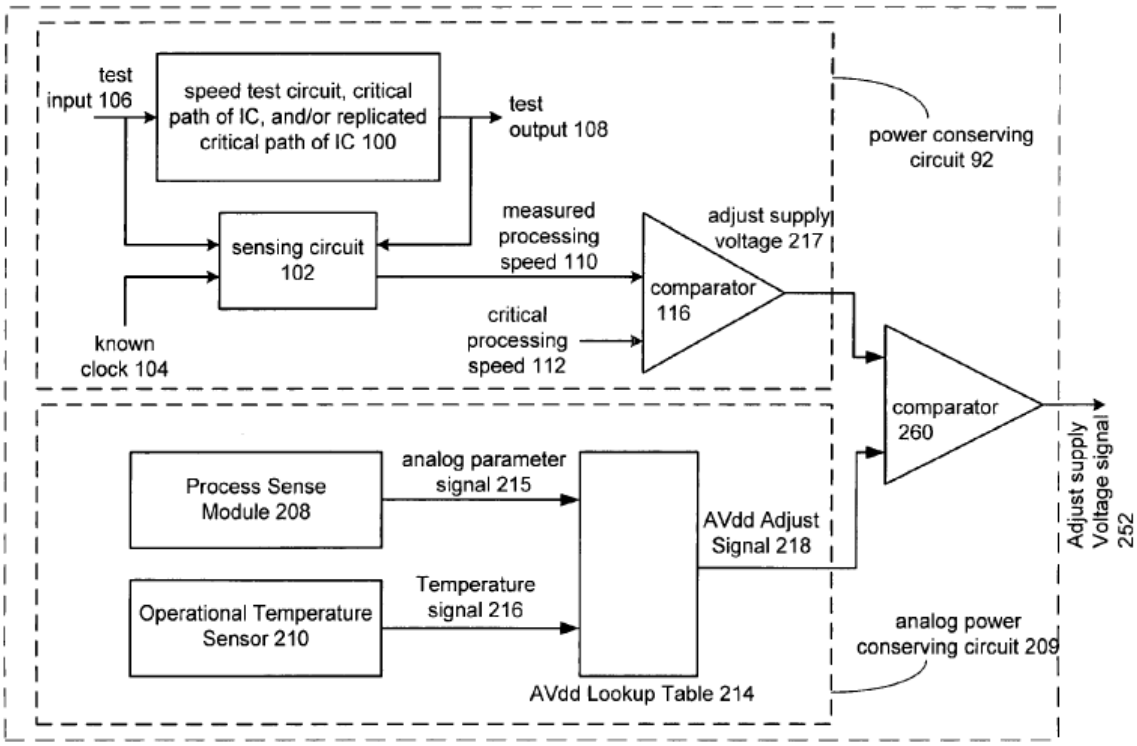

FIG. 11
power conserving circuit 250

Figure 11, above, depicts power conserving circuit 250 that provides "adjust supply voltage signal 252" for a shared voltage source supplying power to the analog and the digital circuitry of battery-optimized system on chip 62. *Id.* at 14:26–30. Power conserving circuit 250 has "digital circuitry power optimization-power conserving circuit 92" and "analog circuitry power optimization-analog power conservation circuit 209." *See id.* at 14:31–35.

Analog power conserving circuit 209 includes "a portion of an IC," "process sense module 208," "operational temperature sensor 210," and look-up table 214. *Id.* at 12:17–20. In operation, process sense module 208

senses the analog variation parameter of the IC portion and provides analog parameter signal 215. *Id.* at 12:23–25. A "suitable value used for assessing the analog variation parameter is the threshold voltage Vt of the IC." *Id.* at 10:63–65. The analog variation parameter can be assessed by measuring the gate voltage of a transistor at a point where a specific small drain current flows. *Id.* at 11:2–5. Operational temperature sensor 210 senses the operational temperature of an IC 100 portion and provides temperature signal 216. *Id.* at 12:25–27. Look-up table 214 receives analog variations parameter signal 215 and temperature signal 216, and using this information, generates analog voltage level (AV_{dd}) adjust signal 218. *Id.* at 12:50–53, 15:5–6. Digital power conserving circuit 92 provides an adjust signal for a supply voltage on a chip-by-chip basis such that the speed of a transistor is maintained at a rate just above the critical speed. *Id.* at 10:36–66.

Comparator 260 receives inputs from analog power conserving circuit 209 (i.e., analog voltage level (AV_{dd}) adjust signal 218) and from digital power conserving circuit (i.e., adjust supply voltage 217). *Id.* at 14:35–36. Based on those inputs, comparator 260 selects adjust supply signal 252. *Id.* at 14:39–50.

D. Challenged Claims

Of the challenged claims, claims 1, 8, and 18 are independent. Claim 1 is representative and is reproduced below.

> 1. A method for power supply optimization of an integrated circuit, comprising:
>
> determining an analog variation parameter representative of an integrated circuit fabrication process variance of the integrated circuit;
>
> determining an operational temperature associated with the analog variation parameter, and

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