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(54) **POWER OPTIMIZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATED CIRCUIT**

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 G01K 1/00 (2006.01)

(52) **U.S. Cl.** **702/130**

(58) **Field of Classification Search** 702/130, 702/117, 121, 124, 60, 64; 377/19, 20; 438/14, 438/17, 18
 See application file for complete search history.

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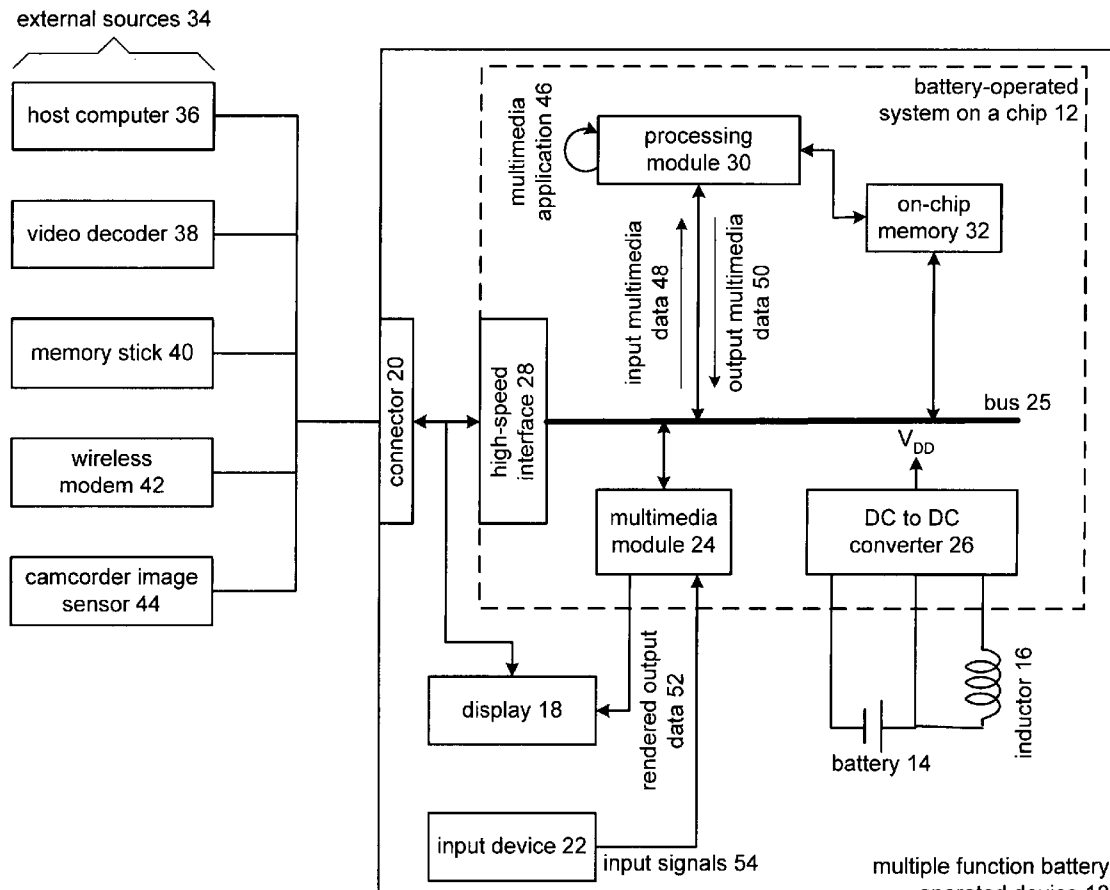
(57) **ABSTRACT**

A method and apparatus for conserving power of a mixed-signal system-on-a-chip having analog circuitry, involving determination of an analog variation parameter that is representative of an integrated circuit fabrication process variance of the integrated circuit, and an operational temperature associated with the analog variation parameter. With the analog variation parameter and the operational temperature, an adjustment signal is determined for a power supply level of the integrated circuit, such that power consumption of the integrated circuit is optimized. Further, in mixed-signal integrated circuits with digital and analog circuitry, a digital variation parameter is determined, where the adjustment signal determination is based on the digital variation parameter and the analog variation parameter with respect to the operational temperature. With such a method and apparatus, power consumption is optimized on an IC-by-IC basis such that power consumption of each IC is optimized.

21 Claims, 10 Drawing Sheets
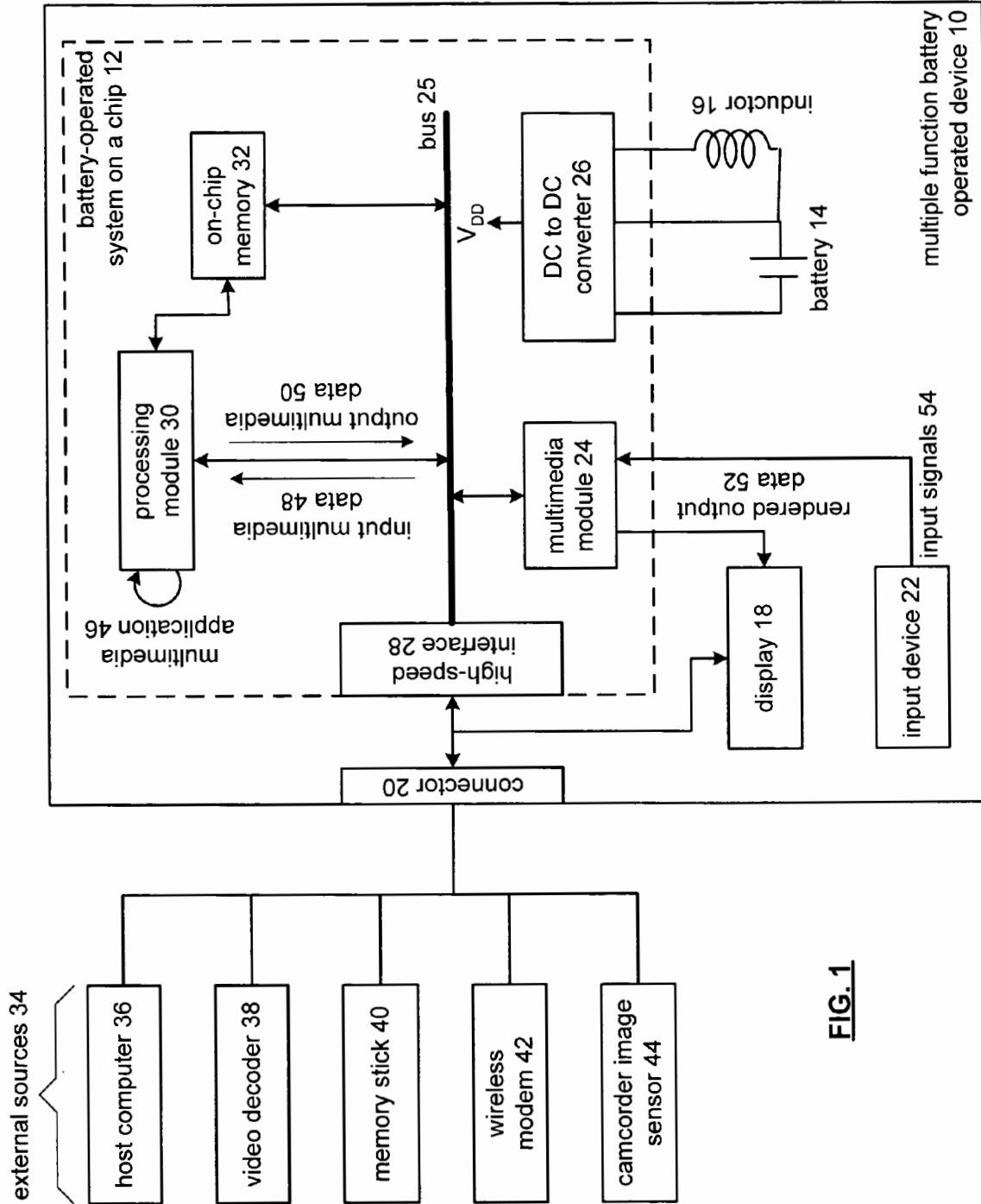
FIG. 1
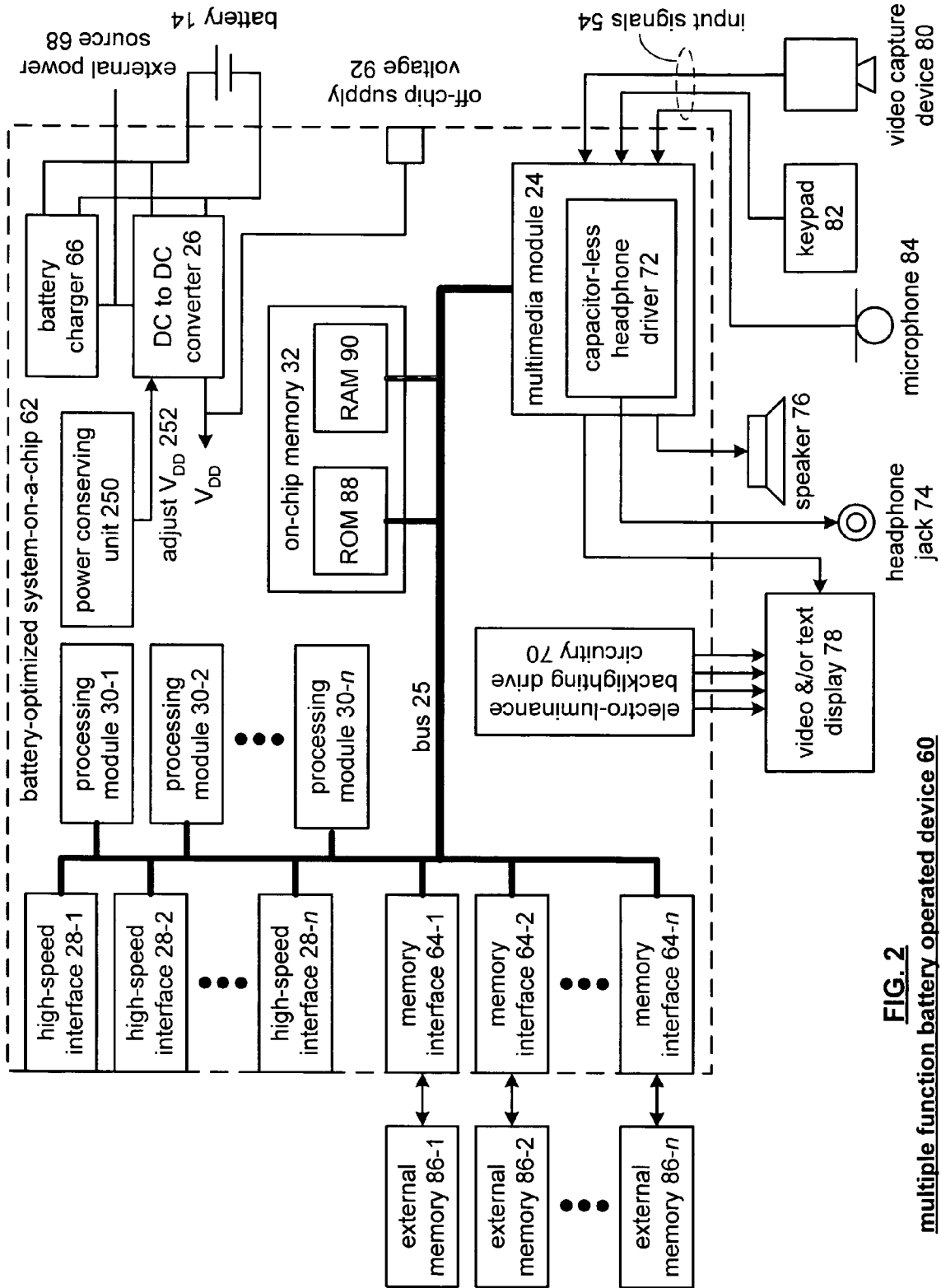
FIG. 2
multiple function battery operated device 60

integrated circuit 100

adjust supply voltage 114

comparator 116

test output 108

measured processing speed 110

critical processing speed 112

speed test circuit, critical path of IC, and/or replicated critical path of IC 100

sensing circuit 102
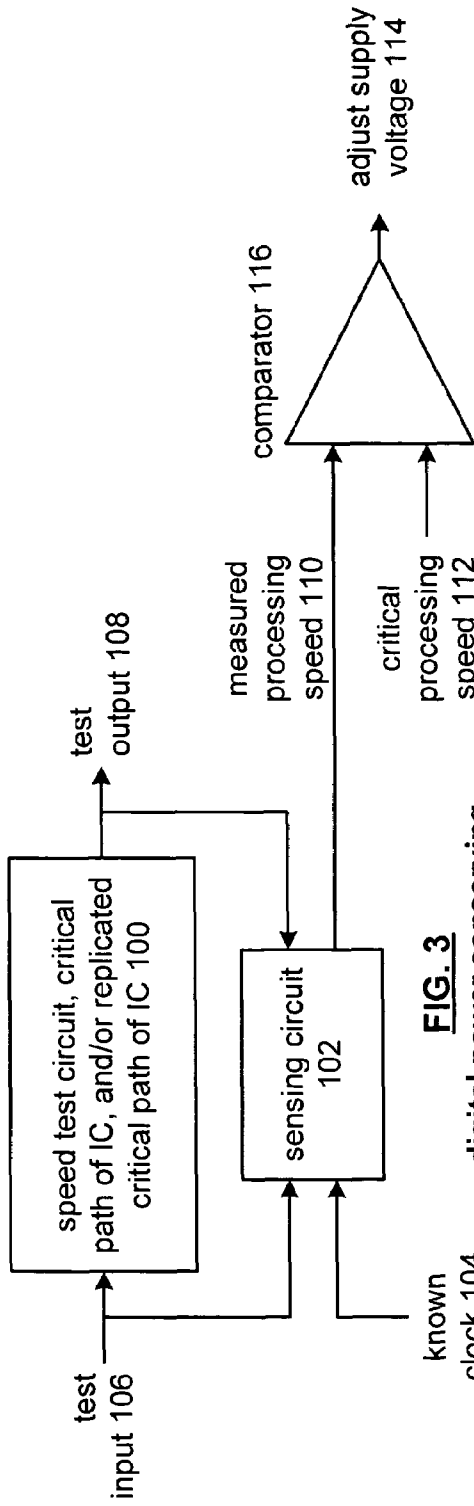
FIG. 3
digital power conserving circuit 92

test input 106

known clock 104

IC power consumption

supply voltage

FIG. 5

transistor speed

min temp

nom

max temp

critical speed

supply voltage

V_{DDmax}

V_{DDnom}

V_{DDmin}

FIG. 4

130

perform a function by the at least a portion of the integrated circuit

132

count a number of cycles of a known clock during the performing of function

134

equate the number of cycles of the known clock to the processing speed

start

120

measure processing speed of at least a portion of an integrated circuit to produce measured processing speed

122

compare the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit

124

comparison favorable?

no

126

maintain supply voltage setting

yes

128

adjust supply voltage to the integrated circuit to reduce power consumption of the integrated circuit.
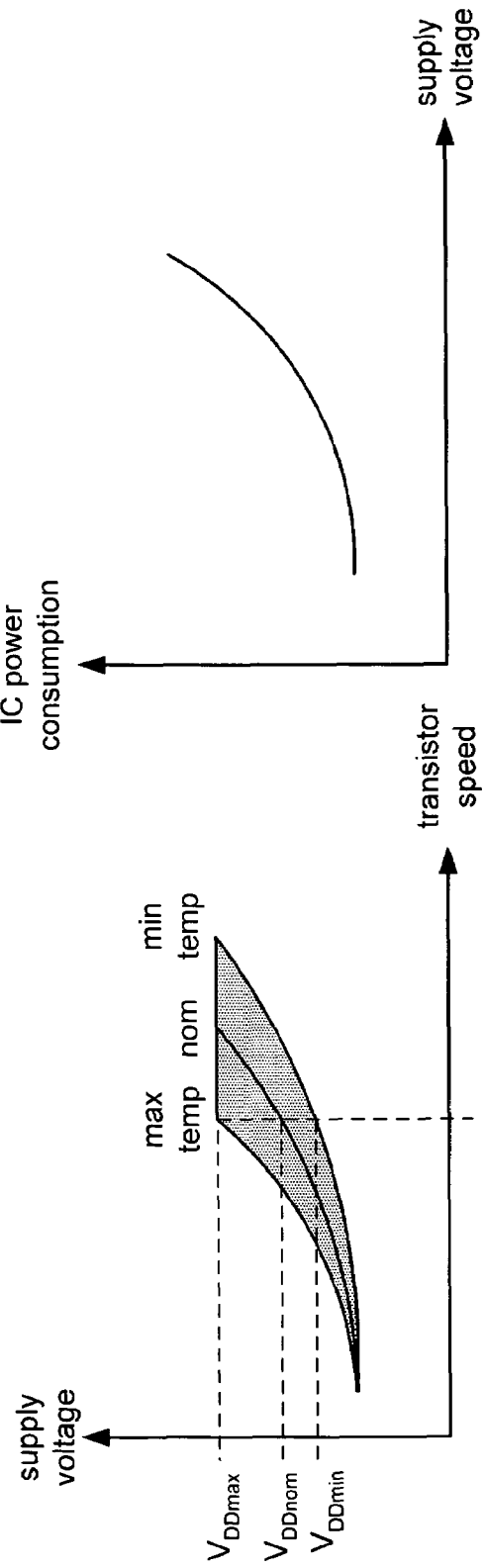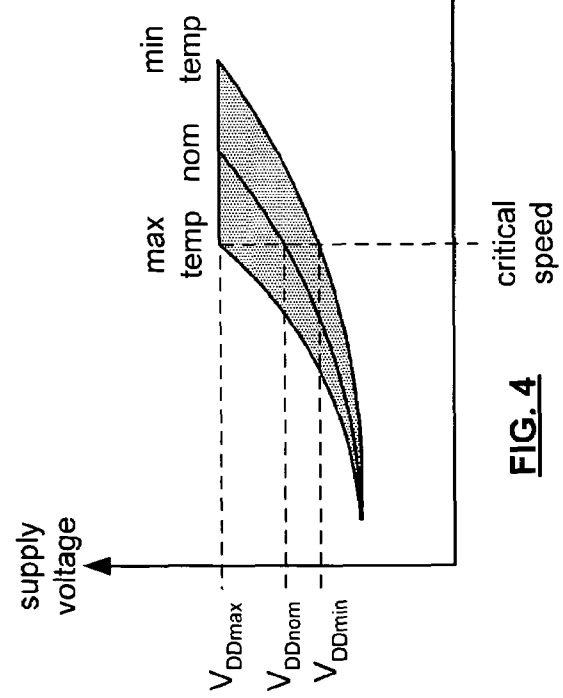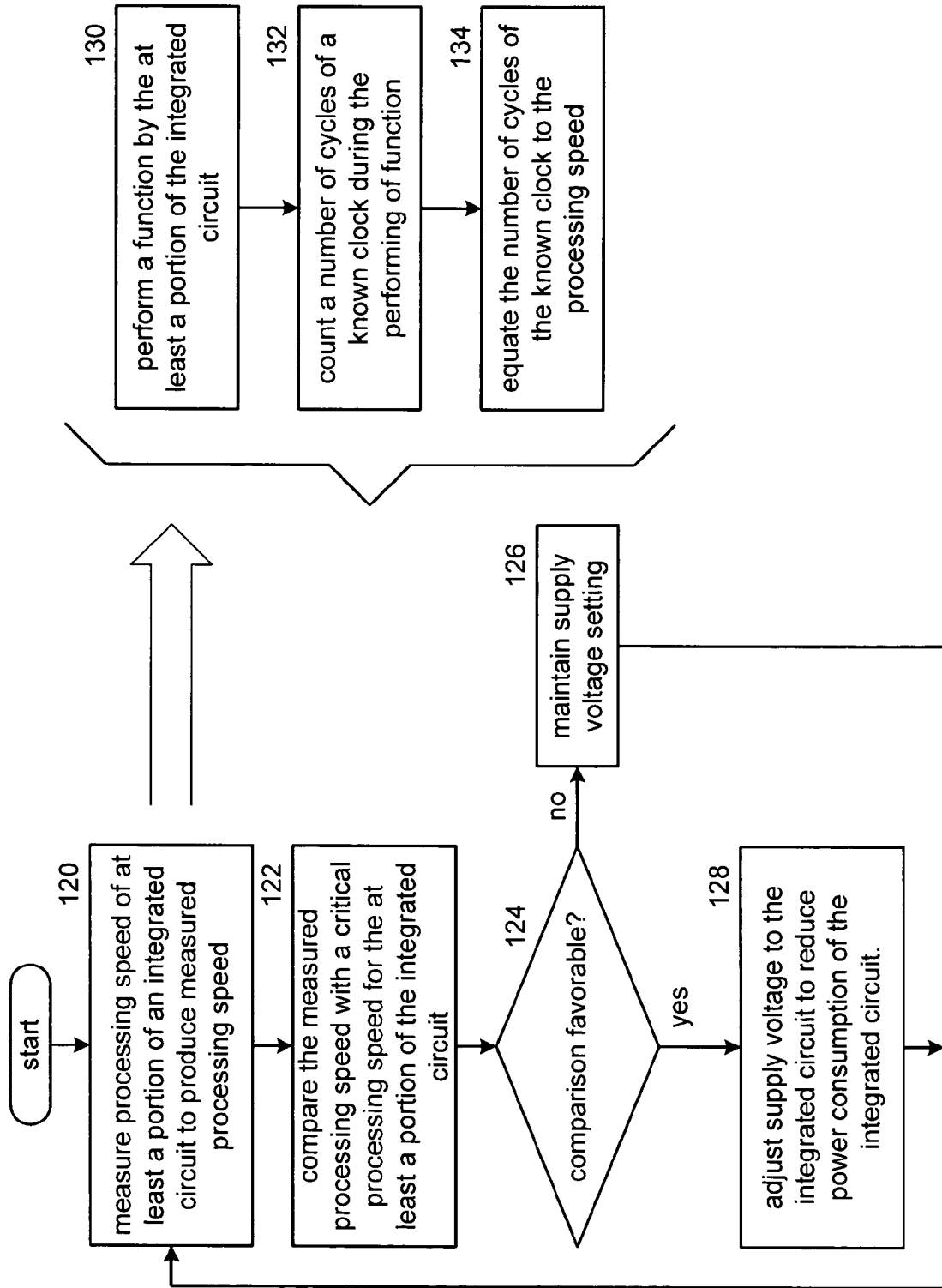
FIG. 6

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