

D.I. 133 (VLSI letter to the Court dated April 12, 2019); D.I. 136 (April 22, 2019 Memorandum Order).

As VLSI explained in connection with the April 3, 2019 Status Conference, all of the Asserted Claims identified by VLSI in its disclosures pursuant to Paragraph 4(c) of the Delaware Default Standard for Discovery (“Paragraph 4(c) Disclosures”) each present “unique issues as to liability or damages.” *In re Katz Interactive Call Processing Patent Litig.*, 639 F.3d 1303, 1312 (Fed. Cir. 2011). Among other things, VLSI demonstrated that each such Asserted Claim presents “unique questions of validity or infringement.” *Id.* at 1313 (explaining that a unique issue as to liability may be a noninfringement or invalidity defense that “does not apply in substantially the same manner” to other asserted claims); D.I. 119-1 at 2-16 (VLSI slides demonstrating unique noninfringement and invalidity issues). VLSI maintains that its due process rights will be violated if VLSI’s rights as to any of the Asserted Claims are adjudicated in this litigation without the Court permitting VLSI to assert all such Asserted Claims at trial. *See Nuance Commcn’s, Inc. v. ABBYY USA Software House, Inc.*, 813 F.3d 1368, 1376 (Fed. Cir. 2016) (explaining that, “had the patentee shown the district court that the excluded claims present unique legal issues, these claims’ exclusion could violate due process.”) (citing *Katz*, 639 F.3d at 1312-13).

Additionally, as VLSI explained in connection with the April 3, 2019 Status Conference, Intel’s noninfringement and invalidity contentions have been severely deficient, thus inhibiting VLSI’s ability to reliably determine which of its Asserted Claims may be stronger than others. *See, e.g.*, D.I. 119-1 at 17-25. Intel’s compliance with its discovery obligations has also been severely deficient, and numerous discovery disputes are in progress and/or are the subject of ongoing correspondence between the parties (which VLSI hereby incorporates by reference).

Court ordered case narrowing thus violates VLSI's due process rights for this additional reason, because VLSI presently lacks the information needed to make informed decisions regarding which Asserted Claims to include in the ordered identification of 25 claims. *See Katz*, 639 F.3d at 1313 n.9 (noting that "a claim selection order could come too early in the discovery process, denying the plaintiff the opportunity to determine whether particular claims might raise separate issues of infringement or invalidity in light of the defendants' accused products and proposed defenses.").

Accordingly, VLSI expressly reserves all rights to, at a later date, seek to assert at trial in this litigation any and/or all of the Asserted Claims that VLSI identified in its Paragraph 4(c) Disclosures. *See also* D.I. 136, Memorandum Order at 2 n.1 ("Plaintiff may seek to add at a later date asserted claims . . . upon a showing of good cause that includes a demonstration that the addition of the proposed new claims . . . is necessary to vindicate [VLSI's] due process rights.").

All rights are expressly reserved.

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Respectfully submitted,

FARNAN LLP

/s/ Brian E. Farnan

Brian E. Farnan (Bar No. 4089)
Michael J. Farnan (Bar No. 5165)
919 N. Market St., 12th Floor
Wilmington, DE 19801
Telephone : (302) 777-0300
Fax : (302) 777-0301
bfarnan@farnanlaw.com
mfarnan@farnanlaw.com

Morgan Chu (admitted *pro hac vice*)
Ben Hattenbach (admitted *pro hac vice*)
Iian D. Jablon (admitted *pro hac vice*)
Christopher Abernethy (admitted *pro hac vice*)

Amy E. Proctor (admitted *pro hac vice*)
Dominik Slusarczyk (admitted *pro hac vice*)
S. Adina Stohl (admitted *pro hac vice*)
Leah Johannesson (admitted *pro hac vice*)
Charlotte J. Wen (admitted *pro hac vice*)
IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067
Telephone: (310) 277-1010
Facsimile: (310) 203-7199
mchu@irell.com
bhattanbach@irell.com
ijablon@irell.com
cabernethy@irell.com
aproctor@irell.com
dslusarczyk@irell.com
astohl@irell.com
ljohannesson@irell.com
cwen@irell.com

Attorneys for VLSI Technology LLC

CERTIFICATE OF SERVICE

I, Brian E. Farnan, hereby certify that on April 26, 2019, a copy of Plaintiff VLSI Technology LLC's Initial Identification of Asserted Patent Claims Pursuant to the Court's April 22, 2019 Memorandum Order (D.I. 136) was served on the following as indicated:

Via E-Mail

Jack B. Blumenfeld
Jeremy A. Tigan
Morris, Nichols, Arsht & Tunnell LLP
1201 North Market Street
P.O. Box 1347
Wilmington, DE 19899
jblumenfeld@mnat.com
jtigan@mnat.com

Attorneys for Defendant Intel Corporation

Via E-Mail

Mark N. Reiter
Omar F. Amin
GIBSON, DUNN & CRUTCHER LLP
mreiter@gibsondunn.com
oamin@gibsondunn.com

Attorneys for Defendant Intel Corporation

Via E-Mail

Jordan L. Hirsch
William F. Lee
Amanda L. Major
David C. Marcus
Mark D. Selwyn
Louis W. Tompros
Kathryn Zalewski
Liv Herriot
WILMER CUTLER PICKERING
HALE AND DORR LLP
jordan.hirsch@wilmerhale.com
william.lee@wilmerhale.com
amanda.major@wilmerhale.com
david.marcus@wilmerhale.com
mark.selwyn@wilmerhale.com
louis.tompros@wilmerhale.com
kathryn.zalewski@wilmerhale.com
liv.herriot@wilmerhale.com

Attorneys for Defendant Intel Corporation

/s/ Brian E. Farnan

Brian E. Farnan (Bar No. 4089)