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Paper No. 46
Entered: March 10, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

TELA INNOVATIONS, INC.,
Patent Owner.

IPR2019-01637
Patent 10,141,335 B2

Before JO-ANNE M. KOKOSKI, KRISTINA M. KALAN, and WESLEY B. DERRICK, *Administrative Patent Judges.*

KALAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision

Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Intel Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting *inter partes* review of claims 1–11, 15, 18, 20, and 22–24 of U.S. Patent No. 10,141,335 B2 (Ex. 1001, "the '335 patent"). Tela Innovations, Inc. ("Patent Owner") filed a Preliminary Response to the Petition. Paper 11. We authorized additional briefing on the issues set forth in the Preliminary Response. Paper 13. Petitioner in turn filed a Reply to Patent Owner's Preliminary Response (Paper 14) and Patent Owner filed a Sur-Reply to Petitioner's Preliminary Reply (Paper 15).

We instituted an *inter partes* review of claims 1–11, 15, 18, 20, and 22–24 of the '335 patent on the ground of unpatentability alleged in the Petition. Paper 16 ("Dec."). After institution of trial, Patent Owner filed a Patent Owner Response. Paper 28 ("PO Resp."). Petitioner filed a Reply. Paper 35 ("Reply"). Patent Owner filed a Sur-Reply. Paper 38 ("Sur-Reply"). An oral hearing was held on December 9, 2020, and a transcript of the hearing is included in the record. Paper 45 ("Tr.").

This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–11, 15, 18, 20, and 22–24 of the '335 patent are unpatentable.

A. Related Proceedings

The parties state that the '335 patent is at issue in a number of proceedings, including *Intel Corp. v. Tela Innovations, Inc.*, No. 3:18-cv-02848-WHO (N.D. Cal.) (the "NDCA Action"). Pet. 3–5, Paper 5, 2. The parties also state that the '335 patent was at issue in an International Trade Commission ("ITC") investigation, Inv. No. 337-TA-1148 (the "ITC

Proceeding"), but was later terminated from the ITC Proceeding. Pet. 3; PO Resp. 3.

B. The '335 Patent

The '335 patent, titled "Semiconductor Cip [sic] Including Region Having Rectangular-Shaped Gate Structures and First-Metal Structures," is directed to an integrated circuit. Ex. 1001, code (54), 4:37–39. The '335 patent explains that a push for circuit chip area reduction in the semiconductor industry has resulted in improvements in the lithographic process that enable smaller feature sizes to be achieved. *Id.* at 3:60–4:4. In the evolution of lithography, the minimum feature size approached, and subsequently reached a scale less than, the wavelength of the light source used to expose the feature shapes, leading to unintended interactions between neighboring features. *Id.* at 4:5–8. The '335 patent defines the difference between the minimum feature size and the wavelength of light as the lithographic gap. *Id.* at 4:11–13. The '335 patent further describes that an interference pattern occurs as each shape on the mask interacts with the light. *Id.* at 4:16–17. The interference patterns from neighboring shapes can create constructive or destructive interference. *Id.* at 4:17–19. In view of the foregoing, the '335 patent identifies a need for a solution that manages lithographic gap issues as technology continues to progress toward smaller semiconductor device feature sizes. *Id.* at 4:30–33.

The '335 patent describes that a dynamic array architecture is provided to address semiconductor manufacturing process variability associated with a continually increasing lithographic gap. *Id.* at 8:62–65. Figure 2 of the '335 patent, shown below, illustrates a generalized stack of layers used to define a dynamic array architecture.

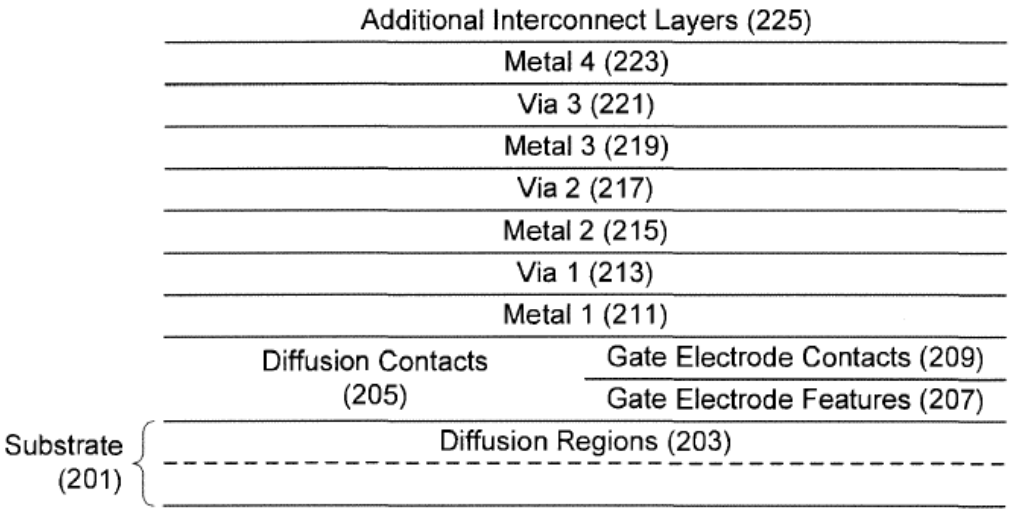

Fig. 2

Figure 2 depicts the generally underlying structure of a dynamic array. *Id.* at 11:4–18. The dynamic array is built up in a layered manner upon base substrate 201 (e.g., a silicon substrate or silicon-on-insulator (SOI) substrate). *Id.* at 11:20–22. Diffusion regions 203 are defined in base substrate 201 and represent selected regions of base substrate 201 within which impurities are introduced for the purpose of modifying the electrical properties of base substrate 201. *Id.* at 11:22–27. Above diffusion regions 203, diffusion contacts 205 are defined to enable connection between diffusion regions 203 and conductor lines. *Id.* at 11:27–29. Gate electrode features 207 are defined above diffusion regions 203 to form transistor gates. *Id.* at 11:32–34. Gate electrode contacts 209 are defined to enable connection between gate electrode features 207 and conductor lines. *Id.* at 11:34–36. Interconnect layers are defined above diffusion contact 205 layer and gate electrode contact layer 209. *Id.* at 11:39–40. The interconnect layers include first metal (metal 1) layer 211, first via (via 1)

layer 213, second metal (metal 2) layer 215, second via (via 2) layer 217, third metal (metal 3) layer 219, third via (via 3) layer 221, and fourth metal (metal 4) layer 223. *Id.* at 11:40–45.

Figure 5 of the '335 patent is shown below:

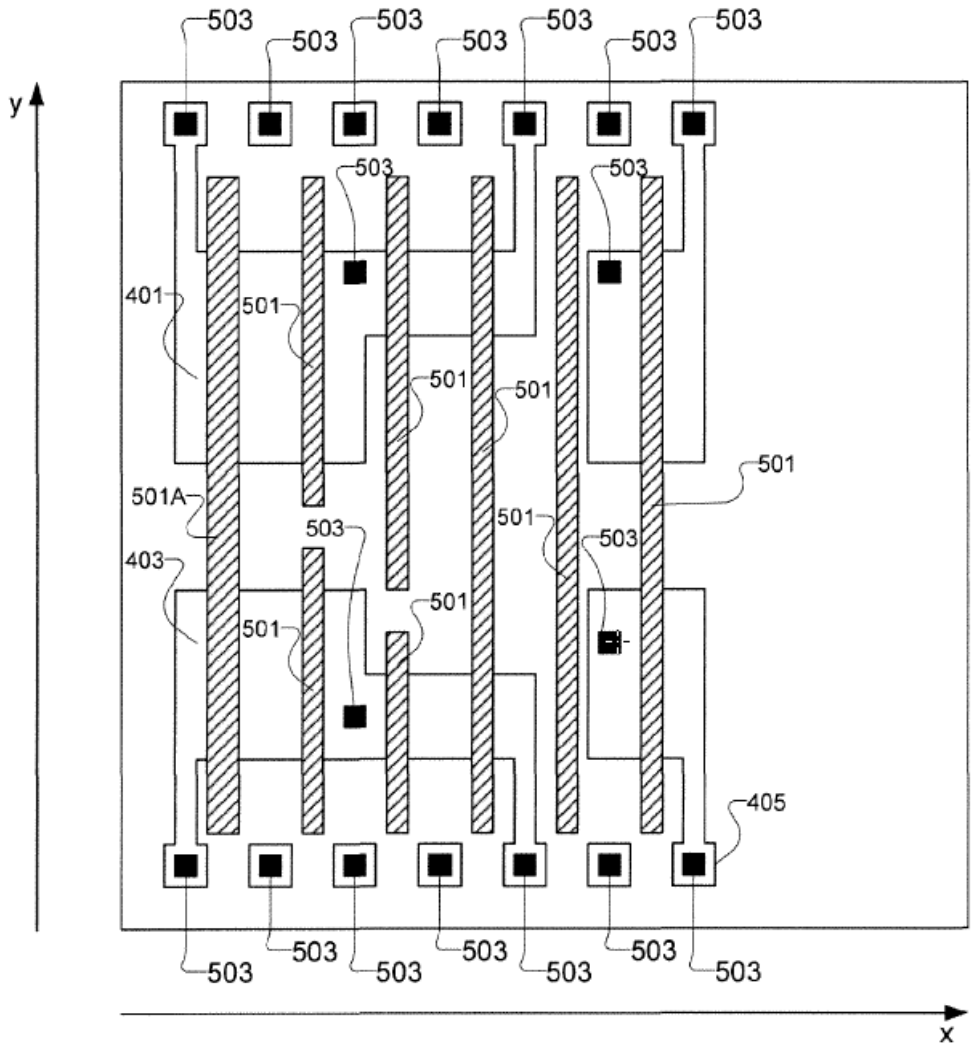

Fig. 5

Figure 5 illustrates an exemplary layout of a dynamic array that includes a gate electrode layer, a diffusion contact layer, and a diffusion layer. *Id.* at 16:10–13. The diffusion layer shows p-diffusion region 401 and n-

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