UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

INTEL CORPORATION,

Plaintiff,

v.

TELA INNOVATIONS, INC.,

Defendant.

Case No. 3:18-cv-02848-WHO

CLAIM CONSTRUCTION ORDER

Re: Dkt. No. 163

Before me are six patents from the same patent family, all assigned to declaratory judgment defendant Tela Innovations, Inc., and all asserted against plaintiff Intel Corporation. The patented technology aims to improve the design and manufacturability of integrated circuits by ameliorating difficulties associated with the lithographic gap, or the size difference between ever-shrinking semiconductor features and the wavelength of light used to fabricate them. The parties have asked me to construe seven terms from the asserted claims. My constructions are below.

BACKGROUND

Between November 4, 2008 and January 22, 2019, the United States Patent and Trademark Office ("PTO") issued United States Patent Nos. 7,446,352 ("the '352 Patent"), 7,943,966 ("the '966 Patent"), 7,948,012 ("the '012 Patent"), 10,141,334 ("the '334 Patent"), 10,141,335 ("the '335 Patent"), and 10,186,523 ("the '523 Patent") (collectively, the "patents in suit"). *See* Declaration of Frank Liu ("Liu Decl."), Exs. 1-6 [Dkt. Nos. 166-2, 166-3, 166-4, 166-5, 166-6, 166-7]. All of the patents in suit are part of the same patent family, all claim priority to Provisional Application No. 60/781,288, filed on March 9, 2006, and all list Tela as the sole assignee.

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Intel filed this declaratory judgment action on May 15, 2018.[1] Dkt. No. 1. Since that time, I have resolved a motion to transfer, several motions to dismiss and strike, a disputed motion for a protective order, and several discovery disputes. *See* Dkt. Nos. 64, 70, 86, 162. The parties briefed claim construction starting on June 13, 2019, and each submitted an electronic technology tutorial in advance of the claim construction hearing. *See* Dkt. Nos. 163, 173. After providing the parties with my tentative opinions, I heard argument on September 27, 2019. Dkt. Nos. 172, 173.

LEGAL STANDARD

Claim construction is a matter of law. *See Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). "Generally, a claim term is given its ordinary and customary meaning—the meaning that a term would have to a person of ordinary skill in the art in question at the time of the invention." *Howmedica Osteonics Corp. v. Zimmer, Inc.*, 822 F.3d 1312, 1320 (Fed. Cir. 2016) (internal quotation marks and citation omitted). In determining the proper construction of a claim, a court begins with the intrinsic evidence of record, consisting of the claim language, the patent specification, and, if in evidence, the prosecution history. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005); *see also Vitronics*, 90 F.3d at 1582. "A claim term used in multiple claims should be construed consistently . . . ." *Inverness Med. Switzerland GmbH v. Princeton Biomeditech Corp.*, 309 F.3d 1365, 1371 (Fed. Cir. 2002).

"The appropriate starting point . . . is always with the language of the asserted claim itself." *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1312. "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

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Such redefinition or disavowal need not be express to be clear. *Trustees of Columbia Univ. in City of New York v. Symantec Corp.*, 811 F.3d 1359, 1364 (Fed. Cir. 2016).

Courts read terms in the context of the claim and of the entire patent, including the specification. *Phillips*, 415 F.3d at 1313. The specification is "the single best guide to the meaning of a disputed term." *Vitronics*, 90 F.3d at 1582. "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). The court may also consider the prosecution history of the patent, if in evidence. *Markman*, 52 F.3d at 980. The prosecution history may "inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317 (citing *Vitronics*, 90 F.3d at 1582-83); *see also Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.") (internal quotations omitted).

In most situations, analysis of the intrinsic evidence alone will resolve claim construction disputes, *Vitronics*, 90 F.3d at 1583; however, a court can further consult "trustworthy extrinsic evidence" to compare its construction to "widely held understandings in the pertinent technical field," *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1309 (Fed. Cir. 1999). Extrinsic evidence "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Markman*, 52 F.3d at 980. All extrinsic evidence should be evaluated in light of the intrinsic evidence, *Phillips*, 415 F.3d at 1319, and courts should not rely on extrinsic evidence in claim construction to contradict the meaning of claims discernible from examination of the claims, the written description, and the prosecution history, *Pitney Bowes*, 182 F.3d at 1308 (citing *Vitronics*, 90 F.3d at 1583).

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DISCUSSION

I. THE TECHNOLOGY

The patents at issue aim to improve the design and manufacturability of integrated circuits by creating solutions to manage the lithographic gap. '352 Patent 1:49-51. Integrated circuit chips are the building blocks of devices like computers, smart phones, and tablets, and transistors are the building blocks of integrated circuit chips. Today, a single integrated circuit chip includes billions of transistors, which form the bottom layer of the chip, connected to the layers above by metal interconnects. Transistors are effectively switches that control the flow of electrical current through a circuit.

Transistors are made up of a substrate, a source region, a drain region, and a gate. A semiconductor material forms the substrate. The source and drain regions have the same charge, either positive or negative, which is created by introducing impurities during the fabrication process. The transistor gate can be made of metal or polysilicon. Voltage applied to the transistor gate determines whether a channel forms underneath the gate, allowing charge to flow between the source and drain regions. When the opposite charge is applied to the gate, a current begins to flow through the substrate between the source and drain regions (i.e., the transistor is "on").

Fabrication of integrated circuits occurs one layer at a time, beginning with the bottom transistor layer, known as the front end. To fabricate transistors, different materials are added, altered, and removed until the desired features are present. The Asserted Patents are primarily directed to one tool used during fabrication, called photolithography, or lithography. Lithography is used to create a specific pattern of gates on the substrate. Once the gate material has been deposited onto the substrate, a material called photoresist, which is sensitive to light, is placed on top.[2] A light is shone through a patterned mask, altering the chemical nature of the photoresist that it reaches and creating the desired pattern. When the photoresist is developed, depending on what type of photoresist was used, either the parts that were exposed to light or the parts that were not exposed to light will remain. The exposed gate material, i.e. without photoresist on top, is

[2] This account given in this Order does not detail every step involved in semiconductor

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chemically etched away, leaving the desired gate pattern. Finally, ashing removes the remaining photoresist.

When transistors are too close, they can electrically interfere with one another. With up to billions of transistors on a single chip, they might be separated by only the space of only one one-hundredth of a human hair. Despite this proximity, there are a few ways to prevent transistors from interfering with one another. Dummy gates, which lack source and drain regions, can separate transistors. In addition, field oxide can be used as an insulator to cover the portions of the substrate that do not have active transistors, and gates can be formed on top of the field oxide.

At the time of the '352 Patent, transistor feature sizes had decreased and were approaching 45 nm (nanometers).[3] '352 Patent 1:27-30. Because those feature sizes are smaller than the wavelength of light, unintended interactions can occur between neighboring features during lithography. *See id.* at 1:24-27. Specifically, unwanted shapes may be created (constructive interference) or desired shapes may be removed (destructive interference). *Id.* 1:35-41. The patented technology aims to create a solution "for managing lithographic gap issues as technology continues to progress toward smaller semiconductor device features sizes." *Id.* at 1:49-51.

II. CLAIM CONSTRUCTION

The parties agree on the construction of the following two terms:

Claim Term	Agreed Construction
"diffusion region"	selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor
"a lithography process"	plain and ordinary meaning, *i.e.*, a process by which a pattern is imprinted on a resist or semiconductor wafer using light using a mask

Joint Claim Construction and Prehearing Statement [Dkt. No. 163] 2. The parties dispute seven terms, and I construe them as follows.

[3] Also at the time of the '352 Patent, improvement in chemical mechanical polishing (CMP) allowed more interconnect layers to be stacked together. *Id.* at 1:21-23. The topology of the different interconnect layers can limit how many layers can be stacked together because "islands, ridges, and troughs can cause breaks in the interconnect lines that cross them." *Id.* at 17:13-22. CMP can help flatten the surface of the semiconductor wafer to facilitate stacking. *Id.* at 17:23-

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