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This Declaration relates to the dates of receipt and availability of the following:

Thurber, K. J., & Wald, L. D. (1975). *Associative and parallel processors*. *ACM Computing Surveys*, 7(4), 215–255.

Standard operating procedures for materials at the University of Wisconsin-Madison Libraries. When an issue was received by the Library, it would be checked in, stamped with the date of receipt, added to library holdings records, and made available to readers as soon after its arrival as possible. The procedure normally took a few days or at most 2 to 3 weeks.

Exhibit A to this Declaration is true and accurate copy of the issue cover with library date stamp of *ACM Computing Surveys* (1975), from the University of Wisconsin-Madison Library collection. Exhibit A also includes an excerpt of pages 215 to 255 of that issue, showing the article entitled *Associative and parallel processors*

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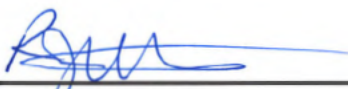
(1975). Based on this information, the date stamp on the journal title page indicates *Associative and Parallel Processors* (1975) was received by the Engineering Library at the University of Wisconsin-Madison on February 25, 1976.

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COMPUTING SURVEYS

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Associative and Parallel Processors

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This paper is a tutorial survey of the area of parallel and associative processors. The paper covers the main design tradeoffs and major architectures of SIMD (Single Instruction Stream Multiple Data Stream) systems. Summaries of ILLIAC IV, STARAN, OMEN, and PEPE, the major SIMD processors, are included.

Keywords and Phrases: associative processor, parallel processor, OMEN, STARAN, PEPE, ILLIAC IV, architecture, large-scale systems, SIMD processors, array processors, ensemble.

CR Categories: 3.80, 4.20, 6.22

INTRODUCTION

Purpose and Scope

The purpose of this paper is to present a tutorial survey on the subject of parallel and associative processors. The paper covers the topics of system categorizations, applications, main tradeoff issues, historically important architectures, and the architectures of systems that are currently available.

Currently, the microprocessor/computer-on-a-chip revolution is providing the potential for production of very cost-effective high-performance computers through utilization of a large number of these processors in parallel or in a network. The parallel and associative processors provide a class of architectures which can be readily used to take immediate advantage of the microprocessor technology.

Surveys

A number of good surveys on the subject (or bordering on the subject) of parallel and asso-

ciative processors have been published [1-10]. Some of these surveys are only of historical interest due to their age. Several conferences in this area may also be of interest [11-14].

Classification of Computer Architectures

Many approaches to classification of computer architectures are possible. Most techniques use global architecture properties and are thus valid only within limited ranges. The main classification techniques discussed below provide a framework within which to view associative and parallel processors.

Flynn [15] proposed a classification scheme that divides systems into categories based upon their procedure and data streams. The four categories are:

- 1) SISD (Single Instruction Stream Single Data Stream) – a uniprocessor such as a single processor IBM 360.
- 2) MISD (Multiple Instruction Stream Single Data Stream) – a pipeline processor such as CDC STAR.

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