

**IN THE UNITED STATES DISTRICT COURT  
FOR THE DISTRICT OF DELAWARE**

PACT XPP SCHWEIZ AG

Plaintiff,

v.

INTEL CORPORATION

Defendant.

Case No. \_\_\_\_\_

**JURY TRIAL DEMANDED**

**COMPLAINT**

Plaintiff PACT XPP Schweiz AG, for its Complaint against Intel Corporation (“Intel” or “Defendant”), hereby alleges as follows:

**PARTIES**

1. Plaintiff PACT XPP Schweiz AG is a Swiss corporation, with its principal place of business in Switzerland. PACT XPP Schweiz AG is the assignee of all patents identified in this Complaint including all rights to sue for past and future damages for infringement of said patents.

2. Upon information and belief, Intel is a Delaware corporation with its corporate headquarters in Santa Clara, California and manufacturing facilities in Oregon, Arizona, New Mexico, Massachusetts, and numerous other countries.

3. Intel, founded in 1968, has over an 80% market share in computer processor technology, and over \$70 Billion in revenues producing \$29.4 Billion of cash from operations and returned nearly \$16.3 Billion to shareholders in 2018 based on a gross profit margin of 61.7% of revenues. Intel’s two major operating segments are the PC Client Group, which produced over \$37 Billion in revenue for 2018 and focuses on the processors found in consumer-

certain software, or the like by ODMs, OEMs, and/or end users). Based on these facts and the facts set forth in the paragraphs above, Intel infringes the '301 Patent under 35 U.S.C. § 271(f)(1) and (f)(2).

106. As a result of Intel's infringement of the '301 Patent, PACT has been damaged. PACT is entitled to recover for damages sustained as a result of Intel's wrongful acts in an amount subject to proof at trial but no less than a reasonable royalty.

107. In addition, Intel's infringing acts and practices have caused and are causing immediate and irreparable harm to PACT.

108. PACT is informed and believes, and thereon alleges, that the infringement of the '301 Patent by Intel has been and continues to be willful. As noted above, at least as of the service of this Complaint, Intel has actual knowledge of its infringement of the '301 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for PACT's patent rights. Thus, Intel's infringing actions have been and continue to be consciously wrongful, entitling PACT to increased damages under 35 U.S.C. § 284.

109. PACT is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to PACT pursuant to 35 U.S.C. § 285.

#### **COUNT IV – INFRINGEMENT OF U.S. PATENT NO. 8,471,593**

110. PACT incorporates each of the above paragraphs 1-35 as though fully set forth herein.

111. PACT is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '593 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using (including testing), offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States,

and importing into the United States, without authority or license, Intel products with the infringing features, including the Accused Core Instrumentalities and the Accused Xeon Instrumentalities.

112. For example, the Accused Core Instrumentalities and the Accused Xeon Instrumentalities embody every limitation of at least claim 1 of the '593 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

***"A data processor on a chip comprising"***

113. The Accused Core Instrumentalities and the Accused Xeon Instrumentalities are processors incorporated on a chip, thus, constitute data processor on a chip.

***"a plurality of data processing cores, each of at least some of the processing cores including:  
at least one arithmetic logic unit that supports at least division and multiplication of at least  
32-bit wide data; and at least 3 registers for storing at least 32-bit wide data"***

114. The Accused Core Instrumentalities and the Accused Xeon Instrumentalities are multi-core processors including ALUs capable of 32-bit wide division and multiplication and at least 3 general purpose registers being at least 32-bit wide.

***"a plurality of memory units to buffer at least 32-bit wide data"***

115. The Accused Core Instrumentalities and the Accused Xeon Instrumentalities include Last Level Caches with line size at least 32-bit to buffer data.

***"at least one interface unit for providing at least one communication channel between the  
data processor and external memory, and"***

116. The Accused Core Instrumentalities and the Accused Xeon Instrumentalities include a System Agent working with the ring bus system (or equivalents) for providing at least

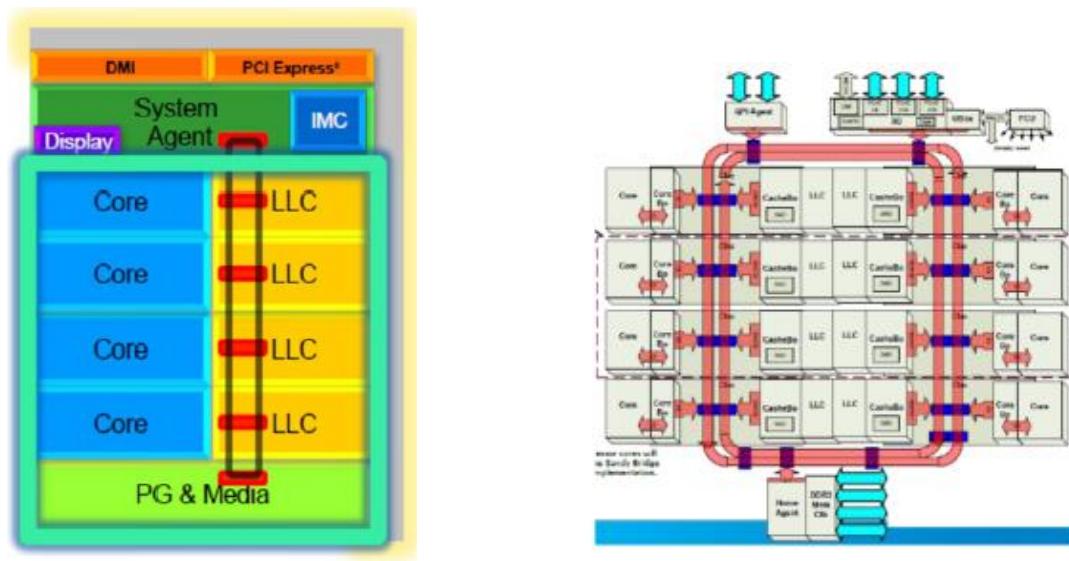
one communication channel between the core and external memory such as RAM and/or various types of DRAMs.

***“a bus system flexibly interconnecting the plurality of processing cores, the plurality of memory units, and the at least one interface”***

117. The Accused Core Instrumentalities and the Accused Xeon Instrumentalities include at least a ring bus system (or equivalents) flexibly interconnecting the cores, LLCs, and the System Agent, etc.

***“wherein: the bus system includes a first structure dedicated for data transfer in a first direction and a second structure dedicated for data transfer in a second direction, and”***

118. In the Accused Core Instrumentalities and the Accused Xeon Instrumentalities, the above identified ring bus system (or equivalents) transfers data in at least two directions with two structures as shown in the two figures below:



***“each of at least some of the data processing cores includes a physically dedicated connection to at least one physically assigned one of the plurality of memory units, the assigned one of the***

*plurality of memory units being accessible by another of the data processing cores via a secondary bus path of the bus system”*

119. In the Accused Core Instrumentalities and the Accused Xeon Instrumentalities, each core includes a physically dedicated connection to at least one physically assigned LLC as shown in the two figures above. The assigned LLC is accessible by another core via a secondary bus path of the ring bus system (or equivalents) as shown in the two figures above.

120. In violation of 35 U.S.C. § 271, Intel has infringed and is currently infringing, directly and/or through intermediaries, the '593 Patent by making, using, selling, offering for sale, and/or importing into the United States, without authority, products that practice at least claim 1 of the '593 Patent. These products include the Accused Core Instrumentalities and the Accused Xeon Instrumentalities, and any other products that incorporate the Accused Core Instrumentalities and the Accused Xeon Instrumentalities. Intel has infringed and is currently infringing literally and/or under the doctrine of equivalents.

121. On information and belief, PACT asserts that Intel was aware of this patent before this lawsuit was filed, and at least as of the service of this Complaint, Intel had actual knowledge of its infringement of the '593 Patent.

122. PACT is informed and believes, and thereon alleges, that Intel, subsequent to the time it first learned of the '593 Patent and at least as of the time of service of this Complaint, specifically intended to induce patent infringement by third-party original equipment manufacturers (OEMs), customers, and users of the Accused Core Instrumentalities and the Accused Xeon Instrumentalities and had knowledge that the inducing acts would cause infringement or is willfully blind to the possibility that their inducing acts would cause infringement. Intel has sold and continues to sell the Accused Core Instrumentalities and the

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