

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTEL CORPORATION,  
Petitioner,

v.

PACT XPP SCHWEIZ AG,  
Patent Owner.

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IPR2020-00532  
Patent 8,471,593 B2

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Before SALLY C. MEDLEY, KEN B. BARRETT, and  
CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

DECISION  
Denying Institution of *Inter Partes* Review  
35 U.S.C. § 314

## I. INTRODUCTION

### A. *Background and Summary*

Intel Corporation (“Petitioner”)<sup>1</sup> filed a Petition requesting *inter partes* review of U.S. Patent No. 8,471,593 B2 (“the ’593 patent,” Ex. 1003). Paper 2 (“Pet.”). The Petition challenges the patentability of claims 1, 2, 4–11, 14–17, and 19–27 of the ’593 patent. PACT XPP Schweiz AG (“Patent Owner”)<sup>2</sup> filed a Preliminary Response to the Petition. Paper 6 (“Prelim. Resp.”). As authorized by the Board, Petitioner filed a Reply to the Preliminary Response (Paper 9, “Pet. Reply”) and Patent Owner filed a Sur-Reply (Paper 10, “PO Sur-Reply”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing on at least one of the challenged claims of the ’593 patent. Accordingly, we do not institute an *inter partes* review of the challenged claims.

### B. *Related Proceedings*

One or both parties identify, as matters involving or related to the ’593 patent: *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-00267 (D. Del. Feb. 7, 2019); *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-00273

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<sup>1</sup> Petitioner identifies Intel Corporation as the real party-in-interest. Pet. 1.

<sup>2</sup> Patent Owner identifies PACT XPP Schweiz AG (formerly known as Scientia Sol Mentis AG) as the real party-in-interest. Paper 3, 1.

(W.D. Tex. April 23, 2019); *Intel Corp. v. PACT XPP Schweiz AG*, No. 19-cv-02241 (N.D. Cal. April 25, 2019); and *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-01006<sup>3</sup> (D. Del. May 30, 2019). Pet. 2; Paper 3, 1–2.

### C. *The '593 Patent*

The '593 patent pertains to logic cell arrays. Ex. 1003, 1:18. According to the patent, “[o]ne of the difficulties with conventional systems is that a large number of cells have to communicate with each other . . . [and t]he communication may be required in order to pass the data to be processed from one cell to another.” *Id.* at 1:51–55. Also, certain conventional bus systems “become[] problematic when a great many communicating units need access to the bus or busses.” *Id.* at 1:66–2:6. The patent describes a “bus system [that] includes different segment lines having shorter and longer segments for connecting two points in order to be able to minimize the number of bus elements traversed between separate communication start and end points.” *Id.* at 2:38–44. The '593 patent explains that, by configuring the bus using long segments “that are fashioned as a single line for bypassing long paths in a logic cell array, an especially simple design and an especially efficient operation result . . . [and b]y simultaneously providing short segment lines, it is ensured that all points are addressable as needed.” *Id.* at 2:45–50.

### D. *The Challenged Claim*

Of the challenged claims of the '593 patent, claims 1 and 16 are independent claims. The remaining challenged claims depend directly or

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<sup>3</sup> Patent Owner identified the case as “19-1066.” Paper 3, 2 (underlining added). We understand that to contain a typographical error.

indirectly from claim 1 or claim 16. Claim 1, reproduced below with emphasis added, is illustrative.

1. A data processor on a chip comprising:
    - a plurality of data processing cores, each of at least some of the processing cores including:
      - at least one arithmetic logic unit that supports at least division and multiplication of at least 32-bit wide data; and
      - at least 3 registers for storing at least 32-bit wide data;
    - a plurality of memory units to buffer at least 32-bit wide data;
    - at least one interface unit for providing at least one communication channel between the data processor and external memory; and
    - a bus system flexibly interconnecting the plurality of processing cores, the plurality of memory units, and the at least one interface;
- wherein:
- the bus system includes a first structure dedicated for data transfer in a first direction and a second structure dedicated for data transfer in a second direction; and*
  - each of at least some of the data processing cores includes a physically dedicated connection to at least one physically assigned one of the plurality of memory units, the assigned one of the plurality of memory units being accessible by another of the data processing cores via a secondary bus path of the bus system.

Ex. 1003, 12:19–44 (emphasis added).

#### *E. Evidence*

Petitioner relies on the following references:

Reference	Exhibit No.
US 5,197,140; filed Nov. 17, 1989; issued Mar. 23, 1993 (“Balmer”)	1005

Reference	Exhibit No.
EP 0 071 727 A1; filed June 23, 1982; published Feb. 16, 1983 (“Budzinski”)	1006
US 6,240,458 B1; filed Dec. 22, 1998; issued May 29, 2001 (“Gilbertson”)	1007
John L. Hennessy & David A. Patterson, COMPUTER ORGANIZATION AND DESIGN: THE HARDWARE/SOFTWARE INTERFACE (2d. ed. 1998) (“Hennessy”)	1012

Petitioner also relies on the Declaration of Dr. Pinaki Mazumder (Ex. 1001) in support of its arguments. The parties rely on other exhibits as discussed below.

*F. Asserted Grounds of Unpatentability*

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4–11, 14–17, 19–27	103(a)	Balmer, Hennessy
1, 2, 4–11, 14–17, 19–27	103(a)	Budzinski, Hennessy
1, 2, 4–11, 14–17, 19–27	103(a)	Budzinski, Hennessy, Gilbertson

II. ANALYSIS

*A. Principles of Law*

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that

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