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Paper 12
Date: September 10, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

PACT XPP SCHWEIZ AG,
Patent Owner.

IPR2020-00537
Patent 7,928,763 B2

Before SALLY C. MEDLEY, KEN B. BARRETT, and CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Intel Corporation ("Petitioner")[1] filed a Petition requesting *inter partes* review of U.S. Patent No. 7,928,763 B2 ("the '763 patent," Ex. 1003). Paper 2 ("Pet."). The Petition challenges the patentability of claims 19 and 49[2] of the '763 patent. PACT XPP Schweiz AG ("Patent Owner")[3] filed a Preliminary Response to the Petition. Paper 6 ("Prelim. Resp."). As authorized by the Board, Petitioner filed a Reply to the Preliminary Response (Paper 7, "Pet. Reply") and Patent Owner filed a Sur-Reply (Paper 10, "PO Sur-Reply").

An *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing on at least one of the challenged claims of the '763 patent. Accordingly, we do not institute an *inter partes* review of the challenged claims.

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[1] Petitioner identifies Intel Corporation as the real party-in-interest. Pet. 2.
[2] As discussed below in Section II.A, the Petition also has grounds directed to claims 1–3, 9–14, 16–18, 20–22, 24, 26, 30–33, 39–44, 46–48, 50–52, 54, 56, and 60. However, because those claims have been statutorily disclaimed by Patent Owner, they are treated as if they never were part of the '763 patent. *See* Ex. 2002, 2.
[3] Patent Owner identifies PACT XPP Schweiz AG (formerly known as Scientia Sol Mentis AG) as the real party-in-interest. Paper 3, 1.

B. Related Proceedings

One or both parties identify, as matters involving or related to the '763 patent: *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-00267 (D. Del. Feb. 7, 2019); *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-00273 (W.D. Tex. April 23, 2019); *Intel Corp. v. PACT XPP Schweiz AG,* No. 19-cv-02241 (N.D. Cal. April 25, 2019); and *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-01006[4] (D. Del. May 30, 2019). Pet. 2; Paper 3, 1–2.

C. The '763 Patent

The '763 patent is titled "Multi-Core Processor System," and "relates to a cell element field and a method for operating same . . . [and] in particular to reconfigurable data processing architectures." Ex. 1003, code (54), 1:23–25. According to the patent, such architectures have certain advantages and off-setting disadvantages, and that "[i]t is desirable to design and use the reconfigurable architecture in such a way that even those data processing steps which are typically particularly suitable for being executed using sequencers are executable particularly rapidly and efficiently." *Id.* at 1:61–2:9.

> [I]t is possible to construct a sequencer structure in a cell element field by providing a dedicated control connection controlled by function cells in a dedicated manner between function cell and function cell means and memory cell and/or memory cell means with only two elements connected by suitable buses without requiring additional measures and/or design changes otherwise.

Id. at 3:19–24. Figure 1 of the '763 is reproduced below.

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[4] Patent Owner identified the case as "19-1066." Paper 3, 2 (underlining added). We understand that to contain a typographical error.

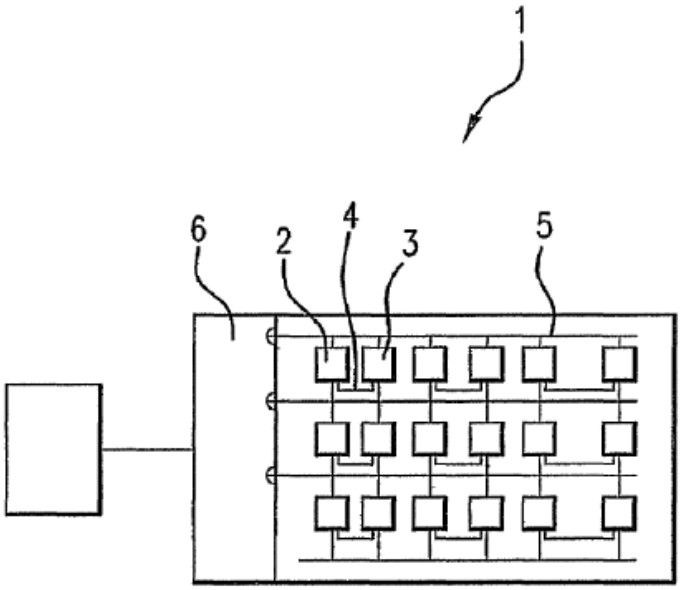

FIG. 1

Id., Fig. 1. Figure 1 shows "a cell element field 1 for data processing [that] includes function cell means 2 for execution of arithmetic and/or logic functions and memory cell means 3 for receiving, storing and/or outputting information, [and] a control connection 4 connecting function cells 2 to memory cells 3," and "interface circuit for communication with external load logic 6." *Id.* at 7:31–32, 7:47–60. "The connections may be configured by switching bus systems 5 as necessary." *Id.* at 7:55–56.

D. Illustrative Claim

The challenged claims of the '763 patent, claims 19 and 49, depend, respectively, from disclaimed independent claims 1 and 31. Independent claim 1 and dependent claim 19, reproduced below, are illustrative.

1. A multi-processor chip, comprising:
a plurality of data processing cells, each adapted for
sequentially executing at least one of algebraic and logic functions and having:
at least one arithmetic logic unit;

at least one data register file;
a program pointer; and
at least one instruction decoder;
a plurality of memory cells;
at least one interface unit;
at least one Memory Management Unit (MMU); and
a bus system for interconnecting the plurality of data processing cells, the plurality of memory cells, and the at least one interface unit;
wherein the bus system is adapted for programmably interconnecting at runtime at least one of data processing cells and memory cells with at least one of memory cells and one or more of the at least one interface unit.

19. The multi-processor chip according to claim 1, wherein at least one of the memory cells is adapted to store data in a non-volatile manner.

Ex. 1003, 13:2–20, 14:13–15.

E. Evidence

Petitioner relies on the following references:

Reference	**Exhibit No.**
US 5,197,140; filed Nov. 17, 1989; issued Mar. 23, 1993 ("Balmer")	1005
US 5,761,523; filed June 7, 1995; issued June 2, 1998 ("Wilkinson")	1007
Takashi Miyamori & Kunle Olukotun, *A Quantitative Analysis of Reconfigurable Coprocessors for Multimedia Applications*, PROCEEDINGS, IEEE SYMPOSIUM ON FPGAS FOR CUSTOM COMPUTING MACHINES, date of conference April 17, 1998 ("Miyamori")[5]	1009

[5] Patent Owner disputes the status of Miyamori as a prior art printed publication. Prelim. Resp. 30–35. For reasons discussed below, disposition of this case does not require us to reach that issue.

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