IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

TESSERA ADVANCED TECHNOLOGIES, INC.,
Patent Owner.

Case No. IPR2020-00581
Patent No. 5,666,046

PETITIONER'S EXHIBIT LIST

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Exhibit	Description
Exhibit 1001	U.S. Patent No. 5,666,046
Exhibit 1002	Declaration of Dr. Behzad Razavi
Exhibit 1003	Prosecution History for U.S. Patent No. 5,666,046
Exhibit 1004	Japanese Patent Application Publication No. JPA H05-251954 ("Hara")
Exhibit 1005	Decision Denying Institution of *Inter Partes* Review in IPR2017-00810 (Paper 8)
Exhibit 1006	Millman et al., Integrated Electronics: Analog and Digital Circuits and Systems (1972)
Exhibit 1007	Lin et al., *A.V.be(T) Model with Application to Bandgap Reference Design,* Regular Correspondence, IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 6 (December 1985)
Exhibit 1008	Hammerschmidt, et al., *A CMOS Bandgap Reference for Low Voltage Application,* IEEE Journal of Solid-State Circuits Conference (October 1993)
Exhibit 1009	U.S. Pat. No. 3,887,863 ("Brokaw")
Exhibit 1010	U.S. Pat. No. 5,631,600 ("Akioka")
Exhibit 1011	IPR2017-00810 Patent Owner Preliminary Response (Paper 6)
Exhibit 1012	U.S. Pat. No. 4,263,519 ("Schade")
Exhibit 1013	Paul A. Tipler, Physics for Scientist and Engineers (3rd ed. 1991)
Exhibit 1014	Gray & Meyer, Analysis and Design of Analog Integrated Circuits (3rd ed. 1993) ("Gray and Meyer")
Exhibit 1015	Grebene, Bipolar and MOS Analog Integrated Circuit Design (1984) ("Grebene")
Exhibit 1016	Nicollini, Senderowicz, *A CMOS Bandgap Reference for Differential Signal Processing*, IEEE Journal of Solid-State Circuits, Vol. 26, No. 1 (January 1991)
Exhibit 1017	Sedra & Smith, Microelectronic Circuits (3rd ed. 1991)
Exhibit 1018	U.S. Pat. No. 5,021,730 ("Smith")
Exhibit 1019	U.S. Pat. No. 4,857,823 ("Bitting")
Exhibit 1020	U.S. Pat. No. 5,049,806 ("Urakawa")
Exhibit 1021	U.S. Pat. No. 5,229,711 ("Inoue")
Exhibit 1022	U.S. Pat. No. 5,512,817 ("Nagaraj")
Exhibit 1023	Gunawan et al, *A Curvature-Corrected Lowe –Voltage Bandgap Reference*, IEEE Journal of Solid State Circuits (June 1993)

Exhibit 1024	Robert A. Pease, *The Design of Band-GAP Reference Circuits: Trials and Tribulations,* IEEE 1990 Bipolar Circuits and Technology Meeting 9.3 (1990)
Exhibit 1025	Eric A. Vittoz, *The Design of High-Performance Analog Circuits on Digital CMOS Chips*, IEEE Journal of Solid-state Circuits (June 1985)
Exhibit 1026	Behzad Razavi, *A Circuit For All Seasons*, IEEE Solid-state Circuits Magazine (2016)
Exhibit 1027	Dismissal Order entered in the U.S. District Court litigation captioned *Invensas Corporation and Tessera Advanced Technologies, Inc. v. NVIDIA Corporation*, No. 19-cv-861-RGA (D. Del. filed May 8, 2019)

Unless indicated otherwise, all emphasis and annotations herein are added by Petitioner. Unless indicated otherwise, all citations to non-patent documents herein are to native page numbers.