NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

BOT M8 LLC, Appellant

v.

SONY INTERACTIVE ENTERTAINMENT LLC, Appellee

KATHERINE K. VIDAL, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PA-TENT AND TRADEMARK OFFICE,

Intervenor

2022-1569, 2022-1570

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2020-00726, IPR2020-01288.

Decided: August 30, 2023

Paul J. Andre, Kramer Levin Naftalis & Frankel LLP, Redwood Shores, CA, argued for appellant. Also represented by James R. Hannah, Liea Kohialka, Shroya Rame

sented by James R. Hannah, Lisa Kobialka, Shreya Ramchandani; Jeffrey Eng, Aaron M. Frankel, Cristina Martin



ez, New York, NY.

Abran J. Kean, Erise IP, P.A., Greenwood Village, CO, argued for appellee. Also represented by Eric Allan Buresh, Overland Park, KS.

William LaMarca, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA, for intervenor. Also represented by Michael S. Forman, Thomas W. Krause, Farheena Yasmeen Rasheed.

Before Prost, Reyna, and Cunningham, *Circuit Judges*. Cunningham, *Circuit Judge*.

Bot M8 LLC appeals from final written decisions issued in two Patent Trial and Appeal Board inter partes reviews that found claims 1–5 of U.S. Patent No. 8,112,670 and claims 1–10 of U.S. Patent No. 7,664,988 (collectively, the "Challenged Claims" or "Challenged Patents," respectively) to be unpatentable. Sony Interactive Ent. LLC v. Bot M8, LLC, IPR2020-00726, 2021 WL 4876235, at *1 (P.T.A.B. Oct. 4, 2021) ("Decision I"); Sony Interactive Ent. LLC v. Bot M8, LLC, IPR2020-01288, 2022 WL 495115, at *1 (P.T.A.B. Feb. 15, 2022) ("Decision II"). On appeal, Bot M8 challenges the Board's determinations based on its constructions of the claim terms "fault inspection program" and "boot program." We disagree that the Board adopted erroneous constructions of those terms and affirm.

I. Background

The '670 patent is a continuation of the '988 patent and is entitled "Gaming Apparatus Having Memory Fault Detection." The Challenged Patents disclose "an information



¹ Because the Challenged Patents are related and share a specification, we generally cite to the '670 patent.

process device in which it can be guaranteed that a fault inspection program properly operates even if a fault occurs in a memory device which is inspected through the fault inspection program." '670 patent col. 1 ll. 35–40. Among other things, the Challenged Patents accomplish this objective by using a "fault inspection program" stored in one memory device that inspects faults in a second memory device. *Id.* col. 1 ll. 41–65. Because the fault inspection program is not stored in the memory it inspects, it "properly operates" independent of whether that memory has a fault. *Id.* col. 1 ll. 60–65.

Claim 1 of the '670 patent recites:

1. A gaming device configured to execute a game, the gaming device comprising:

a mother board on which a first memory device is provided;

a second memory device configured to store a game application program, the second memory device being connected to the mother board; and

a control device for executing a fault inspection program for the second memory device to inspect whether or not a fault occurs in the second memory device;

wherein the fault inspection program is stored in the first memory device, and the control device completes the execution of the fault inspection program before the game is started.

Id. col. 4 l. 61–col. 5 l. 7 (emphasis added). Dependent claim 2 introduces a "boot program" and recites:

2. The gaming device according to claim 1,



4 BOT M8 LLC v. SONY INTERACTIVE ENTERTAINMENT LLC

wherein the first memory device stores a boot program executed when the gaming device is started to operate, and

wherein the control device executes the fault inspection program after the boot program is executed.

- *Id.* col. 5 ll. 8–12 (emphases added). Independent claim 4 contains similar requirements to claim 1, but it inspects faults in the "game application program" stored in the memory device, not the memory device itself, and recites:
 - 4. A gaming device configured to execute a game, the gaming device comprising:
 - a ROM configured to store a fault inspection program;
 - a memory device which is electrically rewritable a game application program stored therein;
 - a control device configured to execute the fault inspection program to inspect whether or not a fault occurs in the game application program stored in the memory device;

wherein the control device executes the fault inspection program when the gaming device is started to operate and completes the execution of the fault inspection program before the game is started.

Id. col. 5 l. 15–col. 6 l. 10 (emphasis added).

Claim 1 of the '988 patent generally combines these requirements into a single claim:

1. A gaming device configured to execute a game, the gaming device comprising:



a first memory device for *storing a boot program* executed when the gaming device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing a game application program for the game, the second memory device being connected to the mother board; and

a control device for executing a fault inspection program for the gaming device to inspect whether or not a fault occurs in the second memory device and the game application program stored therein,

wherein the fault inspection program is stored in the first memory device, and the control device executes the fault inspection program when the gaming device is started to operate and completes the execution of the fault inspection program before the game is started.

'988 patent col. 4 l. 55–col. 5 l. 5 (emphases added).

In its final written decision for the IPR on the '670 patent, the Board concluded, among other things, that claims 1–4 are unpatentable based on Sugiyama² in combination with Gatto,³ and claim 5 is unpatentable based on Sugiyama in combination with Gatto and Yamaguchi.⁴ *Decision I* at *2, *17. For the IPR on the '988 patent, the



² Japanese Unexamined Patent Application Publication Disclosure No. JP 2000-35888 published Feb. 2, 2000.

³ WIPO Int'l Publication No. WO 2004/004855 A1 published Jan. 15, 2004.

⁴ U.S. Patent No. 5,844,776 issued Dec. 1, 1998.

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