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Paper 36
Entered: December 1, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

IPR2020-01007
Patent 6,424,041 B1

Before JUSTIN T. ARBES, DAVID C. MCKONE,
and AMBER L. HAGY, *Administrative Patent Judges*.

MCKONE, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Micron Technology, Inc. ("Petitioner") filed a Corrected Petition (Paper 7, "Pet.")[1] requesting *inter partes* review of claims 1–17 of U.S. Patent No. 6,424,041 B1 (Ex. 1001, "the '041 patent"). Pet. 1. Godo Kaisha IP Bridge 1 ("Patent Owner") filed a Preliminary Response (Paper 9, "Prelim. Resp."). Pursuant to our authorization (Paper 10), Petitioner filed a Preliminary Reply (Paper 11) and Patent Owner filed a Preliminary Sur-reply (Paper 12). Pursuant to 35 U.S.C. § 314, we instituted this proceeding. Paper 15 ("Dec.").

Patent Owner filed a Patent Owner's Response (Paper 20, "PO Resp."), Petitioner filed a Reply to the Patent Owner's Response (Paper 24, "Reply"), and Patent Owner filed a Sur-reply to the Reply (Paper 29, "Sur-reply"). An oral argument was held in this proceeding on September 15, 2021. Paper 35 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–17. Based on the record before us, Petitioner has proved, by a preponderance of the evidence, that claims 1–17 are unpatentable.

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[1] Petitioner filed an original Petition in this proceeding as Paper 1. The parties jointly requested that Petitioner be permitted to file a corrected Petition deleting certain material to remedy an alleged violation of the maximum word count. Given the parties' agreement, we authorized the filing of the corrected Petition by e-mail on July 28, 2020. *See* Ex. 1026 (redline comparison between the original Petition and corrected Petition).

B. Related Matters

The parties indicate that the '041 patent has been asserted in *Godo Kaisha IP Bridge 1 v. Micron Technology, Inc.*, Case No. 6:20-cv-00178 (W.D. Tex.[2]) ("the Texas case"). Pet. 5; Paper 5, 1. Petitioner also has filed petitions for *inter partes* review of two other patents in IPR2020-01008 and IPR2020-01009. Pet. 5; Paper 5, 1. The patents challenged in those two petitions also are asserted in the Texas case. Pet. 5. The '041 patent previously was challenged in *Intel Corp. v. Godo Kaisha IP Bridge 1*, IPR2018-00664. Pet. 5. A panel of the Board instituted a trial in that proceeding. Ex. 1004. It later was terminated due to settlement. Ex. 1005; Pet. 5.

C. The '041 Patent

The '041 patent describes semiconductor devices designed to prevent copper from diffusing from wiring into memory storage regions. Ex. 1001, Abstract. The patent explains that, as demand has increased for smaller semiconductor devices, aluminum wiring has been replaced with copper wiring, which has reduced electrical resistance, power consumption, and heat generation. *Id.* at 1:10–34. On the other hand,

> copper atoms have a property of easily diffusing into silicon and a silicon oxide film. Therefore, a copper bridge is formed between copper wires, causing short-circuit thereof. Moreover, the copper atoms get into an active region of the silicon substrate, resulting in unsatisfactory characteristics and malfunctioning.

[2] We refer to the United States District Court for the Western District of Texas, Waco Division, as "the Texas court."

Id. at 1:35–40. The patent describes a solution employing a "copper diffusion blocking means provided in a region surrounding the memory storage portion for blocking copper diffusion from the wiring portion toward the memory storage portion." *Id.* at 2:60–63. Figure 1, reproduced below, illustrates an example:

FIG. 1

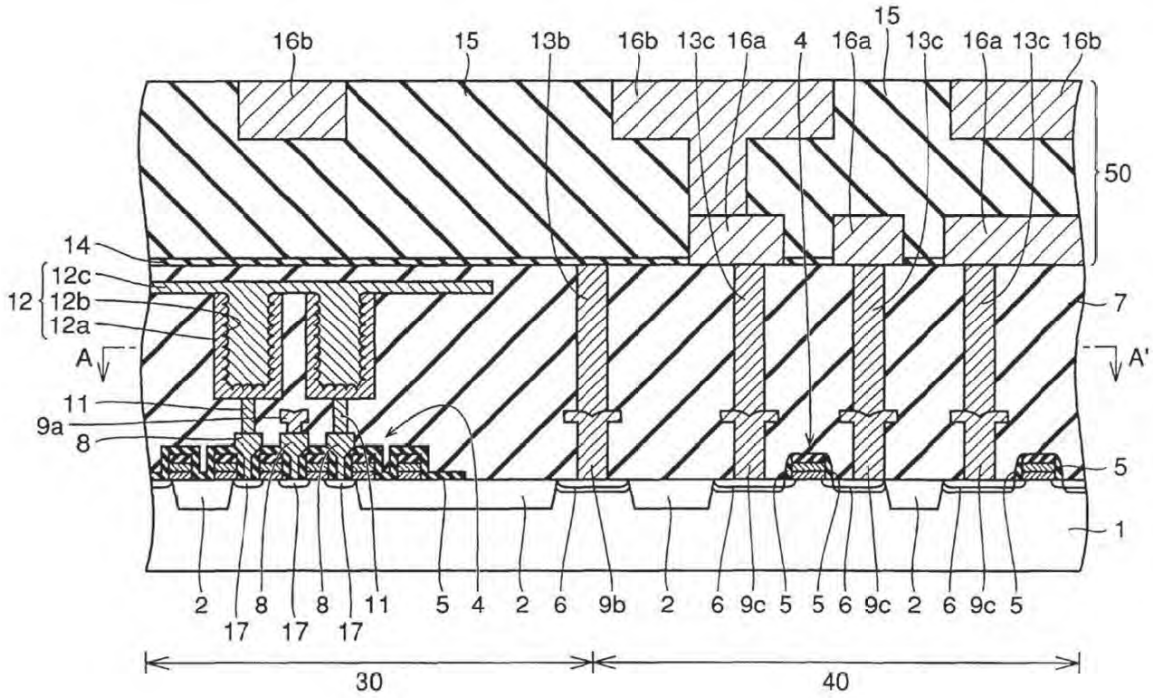

Figure 1 is a cross-sectional view of a semiconductor device. *Id.* at 5:66–67.

As shown in Figure 1, a semiconductor device includes substrate 1 and is divided into memory cell portion 30 and peripheral circuit portion 40. *Id.* at 7:2–5. The semiconductor device also includes wiring layer region 50 that includes insulating film 15 and copper wires 16a, 16b formed in insulating film 15. *Id.* at 7:16–19.

As to memory cell portion 30, the '041 patent states:

> Gates 4 and source/drain regions 17 with the corresponding gate interposed therebetween are formed in the memory cell portion 30. A lift pad 8 is formed on each source/drain region 17. A bit-line contact and bit line 9*a* are formed on the lift pads

> 8 that are not connected to a capacitor. A capacitor 12 is provided on the other lift pads 8 with respective capacitor contacts 11 interposed therebetween.

Id. at 7:5–12. Patent Owner contends that gates 4 and source/drain regions 17, together, form an access transistor that controls charge entering and leaving capacitor 12. PO Resp. 6–9 (citing Ex. 1001, 3:24–30, 7:3–12).

Between memory cell portion 30 and wiring layer region 50 is ceiling film 14, formed from a non-conductive silicon nitride (Si_3N_4) film. Ex. 1001, 7:25–26. According to the '041 patent, "[t]his ceiling film is located away from the copper wires, i.e., at a position where the driving force for copper diffusion is small. Therefore, even a slight amount of copper diffusion can be prevented." *Id.* at 7:26–30. The patent also explains that

> [c]opper-diffusion preventing films 9b and 13b extending like a vertical wall are formed at the boundary between the memory cell portion 30 and peripheral circuit portion 40 so as to surround the side surface of the memory cell portion. This vertical-wall-like copper-diffusion preventing films 9b and 13b are formed from a tungsten film.

Id. at 7:39–45. According to the patent, "[t]he ceiling film 14 and vertical walls 9b and 13b block diffusion of copper atoms from the copper wires 16, so that copper atoms no longer reach the capacitors 12 of the memory cells even in a slight amount." *Id.* at 8:3–6.

Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A semiconductor device, comprising:
>
> a semiconductor substrate,
>
> a memory storage portion on a main surface of said semiconductor substrate,

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