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Paper 31
Entered: December 6, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

IPR2020-01008
Patent 6,445,047 B1

Before JUSTIN T. ARBES, DAVID C. McKONE, and AMBER L. HAGY, *Administrative Patent Judges.*

ARBES, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Petitioner Micron Technology, Inc. ("Petitioner"), filed a Petition (Paper 7, "Pet.") requesting *inter partes* review of claims 1–4 of U.S. Patent No. 6,445,047 B1 (Ex. 1001, "the '047 patent") pursuant to 35 U.S.C.

§ 311(a). On December 7, 2020, we instituted an *inter partes* review as to all challenged claims on all grounds of unpatentability asserted in the Petition. Paper 10 ("Decision on Institution" or "Dec. on Inst."). Patent Owner Godo Kaisha IP Bridge 1 ("Patent Owner") subsequently filed a Patent Owner Response (Paper 15, "PO Resp."), Petitioner filed a Reply (Paper 18, "Reply"), and Patent Owner filed a Sur-Reply (Paper 22, "Sur-Reply"). An oral hearing was held on September 15, 2021, and a transcript of the hearing is included in the record (Paper 30, "Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–4 are unpatentable.

B. Related Matters

The parties indicate that the '047 patent is the subject of the following pending district court case: *Godo Kaisha IP Bridge 1 v. Micron Technology, Inc.*, Case No. 20-cv-00178 (W.D. Tex.) ("the district court case"). *See* Pet. 5; Paper 5, 1. Petitioner also filed petitions challenging claims of other patents asserted in the district court case in Cases IPR2020-01007 and IPR2020-01009.

C. The '047 Patent

The '047 patent discloses a semiconductor device including two different surface-channel-type metal-oxide-semiconductor field-effect transistors (MOSFETs) with different threshold voltages. Ex. 1001, col. 1, ll. 5–10. According to the '047 patent, "it is very important to form surface-channel-type MOSFETs of multiple types on a semiconductor chip"

to enhance performance in a large-scale integration (LSI) system. *Id.* at col. 1, ll. 11–17. The '047 patent states that it was known to use, in the same semiconductor device, MOSFETs in a "logic circuit block" that "enhance their driving power by lowering the threshold voltage and increasing the saturated current value" and MOSFETs in a "memory cell block" that "increase a data retention time by raising the threshold voltage value and minimizing the leakage current." *Id.* at col. 1, ll. 18–27. Further, to form multiple types of surface-channel-type MOSFETs with different threshold voltages, it was known to "mak[e] the dopant concentrations in the channel regions different by implanting dopant ions at mutually different doses into the channel regions." *Id.* at col. 1, ll. 47–52. Setting a higher implant dose for the memory cell block MOSFET results in a higher threshold voltage. *Id.* at col. 1, ll. 52–57. Also, as gate insulating films become thinner due to the need for miniaturization, the dopant concentration needed to realize a certain threshold voltage increases. *Id.* at col. 1, ll. 58–62. The '047 patent discloses that "performance degrades . . . as the dopant concentration in the channel region gets higher" due to, for example, increased "leakage current flowing through the pn junction." *Id.* at col. 1, l. 63–col. 2, l. 12.

The '047 patent seeks to solve these problems using a first-surface-channel-type MOSFET in a "logic circuit block" "with a threshold voltage of a relatively small absolute value" and a second-surface-channel-type MOSFET that "controls power to be supplied to the logic circuit block" "with a threshold voltage of a relatively large absolute value." *Id.* at col. 2, ll. 20–24, 58–62. To increase the threshold voltage "without raising the dopant concentration," the second-surface-channel-type MOSFET includes a gate electrode "formed out of a refractory metal film made of a refractory metal or a compound thereof" (e.g., titanium nitride, tungsten, molybdenum,

tantalum). *Id.* at col. 2, ll. 28–48, col. 3, ll. 61–63, col. 6, ll. 46–51. The second-surface-channel-type MOSFET also has a thicker gate insulating film to "enhance its OFF-state leakage current characteristics" and improve storage ability. *Id.* at col. 3, ll. 4–16.

Figures 4(a)–4(c) of the '047 patent are reproduced below.

Fig. 4(a)

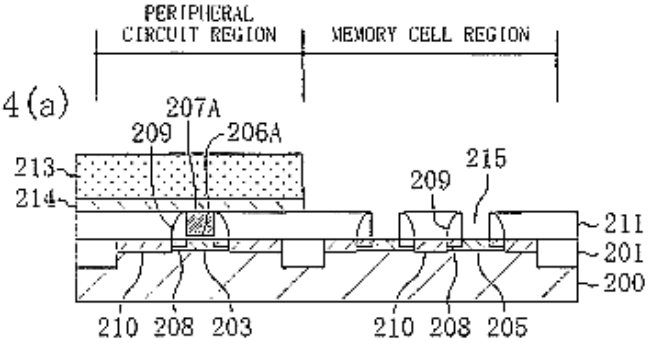


Fig. 4(b)

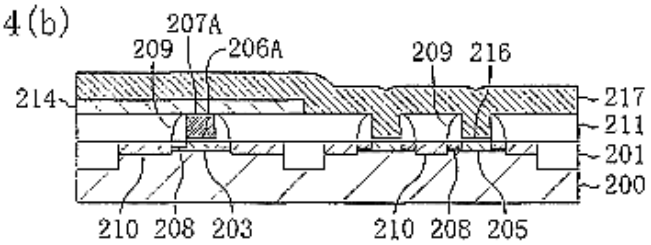
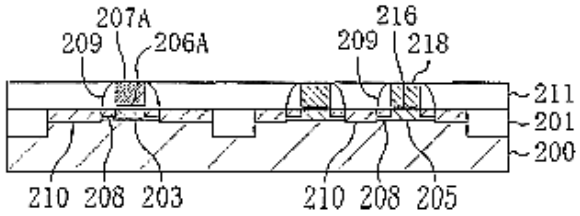


Fig. 4(c)



Figures 4(a)–4(c) depict the later steps of a fabrication process for a semiconductor device with "a first [n-type metal-oxide-semiconductor (NMOS)] transistor . . . formed in a peripheral circuit region on the left side, while second NMOS transistors are formed in a memory cell region on the right side." *Id.* at col. 6, ll. 60–67. The first-surface-channel-type NMOS transistor has first gate electrode 207A, which is "made of an n-type

polysilicon film" and has "a threshold voltage with a relatively small absolute value," formed on first gate insulating film 206A "with a relatively small thickness of 2.5 nm." *Id.* at col. 8, ll. 15–20, 26–30. The second-surface-channel-type NMOS transistors each have second gate electrode 218, which is made of a refractory metal (tungsten) and has "a threshold voltage with a relatively large absolute value," formed on second gate insulating film 206B "with a relatively large thickness of 5 nm." *Id.* at col. 8, ll. 20–25, 30–35. P-type doped region 205 in the channel region of the second-surface-channel-type NMOS transistors has a "relatively low dopant concentration" as compared to p-type doped region 203 of the channel region of the first-surface-channel-type NMOS transistor, which has a "relatively high dopant concentration." *Id.* at col. 7, ll. 6–22, col. 8, ll. 36–40.

D. Illustrative Claim

Challenged claim 1 of the '047 patent is independent. Claims 2–4 depend from claim 1. Claim 1 recites:

> 1. A semiconductor device comprising:
>
> a first-surface-channel-type MOSFET with a first threshold voltage; and
>
> a second-surface-channel-type MOSFET with a second threshold voltage having an absolute value greater than an absolute value of said first threshold voltage,
>
> wherein the first-surface-channel-type MOSFET includes:
>
> a first gate insulating film formed on a semiconductor substrate; and
>
> a first gate electrode, which has been formed out of a poly-silicon film formed directly on the first gate insulating film, and

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