UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	276900US90
First Inventor or Application Identifier	Jun HAISHIMA
Title	INFORMATION PROCESS DEVICE

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Commissioner for Patents
Mail Stop Patent Application
Alexandria, Virginia 22313

1. ■ Fee Transmittal Form (e.g. PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ■ Specification — Total Sheets: 8
3. ■ Drawing(s) *(35 U.S.C. 113)* — Total Sheets: 3
4. ■ Oath or Declaration — Total Pages: 3
   a. ■ Newly executed (Fax copy)
   b. ☐ Copy from a prior application *(37 C.F.R. §1.63(d))*
   (for continuation/divisional with box 18 completed)
      i. ☐ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see *37 C.F.R. §1.63(d)(2) and 1.33(b).*
5. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
6. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. Specification or Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ■ Assignment Papers (cover sheet & document(s))
8. ■ Application Data Sheet. See 37 CFR 1.76
9. ☐ 37 C.F.R. §3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
10. ☐ English Translation Document *(if applicable)*
11. ■ Information Disclosure Statement (IDS)/PTO-1449 ■ Copies of IDS Citations (2)
12. ☐ Preliminary Amendment
13. ■ White Advance Serial No. Postcard
14. ■ Certified Copy of Priority Document(s) (1) *(if foreign priority is claimed)*
15. ☐ Applicant claims small entity status. *See 37 CFR 1.27*
16. ☐ Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. ■ Other: Submission Notice Regarding Priority Document(s)

112991 U.S.PTO 11/205121 081705

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no.:

Prior application information: Examiner: Group Art Unit:

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

Customer Number
22850
(703) 413-3000
FACSIMILE: (703) 413-2220

Name:	Masayasu Mori	Registration No.:	47,301
Signature:		Date:	8-17-05
Name:	C. Irvin McClelland	Registration No.:	

Registration Number 21,124

Docket No. 276900US90

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Jun HAISHIMA

SERIAL NO: New Application

FILING DATE: Herewith

FOR: INFORMATION PROCESS DEVICE

FEE TRANSMITTAL

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	3 - 20 =	0	x $50 =	$0.00
INDEPENDENT CLAIMS	1 - 3 =	0	x $200 =	$0.00
UTILITY APPLICATION SIZE FEE	11 - 100 =	0 (each addtl. 50 sheets over 100)	x $250 =	$0.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ $360 =	$0.00
☐ LATE FILING OF DECLARATION			+ $130 =	$0.00
■ FILING FEE ($300.00) ■ SEARCH FEE ($500.00) ■ EXAMINATION FEE ($200.00)			BASIC FEES	$1,000.00
			TOTAL OF ABOVE CALCULATIONS	$1,000.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				$0.00
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Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Date: 8-17-05

Masayasu Mori
Registration No. 47,301

C. Irvin McClelland
Registration Number 21,124

Customer Number
22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 12/04)

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Docket No. 276900US90

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(OSMMN 12/04)

INFORMATION PROCESS DEVICE

CROSS-REFERENCE TO THE RELATED APPLICATION (S)

This application is based upon and claims a priority from the prior Japanese Patent Application No. 2004-245377 filed on August, 25, 2004, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an information process device in which a fault in hardware or software is inspected.

2. Description of Related Art

In a conventional information process device, data and programs required in calculation or control are stored in one memory area of a memory device such as a hard disk and a program for inspecting whether or not a fault such as damage, change or falsification occurs in the programs or data (hereinafter, abbreviated as "fault inspection program") is stored in the other memory area in the same memory device, as disclosed in Unexamined Japanese Publication No. 2003-331236.

Therefore, in a case that the damage occurs in the memory device, there is fear that the fault inspection program is also damaged. At that time, it cannot be guaranteed that the fault inspection program properly operates.

SUMMARY OF THE INVENTION

In order to dissolve the above problems, the present invention has been done and has an object to provide an information process device in which it can be guaranteed that a fault inspection program properly operates even if a fault occurs in a memory device which is inspected through the fault inspection program.

In order to accomplish the above object, according to one aspect of the present invention, it is provided an information process device comprising:

a first memory device for storing a boot program executed when the information process device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing an application program, the second memory device being connected to the mother board;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device;

wherein the fault inspection program is stored in the first memory device; and

wherein the control device executes the fault inspection program when the information process device is started to operate.

According to the information process device of the present invention, the fault inspection program is stored in the first memory device on the mother board which is independent from the second memory device, thereby even if the fault occurs in the second memory device, it can be guaranteed that the fault inspection program properly operates.

The above and further objects and novel features of the invention will more fully appear from the following detailed description when the same is read in connection with the accompanying drawings. It is to be expressly understood, however, that the drawings are for purpose of illustration only and not intended as a definition of the limits of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification illustrate embodiments of the invention and, together with the description, serve to explain the objects, advantages and principles of the invention.

In the drawings,

Fig. 1 is a block diagram of an information process device according to the embodiment,

Fig. 2 is a flowchart of a start program executed when the information process device is started to operate, and

Fig. 3 is a perspective view of the information process device according to the embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the embodiment according to the present invention will be described with reference to the drawings.

Fig. 1 is a block diagram of the embodiment according to the present invention. Fig. 3 is a perspective view of an information process device of the embodiment. As shown in Fig. 3, although the information process device 1 is a gaming machine for business use, such gaming machine utilizes an operating system (OS) which is generally used in a personal computer on sale. And under an operation circumstances thereof, a game soft program stored in a hard disk mentioned later is operated.

And as shown in Fig. 1, in the information process device 1 according to the embodiment, a CPU 12, a ROM 13, a RAM 14, a bus 15, connectors 16, 17, a port 18, extended slots 19, 20 are provided on a mother board 11.

The CPU 12 controls the information process device 1 of the embodiment and executes various programs. Therefore, the CPU 12 corresponds to a control device.

And the ROM 13 is a nonvolatile memory in which various control programs are stored, such control programs being required when the information process device 1 of the embodiment is started to operate. The ROM 13 corresponds to a first memory device. And in the ROM 13, as shown in Fig. 1, a boot program storing area 13a for storing a boot program, a fault inspection program storing area 13b for storing a fault inspection program and a start program storing area 13c for storing a start program are formed.

Here, the boot program stored in the boot program storing area 13a, the fault inspection program stored in the fault inspection program storing area 13b and the start program stored in the start program storing area 13c will be described hereinafter.

Further, the RAM 14 is a memory for temporarily storing various data calculated when the CPU 12 executes programs.

The bus 15 is constructed from a PCI bus in which a bridge circuit for frequency change is formed, and becomes a common signal bus through which transmission and receipt of signals are conducted among the CPU 12, the ROM 13, the RAM 14, the connectors 16, 17, the port 18 and the extended slots 19, 20.

The connector 16 is a device to connect an output device 21 required when the

game soft program is operated, to the mother board 11.

Here, the output device 21 connected to the connector 16 is constructed from a liquid crystal display (see the reference number 21 in Fig. 3) and a sound output device (not shown) such as a speaker. Instead of the liquid crystal display (see the reference number 21 in Fig. 3), a CRT display and the like may be used.

The connector 17 is a device to connect an input device required when the game soft program is operated, to the mother board 11. Here, the input device 22 is constructed from a control panel 22 (see Fig. 3) provided with a plurality of button switches (not shown). The input device 22 may include the other devices such as a keyboard, a mouse and the like, and according to contents of the game soft program, a joystick and the like may be connected to the connector 17. And in Fig. 1, although only one connector 17 is shown, if a plurality of input devices 22 are used, plural connectors 17 are provided respectively corresponding to each of the input devices 22.

And a hard disk 24 (HDD) is connected to the port 18 through a flat cable 23.

And in the hard disk 24 connected to the port 18, there are formed an operating system (OS) storing area 24a for storing the OS, an extended BIOS (Basic Input Output System) storing area 24b for storing an extended BIOS and an application storing area 24c for storing an application program which is the game soft program. Therefore, the hard disk 24 corresponds to a second memory device.

And the extended slot 19 is an insertion slot to connect a video board 25 to the mother board 11.

Here, the video board 25 connected to the mother board 11 through the extended slot 19 is a board having a graphics-accelerator to display figures and characters on the liquid crystal display (see the reference number 21 in Fig. 3) which is one of the output devices 21. The video board 25 can conduct performance with a resolution level and a graphics describing speed so that the operation of the game soft program in the information process device 1 of the embodiment can be properly executed.

And the extended slot 20 is an insertion slot to connect a sound board 26 to the mother board 11.

Here, the sound board 26 connected to the mother board 11 through the extended slot 20 is a board having a chip such as FM sound source and PCM sound

source to output sounds from the speaker (not shown) which is one of the output devices 21. The sound board 26 can conduct performance so that the operation of the game soft program in the information process device 1 of the embodiment can be properly executed.

Next, with reference to a flowchart shown in Fig. 2, it will be described an operation executed when the information process device 1 according to the embodiment is started to operate. Fig. 2 is a flowchart of a start program executed when the information process device 1 is started to operate.

In the information process device 1 of the embodiment, when the device 1 is started to operate, the start program stored in the start program storing area 13c of the ROM 13 is executed by the CPU 12.

That is to say, as shown in Fig. 2, when the start program is executed, at first in S11, a boot program is executed.

Here, the boot program is a program stored in the boot program storing area 13a of the ROM 13, and based on the boot program, initialization of various devices including the extended BIOS (Basic Input Output System) in the hard disk 24 and the OS (Operating System) in the hard disk 24 is executed.

At that time, since the OS (Operating System) in the hard disk 24 is loaded in the RAM 14 and started to operate, the ROM 13 may be called as a boot ROM at this point of view.

Next, when procedure of the start program shifts to S12, the fault inspection program is executed.

Here, the fault inspection program is a program stored in the fault inspection program storing area 13b and through which a fault inspection in the hard disk 24 is executed. Concretely, according to the fault inspection program, it is inspected whether or not a damage occurs in the hard disk 24 or whether or not change or falsification of the program stored in the hard disk 24 is conducted.

Next, when procedure of the start program shifts to S13, it is determined whether or not a fault occurs in the hard disk 24. This determination is conducted based on an execution result of the fault inspection program obtained in S12.

At that time, if it is determined that the fault does not occur in the hard disk 24 (S13: NO), procedure shifts to S14, thereafter the application program stored in

the hard disk 24 is loaded in the RAM 14 and execution of the application program is started. On the other hand, if it is determined that the fault occurs in the hard disk 24 (S13: YES), procedure shifts to S15 and error display is conducted on the liquid crystal display (see the reference number 21 in Fig. 3) which is one of the output devices 21.

As mentioned, in the information process device 1 according to the embodiment, as shown in Fig. 1, the fault inspection program is stored in the fault inspection program storing area 13b of the ROM 13 on the mother board 11 independently from the hard disk 24, thereby even if a fault occurs in the hard disk 24 which is inspected by the fault inspection program, it can be guaranteed that the fault inspection program properly operates.

And as shown in Fig. 3, the information process device 1 of the embodiment is used as the gaming machine for business use, and as shown in Fig. 2, the fault inspection program stored in the ROM 13 is executed at the time that the information process device 1 is started to operate and the fault inspection in the hard disk 24 is executed before games are started. Therefore, measures to avoid troubles during gaming can be taken beforehand, without giving displeasure to a player of the gaming machine for business use.

Here, the present invention is not limited to the embodiment mentioned in the above and various modifications can be conducted within the scope of the present invention.

For example, as shown in Fig. 3, although the information process device 1 of the embodiment is used as the gaming machine for business use, the information process device 1 may be adopted for a personal computer on sale. In this case, the keyboard, the mouse or the joystick may be utilized as the input device, instead of the control panel 22.

And in the information process device 1 of the embodiment, although the hard disk 24 is used as the second memory device, a flash memory in which contents can be changed and stored may be used. In this case, the fault inspection program inspects whether or not a fault occurs in the flash memory.

The present invention can be adopted for the fault inspection in the information process device.

WHAT IS CLAIMED IS:

1. An information process device comprising:

a first memory device for storing a boot program executed when the information process device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing an application program, the second memory device being connected to the mother board;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device;

wherein the fault inspection program is stored in the first memory device; and

wherein the control device executes the fault inspection program when the information process device is started to operate.

2. The information process device according to claim 1, wherein the first memory device is a ROM provided on the mother board,

wherein the second memory device is a hard disk which is independent from the mother board, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk.

3. The information process device according to claim 1, wherein the information process device is utilized as a gaming machine for business use.

ABSTRACT OF THE DISCLOSURE

In the information process device 1, the fault inspection program is stored in the fault inspection program area 13b of the ROM 13 provided on the mother board 11 which is independently arranged from the hard disk 24, thereby even if a fault occurs in the hard disk 24 which is inspected by the fault inspection program, it can be guaranteed that the fault inspection program properly operates.

FIG.1

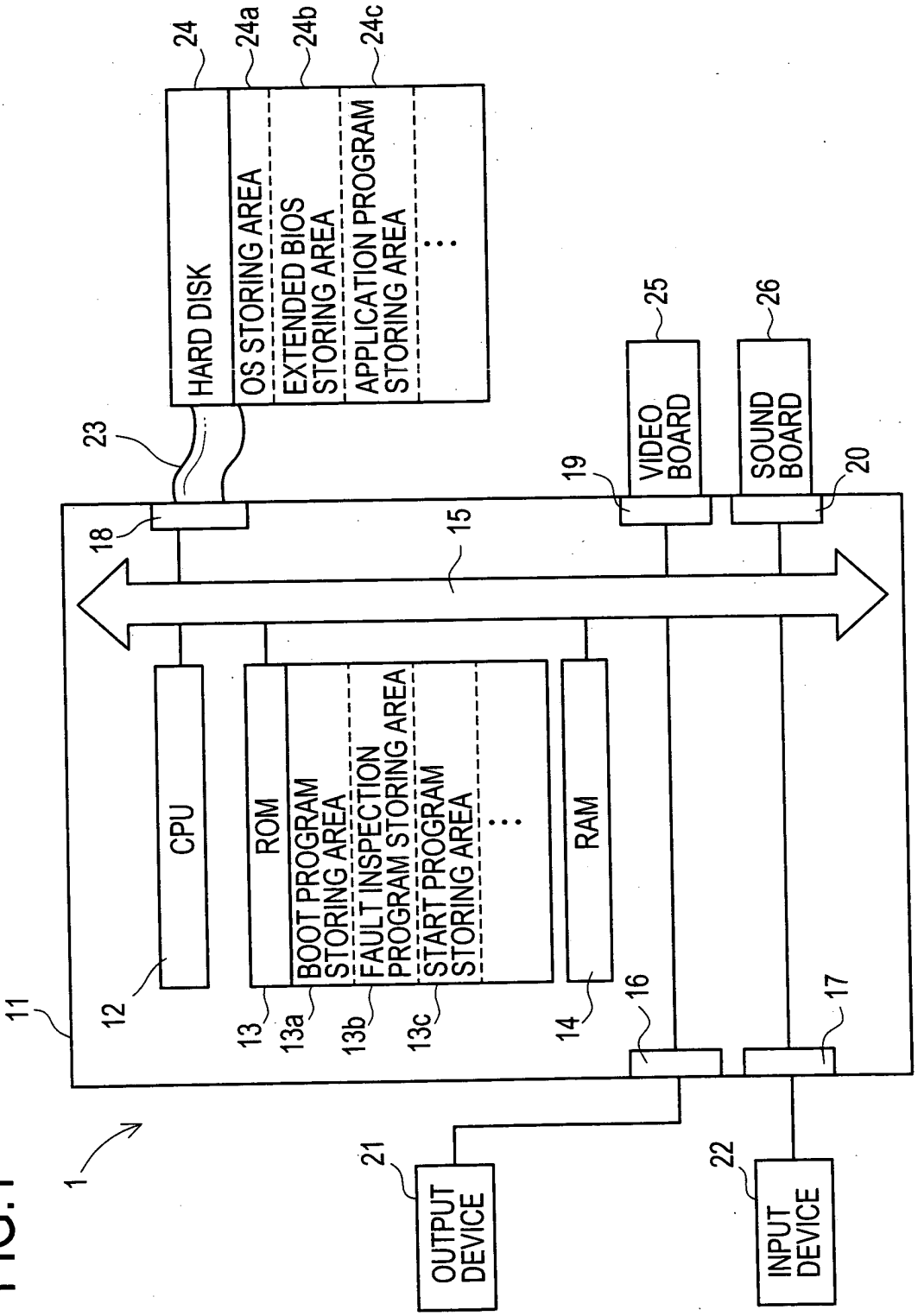

1
11
12
CPU
13
ROM
13a
BOOT PROGRAM STORING AREA
13b
FAULT INSPECTION PROGRAM STORING AREA
13c
START PROGRAM STORING AREA
14
RAM
15
16
17
18
19
20
21
OUTPUT DEVICE
22
INPUT DEVICE
23
24
HARD DISK
24a
OS STORING AREA
24b
EXTENDED BIOS STORING AREA
24c
APPLICATION PROGRAM STORING AREA
25
VIDEO BOARD
26
SOUND BOARD

FIG.2

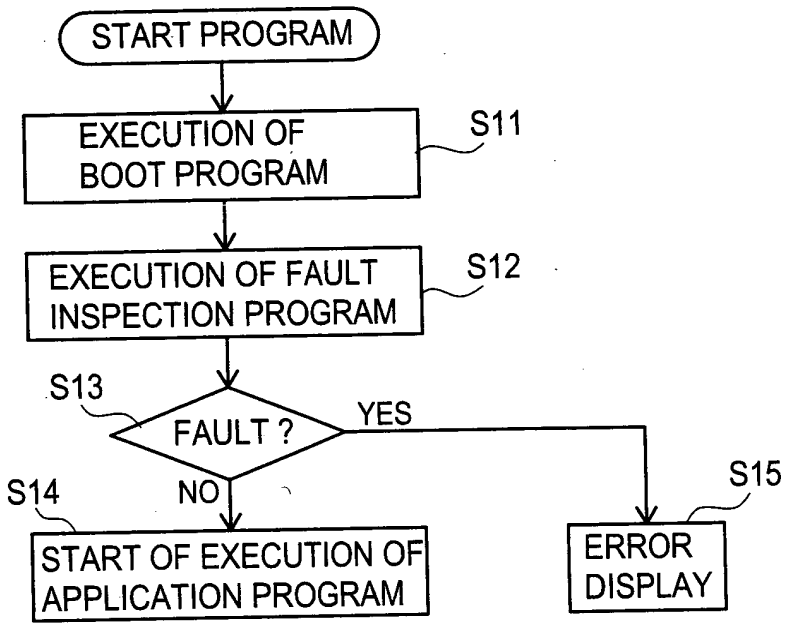
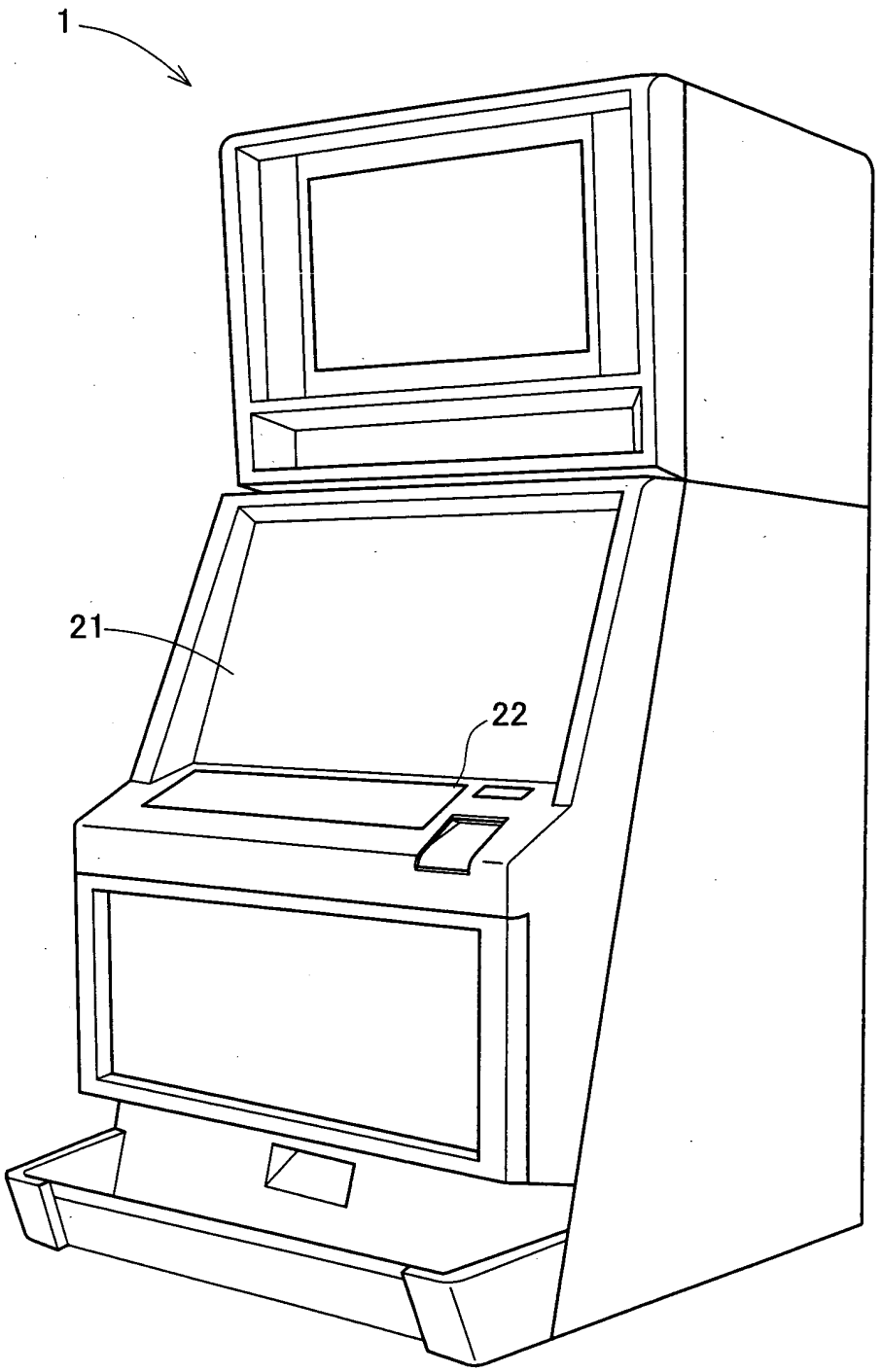

START PROGRAM
EXECUTION OF BOOT PROGRAM
S11
EXECUTION OF FAULT INSPECTION PROGRAM
S12
S13
FAULT ?
YES
NO
S14
S15
START OF EXECUTION OF APPLICATION PROGRAM
ERROR DISPLAY

FIG.3



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

私の住所、郵便の宛先、国籍は下記の私の氏名の後に記載された通りです。

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の名称が複数の場合）であると信じています。

上記発明の明細書は、

☐ 本書に添付されています。

☐ ____ 月 ____ 日に提出され、米国出願番号または特許協定条約国際出願番号を

____ とし、

（該当する場合） ____ に訂正されました。

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

INFORMATION PROCESS DEVICE

the specification of which

☐ is attached hereto.

☐ was filed on ____

as United States Application Number or PCT International Application Number

____ and was amended on

____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第 35 篇 119 条(a) – (d)項又は 365 条 (b)項
に基づき下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約 365(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、件内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, § 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Claimed (優先権主張)	
2004-245337 (Number) (番号)	Japan (Country) (国名)	25 August 2004 (Day/Month/Year Filed) (出願年月日)	☒ Yes はい	☐ No いいえ
			☐ Yes はい	☐ No いいえ

私は、第 35 篇米国法典 119 条 (e) 項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第 35 篇 120 条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約 365 条 (c) に基づく権利をここに主張します。また、
本出願の各請求項の内容が米国法典第 35 篇 112 条第 1 項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第 37 篇 1 条 56 項で定義された特許資格の有効に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第 18 篇第 1001 条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。
（弁護士、または代理人の指名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: (list name and registration number)

022850

書類送付先

Send Correspondence to:

022850

直接電話連絡先：（名前及び電話番号）

Direct Telephone calls to: (name and telephone number)

(703) 413-3000

単独発明者または第一の共同発明者の氏名	Full name of sole or first inventor Jun HAISHIMA
発明者の署名 日付	Inventor's signature 配島 淳 Date 8/11/2005
住所	Residence Tokyo, Japan
国籍	Citizenship Japanese
郵便の宛先	Mailing Address 3-1-25, Ariake, Koto-ku, Tokyo 135-0063 Japan

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

08/18/2005 YPOLITE1 00000029 11205121

01 FC:1011	300.00 OP
02 FC:1111	500.00 OP
03 FC:1311	200.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PTO/SB/03 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number: 11205-121

APPLICATION AS FILED – PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	150.00		N/A	300.00
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	$250		N/A	$500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$100		N/A	$200
TOTAL CLAIMS (37 CFR 1.16(i))	3 minus 20 =	* 0	X$ 25		OR	X$50	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	* 0	X100			X200	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180=			+360=	
			TOTAL			TOTAL	1100

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

APPLICATION DATA SHEET

APPLICATION INFORMATION

Application Type::	REGULAR
Subject Matter::	UTILITY
CD-ROM or CD-R?::	NONE
Title::	INFORMATION PROCESS DEVICE
Attorney Docket Number::	276900US90
Total Drawing Sheets::	3
Small Entity?::	NO

INVENTOR INFORMATION

Applicant Authority Type::	INVENTOR
Primary Citizenship Country::	Japan
Status::	FULL CAPACITY
Given Name::	Jun
Family Name::	HAISHIMA
City of Residence::	Tokyo
Country of Residence::	Japan
Street of Mailing Address::	3-1-25, Ariake, Koto-ku
City of Mailing Address::	Tokyo
Country of Mailing Address::	Japan
Postal or Zip Code of Mailing Address::	135-0063

CORRESPONDENCE INFORMATION

Correspondence Customer Number:: 22850

REPRESENTATIVE INFORMATION

Representative Customer Number:: 22850

DOMESTIC PRIORITY INFORMATION

FOREIGN PRIORITY INFORMATION

Application Number:	Country::	Filing Date::	Priority Claimed::
2004-245337	Japan	08/25/04	YES

Initial 08/17/05

ASSIGNMENT INFORMATION

Assignee Name::	Aruze Corp.
Street of Mailing Address::	3-1-25, Ariake, Koto-ku
City of Mailing Address::	Tokyo
Country of Mailing Address::	Japan
Postal or Zip Code of Mailing Address::	135-0063

Initial 08/17/05

Docket No. 276900US90

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jun HAISHIMA

SERIAL NO: New Application GAU:

FILED: Herewith EXAMINER:

FOR: INFORMATION PROCESS DEVICE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:
Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

☐ Attached is a list of applicant's pending application(s), published application(s) or issued patent(s) which may be related to the present application. In accordance with the waiver of 37 CFR 1.98 dated September 21, 2004, copies of the cited pending applications are not provided. Cited published and/or issued patents, if any, are listed on the attached PTO form 1449.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Masayasu Mori
Registration No. 47,301
C. Irvin McClelland
Registration Number 21,124

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 05/03)

Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO.	SERIAL NO.
		276900US90	New Application
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Jun HAISHIMA	
		FILING DATE	GROUP
		Herewith	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO	2003-330793	11/21/2003	Japan (with English Abstract)		X
	AP	2003-331236	11/21/2003	Japan (with English Abstract)		X
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	
	AX	
	AY	
	AZ	

☐ Additional References sheet(s) attached

Examiner

Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2003-330793
(43)Date of publication of application : 21.11.2003

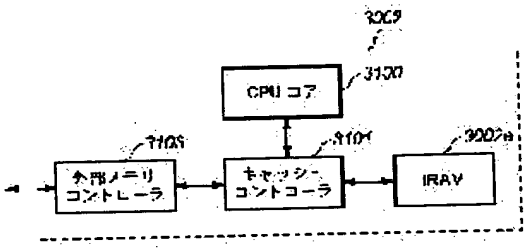
(51)Int.CI. G06F 12/08
G06F 12/06
G06F 12/16

(21)Application number : 2002-139065
(22)Date of filing : 14.05.2002

(71)Applicant : CANON INC
(72)Inventor : KAWANABE TETSUYA
AICHI TAKAO
MASUMOTO KAZUYUKI
SUWA TETSUYA
HAMAMOTO AKIHIKO
HIBI MAKOTO
OSHIMA MASATO
GOTOU FUMIHIRO
ONO MITSUHIRO

(54) INFORMATION PROCESSOR AND CONTROL METHOD THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To solve the problem in conventional equipment that a DRAM to be checked is used, prior to the check of the DRAM to be checked, to execute a check program therefor, and this contradicts the purpose of operation test of the DRAM.
SOLUTION: This information processor has a CPU, an IRAM 3002a connected to the local bus of the CPU, and a ROM and RAM connected to the external bus of the CPU. This processor further has a cache controller 3101 for varying the memory capacity to be used as cache memory according to the operation mode of the device of the memory capacity of the IRAM 3002a to make the IRAM 3002a usable as cache memory. Programs or data are stored in the memory area other than that used as the cache memory in the IRAM 3002a, and the check program stored in the IRAM 3002a is executed to perform a memory check.



LEGAL STATUS
[Date of request for examination]
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2003－330793
（Ｐ２００３－３３０７９３Ａ）
(43)公開日　平成15年11月21日(2003.11.21)

(51)Int.Cl.[7]	識別記号	FI			テーマコード（参考）
G06F 12/08	543	G06F 12/08	543	C	5B005
	523		523	C	5B018
	551		551	H	5B060
12/06	522	12/06	522	B	
12/16	330	12/16	330	B	

審査請求　未請求　請求項の数６　ＯＬ　（全14頁）

(21)出願番号　特願2002－139065(Ｐ2002－139065)

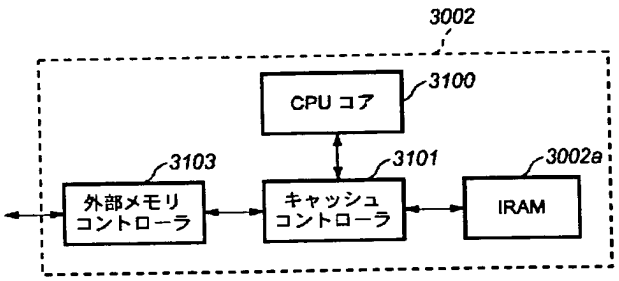
(22)出願日　平成14年５月14日(2002.5.14)

(71)出願人　000001007
キヤノン株式会社
東京都大田区下丸子３丁目30番２号
(72)発明者　河鍋　哲也
東京都大田区下丸子３丁目30番２号　キヤノン株式会社内
(72)発明者　愛知　孝郎
東京都大田区下丸子３丁目30番２号　キヤノン株式会社内
(74)代理人　100076428
弁理士　大塚　康徳　（外３名）

最終頁に続く

(54)【発明の名称】情報処理装置及びその制御方法

(57)【要約】
【課題】　チェック対象のＤＲＡＭをチェックする前に、そのチェックプログラムを実行するためにチェック対象のＤＲＡＭを使うことになってしまい、ＤＲＡＭの動作テストという目的からすると矛盾したことになる。
【解決手段】　ＣＰＵと、ＣＰＵのローカルバスに接続されたＩＲＡＭ３００２ａと、ＣＰＵの外部バスに接続されたＲＯＭ及びＲＡＭを備えた情報処理装置であって、ＩＲＡＭ３００２ａのメモリ容量の内、装置の動作モードに応じてキャッシュメモリとして使用するメモリ容量を可変にしてＩＲＡＭ３００２ａをキャッシュメモリとして利用可能にするキャッシュコントローラ３１０１を有し、ＩＲＡＭ３００２ａにおけるキャッシュメモリとして使用される以外のメモリ領域にプログラムやデータを格納し、そのＩＲＡＭ３００２ａに格納されたチェックプログラムを実行してメモリチェックを行う。



1

【特許請求の範囲】

【請求項１】　ＣＰＵと、当該ＣＰＵのローカルバスに接続された内蔵メモリと、前記ＣＰＵの外部バスに接続されたＲＯＭ及びＲＡＭを備えた情報処理装置であって、

前記内蔵メモリのメモリ容量の内、前記装置の動作モードに応じてキャッシュメモリとして使用するメモリ容量を可変にして前記内蔵メモリをキャッシュメモリとして利用可能にするキャッシュコントローラと、

前記内蔵メモリにおける前記キャッシュメモリとして使用される以外のメモリ領域にデータを格納するデータ格納制御手段と、を有することを特徴とする情報処理装置。

【請求項２】　前記データ格納制御手段は、前記メモリ領域に前記動作モードの情報を記憶することを特徴とする請求項１に記載の情報処理装置。

【請求項３】　前記ＲＡＭのメモリチェックが指示されると、前記ＲＯＭに記憶されているチェック用プログラムを前記内蔵メモリにコピーする手段を有し、前記ＣＰＵは前記内蔵メモリにコピーされた前記チェック用プログラムに基づいて前記ＲＡＭのメモリチェックを実行することを特徴とする請求項１に記載の情報処理装置。

【請求項４】　ＣＰＵと、当該ＣＰＵのローカルバスに接続された内蔵メモリと、前記ＣＰＵの外部バスに接続されたＲＯＭ及びＲＡＭを備えた情報処理装置における制御方法であって、

前記内蔵メモリのメモリ容量の内、前記装置の動作モードに応じてキャッシュメモリとして使用するメモリ容量を可変にして前記内蔵メモリをキャッシュメモリとして利用する工程と、

前記内蔵メモリにおける前記キャッシュメモリとして使用される以外のメモリ領域にデータを格納するデータ格納制御工程と、を有することを特徴とする情報処理装置における制御方法。

【請求項５】　前記データ格納制御工程では、前記メモリ領域に前記動作モードの情報を記憶することを特徴とする請求項４に記載の制御方法。

【請求項６】　前記ＲＡＭのメモリチェックが指示されると、前記ＲＯＭに記憶されているチェック用プログラムを前記内蔵メモリにコピーし、前記ＣＰＵは前記内蔵メモリにコピーされた前記チェック用プログラムに基づいて前記ＲＡＭのメモリチェックを実行することを特徴とする請求項４に記載の制御方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ＣＰＵの内蔵メモリをキャッシュメモリとして使用する情報処理装置とその制御方法に関するものである。

【０００２】

【従来の技術】近年、複数の機能モジュールを備える情

2

報処理装置では、ＲＯＭ上にプログラムやデータを記憶しておき、ＣＰＵがそのＲＯＭからプログラムやデータを逐次読み出して実行することにより所望の制御を行っている。また今日では、これら機器における機能が多種多様になってきている。例えば従来のプリンタ装置にメモリカードのスロットを設けて、そのスロットに装着されたメモリカードに記憶されている画像情報を読み出し、その画像情報に対してプリンタ自身で色処理など施して画像を記録するフォトダイレクトプリンタ装置がある。このような機器は、その処理スピードの高速化が望まれ、その機器を制御しているＣＰＵの駆動周波数がＲＯＭやＤＲＡＭなどの外部メモリへのアクセスピードよりも早いものが使われることが多い。このような高速ＣＰＵを採用した機器では、キャッシュメモリを備えて、できるだけ外部メモリへのアクセス回数を減少させるとともにプログラムの読み出しやデータ読み書きの際のＣＰＵウエイト時間を減少させている。

【０００３】

【発明が解決しようとする課題】このような従来の機器では、ＣＰＵがＲＯＭに書かれたプログラムを逐次読み出して実行する形式のもの（以後、従来例１と呼ぶ）、或いは、キャッシュメモリを備えた機器においては、機器の電源投入時などに、ＲＯＭに書かれたプログラムやデータなどを、一旦そのＲＯＭからＤＲＡＭにコピー或いは展開し、キャッシュメモリを併用してＤＲＡＭに記憶されたプログラムをＣＰＵが実行する形式（以後、従来例２と呼ぶ）がある。

【０００４】このような機器において、製品の信頼性を向上させる目的で制御基板の動作テストなどが実施され、例えばＣＰＵのワークメモリとして使用されるＤＲＡＭのリード／ライトチェックも必要になる。このようなチェックに際しては、従来例１の場合はＤＲＡＭへの読み書きをチェックするプログラムをＲＯＭに記憶しておき、このＲＯＭに書込まれているプログラムを実行してＤＲＡＭの読み書きテストをすることが考えられるが、この方式はＣＰＵがＲＯＭから逐次プログラムを読み出し実行することになり、このチェックに要する時間が長くなるという問題がある。

【０００５】また従来例２の方式では、一度、ＲＯＭのプログラムをＤＲＡＭに展開する必要があり、チェック対象のＤＲＡＭをチェックする前に、そのチェックプログラムを実行するためにチェック対象のＤＲＡＭを使うことになってしまい、ＤＲＡＭの動作テストという目的からすると矛盾したことになる。従って、もしも製造上の問題、或いはＤＲＡＭ部品の不良によりＤＲＡＭが正常に動作できないときは、このような読み書きチェック自体も正常に行なわれなくなる。

【０００６】本発明は上記従来例に鑑みてなされたもので、高速メモリであるＣＰＵ内蔵メモリを効率良く使用して、処理の高速化を図った情報処理装置及びその制御

方法を提供することを目的とする。

【０００７】

【課題を解決するための手段】上記目的を達成するために本発明の情報処理装置は以下のような構成を備える。即ち、ＣＰＵと、当該ＣＰＵのローカルバスに接続された内蔵メモリと、前記ＣＰＵの外部バスに接続されたＲＯＭ及びＲＡＭを備えた情報処理装置であって、前記内蔵メモリのメモリ容量の内、前記装置の動作モードに応じてキャッシュメモリとして使用するメモリ容量を可変にして前記内蔵メモリをキャッシュメモリとして利用可能にするキャッシュコントローラと、前記内蔵メモリにおける前記キャッシュメモリとして使用される以外のメモリ領域にデータを格納するデータ格納制御手段と、を有することを特徴とする。

【０００８】上記目的を達成するために本発明の情報処理装置における制御方法は以下のような工程を備える。即ち、ＣＰＵと、当該ＣＰＵのローカルバスに接続された内蔵メモリと、前記ＣＰＵの外部バスに接続されたＲＯＭ及びＲＡＭを備えた情報処理装置における制御方法であって、前記内蔵メモリのメモリ容量の内、前記装置の動作モードに応じてキャッシュメモリとして使用するメモリ容量を可変にして前記内蔵メモリをキャッシュメモリとして利用する工程と、前記内蔵メモリにおける前記キャッシュメモリとして使用される以外のメモリ領域にデータを格納するデータ格納制御工程と、を有することを特徴とする。

【０００９】

【発明の実施の形態】以下、添付図面を参照して本発明の好適な実施の形態を詳細に説明する。

【００１０】［装置本体の概略説明］図１は、本発明の実施の形態に係るフォトダイレクトプリンタ装置１０００の概観斜視図である。このフォトダイレクトプリンタ装置１０００は、ホストコンピュータ（ＰＣ）からデータを受信して印刷する、一般的なＰＣプリンタとしての機能と、メモリカードなどの記憶媒体に記憶されている画像データを直接読み取って印刷したり、或いはデジタルカメラからの画像データを直接受信して印刷する機能を備えている。

【００１１】図１において、本実施の形態に係るフォトダイレクトプリンタ装置１０００の外殻をなす本体は、下ケース１００１、上ケース１００２、アクセスカバー１００３及び排出トレイ１００４の外装部材を有している。また、下ケース１００１は、このプリンタ装置１０００の略下半部を、上ケース１００２は本体の略上半部をそれぞれ形成しており、両ケースの組合せによって内部に後述の各機構を収納する収納空間を有する中空体構造をなし、その上面部及び前面部にはそれぞれ開口部が形成されている。さらに、排出トレイ１００４は、その一端部が下ケース１００１に回転自在に保持され、その回転によって下ケース１００１の前面部に形成される開口部を開閉させ得るようになっている。このため、記録動作を実行させる際には、排出トレイ１００４を前面側へと回転させて開口部を開成させることにより、ここから記録シートが排出可能となると共に、排出された記録シートを順次積載し得るようになっている。また、排紙トレイ１００４には、２枚の補助トレイ１００４ａ，１００４ｂが収納されており、必要に応じて各トレイを手前に引き出すことにより、用紙の支持面積を３段階に拡大、縮小できるようになっている。

【００１２】アクセスカバー１００３は、その一端部が上ケース１００２に回転自在に保持され、上面に形成される開口部を開閉し得るようになっており、このアクセスカバー１００３を開くことによって本体内部に収納されている記録ヘッドカートリッジ（不図示）あるいはインクタンク（不図示）等の交換が可能となる。なお、ここでは特に図示しないが、アクセスカバー１００３を開閉させると、その裏面に形成された突起がカバー開閉レバーを回転させるようになっており、そのレバーの回転位置をマイクロスイッチなどで検出することにより、アクセスカバーの開閉状態を検出できるようになっている。

【００１３】また、上ケース１００２の右側には、液晶表示部１００６や各種キースイッチ等を備える操作パネル１０１０が設けられている。この操作パネル１０１０の構造は、図２を参照して詳しく後述する。１００７は自動給送部で、記録シートを装置本体内へと自動的に給送する。１００８は紙間選択レバーで、記録ヘッドと記録シートとの間隔を調整するためのレバーである。１００９はカードスロットで、ここにメモリカードを装着可能なアダプタが挿入され、このアダプタを介してメモリカードに記憶されている画像データを直接取り込んで印刷することができる。このメモリカード（ＰＣ）としては、例えばコンパクトフラッシュ（登録商標）メモリ、スマートメディア、メモリスティック等がある。１０１１はビューワ（液晶表示部）で、この装置本体に着脱可能であり、ＰＣカードに記憶されている画像の中からプリントしたい画像を検索する場合などに、１コマ毎の画像やインデックス画像などを表示するのに使用される。１０１２は後述するデジタルカメラを接続するための端子、１０１３は、パーソナルコンピュータ（ＰＣ）を接続するためのＵＳＢバスコネクタを示す。

【００１４】図２は、本実施の形態に係る操作パネル１０１０の概観図である。

【００１５】図において、液晶表示部１００６には、その左右に印刷されている項目に関するデータを各種設定するためのメニュー項目が表示される。ここでに表示される項目としては、印刷したい範囲の先頭写真番号、指定コマ番号（開始／－指定）、印刷を終了したい範囲の最後の写真番号（終了）、印刷部数（部数）、印刷に使用する用紙（記録シート）の種類（用紙種類）、１枚の

5

用紙に印刷する写真の枚数設定（レイアウト）、印刷の品位の指定（品位）、撮影した日付を印刷するかどうかの指定（日付印刷）、写真を補正して印刷するかどうかの指定（画像補正）、印刷に必要な用紙枚数の表示（用紙枚数）等がある。これら各項目は、カーソルキー２００１を用いて選択、或いは指定される。２００２はモードキーで、このキー２００２を押下する毎に、印刷の種類（インデックス印刷、全コマ印刷、１コマ印刷等）を切り替えることができ、これに応じてＬＥＤ２００３の対応するＬＥＤが点灯される。２００４はメンテナンスキーで、記録ヘッド１３０１のクリーニング等、プリンタのメンテナンスや印刷領域指定モードに入るためのキーである。２００５は印刷開始キーで、印刷の開始を指示する時、或いはメンテナンスの設定を確立する際に押下される。２００６は印刷中止キーで、印刷を中止させる時や、メンテナンスの中止を指示する際に押下される。

【００１６】また、この操作パネル１０１０の上部には、押下可能な電源スイッチ（Powerスイッチ）２００８及びレジュームスイッチ（Resume スイッチ）２００７と、プリンタエンジン３００４（図３）の動作状態を示す２色分のＬＥＤ２００９が配置されている。これらレジュームスイッチ２００７，電源スイッチ２００８からの各入力信号は、後述するＡＳＩＣ３００１（図３）のスイッチＩ／Ｆモジュールの管理のもとにプリンタエンジン３００４にも出力されている。

【００１７】次に図３を参照して、本実施の形態に係るフォトダイレクトプリンタ装置１０００の制御に係る主要部の構成を説明する。尚、この図３において、前述の図面と共通する部分は同じ記号を付与して、それらの説明を省略する。

【００１８】図３において、３０００は制御部（制御基板）を示している。３００１はＡＳＩＣ（専用カスタムＬＳＩ）を示している。３００２はＣＰＵで、後述する装置全体の各種制御処理及び、画像処理等を担当している。また、ＣＰＵ３００２の内部には、２次キャッシュとしても動作可能な６４ｋバイトの内臓ＲＡＭ（ＩＲＡＭ）３００２ａを併せもっている。３００３はメモリで、ＣＰＵ３００２の制御プログラムを記憶する２Ｍバイトのフラッシュ ＲＯＭ (FlashROM) ３００３ａ、及び実行時のプログラムを記憶し、画像データなどを記憶するためのワークメモリとして機能する８Ｍバイトの ＳＤＲＡＭ３００３ｂを有している。３００４はプリンタエンジンで、ここでは、複数色のカラーインクを用いてカラー画像を印刷するインクジェットプリンタのプリンタエンジンが搭載されている。３００５はデジタルカメラ３０１２を接続するためのポートとしてのＵＳＢバスコネクタである。３００６はビューワ１０１１を接続するためのコネクタである。３００８はＵＳＢバスハブ(USB HUB)で、このプリンタ装置１０００がＰＣ３０１０からの画像データに基づいて印刷を行う際には、ＰＣ３０１０からのデータをそのままスルーし、ＵＳＢバス３０２１を介してプリンタエンジン３００４に出力する。これにより、接続されているＰＣ３０１０は、プリンタエンジン３００４と直接、データや信号のやり取りを行って印刷を実行することができる（一般的なＰＣプリンタとして機能する）。３００９は電源コネクタで、電源３０１３により、商用ＡＣから変換された直流電圧を入力している。ＰＣ３０１０は一般的なパーソナルコンピュータ、３０１１は前述したメモリカード（ＰＣカード）、３０１２はデジタルカメラである。

6

【００１９】尚、この制御部３０００とプリンタエンジン３００４との間の信号のやり取りは、前述したＵＳＢバス３０２１又はＩＥＥＥ１２８４バス３０２２を介して行われる。

【００２０】更に、制御部３０００とプリンタエンジン３００４との間には、電源スイッチ２００８及びレジュームスイッチ２００７からの信号状態を示す２本のスイッチ信号線３０２３、及びプリンタエンジン３００４内部の制御モジュール（ＣＰＵやＡＳＩＣ）をリセットするためのエンジンリセット信号線３０２４が接続されている。２本のスイッチ信号線３０２３のそれぞれは、操作パネル１０１０に配置されたレジュームスイッチ２００７、電源スイッチ２００８のそれぞれの押下状態に対応した信号を伝えるが、後述するＡＳＩＣ３００１内部のスイッチＩ／Ｆ機能部の設定に応じて、これらスイッチ２００７，２００８の押下状態を直接プリンタエンジン３００４に伝送する（スルーモード）か、或いは、制御部３０００によってエミュレートした信号としてプリンタエンジン３００４に伝送する（ＣＰＵモード）かを選択可能になっている。

【００２１】図４は、ＣＰＵ３００２の機能構成を示すブロック図である。

【００２２】このＣＰＵ３００２の内部には、命令コードフェッチ回路、演算ユニット、レジスタなどを含むＣＰＵコア部３１００と、キャッシュメモリを制御するキャッシュコントローラ３１０１と、フラッシュＲＯＭ３００３ａ、ＡＳＩＣ３００１、ＳＲＡＭ３００３ｂなどの外部メモリ空間へアクセスするためのバス制御回路を含めた外部メモリコントローラ３１０３と、２次キャッシュメモリとしても動作可能な６４ｋバイトの高速メモリで構成されたＩＲＡＭ３００２ａとを備えている。

【００２３】なお、本実施の形態に係るキャッシュコントローラ３１０１では、ＩＲＡＭ３００２ａ内に、１６ｋバイト単位で２次キャッシュメモリとして使う領域をプログラム処理によりＣＰＵコア３１００が任意に設定できる。また、本実施の形態におけるキャッシュコントローラ３１０１は、１次キャッシュメモリとして、命令コードキャッシュ用とデータキャッシュ用にそれぞれ４ｋバイトのメモリを備えた所謂ハーバードアーキテクチ

ヤ構成となっている。キャッシュコントローラ３１０１は、ＣＰＵコア３１００よりの命令コードを読み出し、データの読み書き要求に応じて、１次キャッシュにその命令コードやデータがあれば（ヒット）、その１次キャッシュから命令コードやデータの読み出しやデータの書き込みを高速に行うことができる。また１次キャッシュにその命令コードやデータがなく（ミスヒット）、２次キャッシュ（ＩＲＡＭ）にその命令コードやデータがあれば（ヒット）、その２次キャッシュからその命令やデータの読み出しやデータの書き込みを行い、ミスヒットしたときは外部メモリコントローラ３１０３を介して外部メモリ空間へのアクセスを行うようになっている。

【００２４】このとき例えばＳＤＲＡＭ３００３ｂへのアクセスは所定ワード数単位でバーストモードで高速に読み書きする。これとともに２次キャッシュ（ＩＲＡＭ）が有効な場合は、その２次キャッシュにその命令コードやデータを格納し、同時に１次キャッシュにその命令コードやデータを格納しておいて、ＣＰＵコア３１００から要求された命令コードの読み出しやデータの読み書き動作を行う。尚、これら１次キャッシュ及び２次キャッシュ領域は有限なので、ＣＰＵコア３１００からの要求により、１次キャッシュが溢れる場合には、その溢れてしまう命令コードやデータを１次キャッシュから２次キャッシュ（ＩＲＡＭ）に移動する。更に２次キャッシュが溢れる場合には、その溢れてしまうデータ中にＳＤＲＡＭ３００３ｂへの未書込みデータがあるときには、ＳＤＲＡＭ３００３ｂへ所定ワード数単位でバーストモードににより高速に書込み動作させるキャッシュフラッシュ動作を行う。また、ＩＲＡＭ３００２ａにおける２次キャッシュ領域以外の領域も高速メモリとして使うこともできるようになっている。以上のような構成を採用することで、この装置における制御処理スピードを高速化している。

【００２５】図５は、ＡＳＩＣ３００１の構成を示すブロック図で、この図５においても、前述の図面と共通する部分は同じ記号を付与して、それらの説明を省略する。

【００２６】４００１はＰＣカードインターフェース（Ｉ／Ｆ）部で、装着されたＰＣカード３０１１に記憶されている画像データを読取ったり、或いはＰＣカード３０１１へのデータの書き込み等を行う。４００２はＩＥＥＥ１２８４インターフェース部で、プリンタエンジン３００４との間のデータのやり取りを行う。このＩＥＥＥ１２８４Ｉ／Ｆ部４００２は、デジタルカメラ３０１２或いはＰＣカード３０１１に記憶されている画像データを印刷する場合に使用されるバスである。４００３はＵＳＢインターフェース部で、ＰＣ３０１０との間でのデータのやり取りを行う。４００４はＵＳＢホストインターフェース部で、デジタルカメラ３０１２との間でのデータのやり取りを行う。４００５は操作パネル・インターフェース部で、操作パネル１０１０からの各種操作信号を入力したり、表示部１００６への表示データの出力などを行う。４００６はビューワ・インターフェース部で、ビューワ１０１１への画像データの表示を制御している。４００７aおよび４００７ｂは各種スイッチやＬＥＤ４００９等との間のインターフェースを制御するスイッチ・インターフェース部である。

【００２７】４０１１は、プリンタエンジン３００４のリセット制御を行うレジスタである。このエンジンリセット・レジスタ４０１１は、他のＡＳＩＣ内の各モジュールがリセットスタート（リセット信号により起動）後にはＡＳＩＣ３００１によって自動的に初期化されるのと異なり、リセットスタート後も自動的には初期化されることはなく、完全に電力供給がなくなった時に初めて初期化される。つまり、このレジスタ４０１１の設定値を参照することにより、単純なリセットスタートであるのか、或いはＡＣ電源から電源３０１３を切り離す（電源供給断）ことによる純粋なハードリセットであるかを判別することができる。

【００２８】本実施の形態においては、電源オン中に電源スイッチ２００８が押下される（電源オフ指示）とプリンタエンジン部３００４が電源オフ動作を開始する。そして、その電源オフ動作が終了するとその旨を検出して、図９のステップＳ１９の電源断処理（PowerDown）に進み、スイッチＩ／Ｆ（４００７ａ，ｂ）を通して電源スイッチ２００８の押下によるＣＰＵ３００２にリセットを掛ける設定として、不要なクロック動作を停止させて省電力モードに移行する。この状態のときに電源スイッチ２００８が再び押下されるとリセットが掛かり、システムが起動できるようになっている。４００８はＣＰＵインターフェース部で、ＣＰＵ３００２との間でのデータのやり取りの制御を行っている。４０１０はこれら各部を接続する内部バス（ＡＳＩＣバス）である。

【００２９】上述したように本実施の形態に係るフォトダイレクトプリンタ装置１０００では、ＣＰＵ３００２が、図３のメモリ３００３に記憶された制御プログラムに従って、画像処理に加えて、装置の各部の制御をも実行している。

【００３０】この制御プログラムは、機能モジュールごとにタスク化したマルチタスク形式で構成されており、そのタスク構成の主なものを示すと図６のようになる。

【００３１】図６は、本実施の形態に係るフォトダイレクトプリンタ装置１０００におけるタスクの構成を示すブロック図である。

【００３２】図６において、８０００はシステムコントロールタスクで、各タスク間でのイベント発行、イベントの終了に伴うシーケンス制御や排他処理等、システム全体の調停を行っている。８００１はキーイベントタスクを示し、操作パネル１０１０のキー操作に基づいて、押下されたキーの解析等を行う。８００２はＬＣＤ表示

部１００６への表示タスクを示し、この表示タスクは表示部１００６におけるＵＩ制御或はメッセージ表示要求等が発生した時点で起動され、表示部１００６への表示制御を実行している。８００３はＰＣカード３０１１への読み書きによるデータの入出力により起動されるタスクを示す。８００４はＵＳＢバスを介して接続されるＰＣ３０１０からのデータ転送制御するＵＳＢプリンタタスクで、ＵＳＢのプリンタ割り込みにより起動され、ＰＣプリンタとしての機能を実行する。８００５は、システムコントロールタスク８０００により起動されるＵＳＢストレージタスクで、ＵＳＢＩ／Ｆを通じてＰＣ３０１０との間でコマンドやデータのやり取り行い、ＰＣ３０１０の要求に応じ、ＰＣカード部８００３と連携してＰＣカード３０１１への読み書き制御を行う。また、システムコントロールタスク８０００からのメッセージに応じて、下位タスクであるＵＳＢコントロールタスク、ＵＳＢバルクタスクの起動・終了を行う。８００６は擬似ホストタスクで、ＵＳＢを介して接続されるデジタルカメラ３０１２からのデータの読込みや各種通信制御等を実行する。８００７はファイルタスクで、ファイルのオープン、クローズ、リード、ライト等の入出力制御を行う。

【００３３】８００８はプリンタエンジン３００４と接続されるセントロニクス・インターフェースの通信制御を行うセントロニクスタスクで、印刷データのＤＭＡ送信、ステータス応答等を実行する。８００９は画像処理タスクで、ＲＧＢデータを受取り、３Ｄ処理、四面体補完、色変換やスケーリング及び誤差拡散処理などによりＹＭＣＫデータを作成し、最終的にプリンタエンジン３００４に出力するラスタイメージデータを作成する。８０１０はページ・クリエイトタスクで、ＪＰＥＧデータを伸長して画像データに変換したり、或はＢＭＰ形式のデータからイメージデータを作成したり、或はＨＴＭＬ文書からイメージデータを作成するとともに、フォトデータの補正、階調補正等の画像処理やＲＧＢデータの作成等を行っている。８０１１はビューワタスクで、ビューワ１０１１が接続されている状態で、ビューワ１０１１への表示制御を実行している。

【００３４】次に、命令コードやデータを含む制御コードの、メモリマップ上での配置について、図７乃至図８に示すメモリマップを参照して説明する。

【００３５】図７は、ＩＲＡＭ３００２ａのメモリマップを説明する図で、それぞれの動作モードでの使用方法をＩＭ１～ＩＭ４で示している。

【００３６】図８は、フラッシュＲＯＭ３００３ａのメモリマップ（ＲＯＭ）と、ＳＤＲＡＭ３００３ｂのメモリマップ（ＳＤＲＡＭ）を説明する図である。

【００３７】上記制御コードは、電気的に書き換え可能な２Ｍバイトのフラッシュ ＲＯＭ３００３ａに格納されていて、図８のメモリアップ（ＲＯＭ）に示したように、本実施の形態では、２Ｍバイト中の上位６４ｋバイト、つまり、Ｐ１にリセットスタート時に必要な特殊コードを配置し、残り部分（Ｐ２）には通常コード、つまり、後述する図９中のステップＳ３～Ｓ１９で示す処理用の制御コードなどを配置している。

【００３８】特殊コード部（Ｐ１）には、後述する図１０（ローダ）及び図１１（スタートアップ）の制御フローで示されるプログラムが格納されており、１ｋバイトのローダ（Loader）部（Ａ１）と、７ｋバイトのスタートアップ（StartUP）部（Ａ２）、及び５６ｋバイトのアップデート（Update）部（Ａ３）とがある。

【００３９】通常コード部（Ｐ２）には、ＣＰＵの割り込みベクタ処理用のプログラム部分であるシステムベクタ（SystemVector）部（Ａ４）と、Ｐ２に格納してある後述の図１１で説明する電源断（PowerDown）処理へＰ１からジャンプするためのアドレスなどを格納してあるジャンプテーブル（JTBL）（Ａ５）と、電源断処理の制御コードを格納しているPowerDown（Ａ６）と、前述の図６を参照して説明した各タスクの制御コードを格納している通常プログラム部（Ａ７）と、データ部（Ａ８）と、及び、後述の図１１で説明するＲＡＭチェック処理用の制御コードを格納してあるチェッカー部（Ａ９）とが格納されている。

【００４０】次に、前述の特殊コード（Ｐ１）と通常コード（Ｐ２）との関連について図９以降のフローチャートを参照して説明する。

【００４１】図９は、本実施の形態に係るフォトダイレクトプリンタ装置１０００の全体的な処理の流れを示すフローチャートである。

【００４２】この処理は制御部３０００のリセットが解除されることにより開始され、まずステップＳ１で、ハードウェアによって自動的にフラッシュＲＯＭ３００３ａの先頭から１ｋバイトのローダ部（図８のＡ１）が、ＣＰＵ３００２のＩＲＡＭ３００２ａの先頭から１ｋバイト（図７のＢ１）にロードされ、ＩＲＡＭ３００２ａの先頭番地からのローダ部の制御コードが実行される。このときＩＲＡＭ３００２ａは、図７のＩＭ１で示すようにマッピングされていて、２次キャッシュは禁止状態である。このようにしてステップＳ１より制御プログラムの実行を開始する。

【００４３】このローダ部の制御コードに基づく処理を示すフローチャートが図１０に示されている。

【００４４】図１０において、まずステップＳ１００で、ＣＰＵ内臓レジスタの初期化を行い、次にステップＳ１０１に進み、図７のＩＭ２で示したＢ５部分に、３２ｋバイトの２次キャッシュメモリ（L2Cache）配置させる。次にステップＳ１０２に進み、フラッシュＲＯＭ３００３ａの図８のＡ２に格納されているスタートアップ制御コードをＩＲＡＭ３００２ａの図７のＢ４にロードする。そしてステップＳ１０３に進み、後述のスター

11

トアップ・プログラムなどが動作する上で必要になるスタックメモリ領域を、図７のＢ２に配置させるようにスタックポインタなどを設定してローダ部の処理を終了する（ＩＭ2）。

【００４５】次に、こうしてステップＳ１０２でＩＲＡＭ３００２ａにロードされたスタートアップ部の制御コードを図９のステップＳ２で実行する。

【００４６】図１１は、図９のステップＳ２のスタートアップ制御処理を示すフローチャートである。

【００４７】このスタートアップ部の処理においては、まずステップＳ２００で、エンジンリセット・レジスタ４０１１の内容を読み出し、エンジンリセットが解除済みかどうかを調べる。解除済みでなければ、ＡＣプラグをＡＣ電源と接続することによる電源投入であるため、「モード１」～「モード５」のいずれかであるかを判定する。ここでは、電源投入時に押下されている操作パネル１０１０のスイッチの押下状態の組み合わせに応じて「モード１」～「モード５」のいずれかが選択される。例えば、レジュームスイッチ２００７，電源スイッチ２００８、及び所定のスイッチが全てオフ状態のときを「モード１」とすると、この「モード１」では通常のＡＣオン時の処理を開始し、ステップＳ２１０でフラッシュＲＯＭ３００３ａのＪＴＢＬ（Ａ５）～PowerDown（Ａ６）のみをＳＤＲＡＭ３００３ｂにコピーし、ＰＩＮＦ（Ｂ３）のモードを「パワーオン待機モード」とし、ＪＴＢＬ（Ａ５）を介して図９のステップＳ１９にジャンプして電源断処理を実行する。

【００４８】このステップＳ１９の電源断処理では、エンジンリセット・レジスタ４０１１を操作してプリンタエンジン３００４のリセットを解除し、スイッチＩ／Ｆ（４００７ａ，ｂ）をスルーモードに切り替えるとともに、電源スイッチ２００８の押下によりＣＰＵ３００２にリセットを掛ける設定として、不要なクロック動作を停止させて省電力モードに移行する。この後、電源スイッチ２００８が再び押下されることによりＣＰＵ３００２にリセットが掛かり、これと同時にプリンタエンジン３００４を起動させる。そしてＣＰＵ３００２のリセットによりステップＳ１より起動されると、図１１のステップＳ２００の判定で、今度はエンジンリセットが解除済みとなるので、ステップＳ２６０に進んで「通常モード」での処理に移行する。

【００４９】「モード２」は、製造工程などにおける基板チェック工程用の検査モードである。この検査モードは、ＳＤＲＡＭ３００３ｂのリード／ライトチェックを行うもので、まずステップＳ２２０で、２次キャッシュを禁止し、図７のＩＭ2マップからＩＭ3マップに切り替える準備を行う。次にステップＳ２２１に進み、フラッシュＲＯＭ３００３ａに格納されているChecker制御コード（図８のＡ９）をＩＲＡＭ３００２ａのＢ６へロードする（ＩＭ3）。次にステップＳ２２２に進み、そ

12

のChecker処理を実行してＳＤＲＡＭ３００３ｂのリード／ライトチェックを行う。このステップＳ２２２でＳＤＲＡＭ３００３ｂをテストした結果をＰＩＮＦ（Ｂ３）に格納しておく。ここで例えばエラーであった場合には、これ以上プログラムを動作させてＳＤＲＡＭ３００３ｂを使用すると暴走などの危険があるので、ＡＳＩＣ３００１の特殊ポートなどにその旨を出力して動作を停止させる。一方、正常であった場合はステップＳ２２３に進み、再びＩＲＡＭ３００２ａのメモリマップをＩＭ2マップに切り替えるために２次キャッシュを３２ｋバイト設定にして、モードを「検査モード１」とする。

【００５０】「モード３」及び「モード４」は、製造工程などにおける検査モードである。この検査モードでは、各々ステップＳ２３０でモードを「検査モード２」、もしくはステップＳ２４０でモードを「検査モード３」と設定する。

【００５１】「モード５」は、フラッシュＲＯＭ３００３ｂを書き換えるアップデートモードである。この場合は、まずステップＳ２５０で、フラッシュＲＯＭ３００３ａに格納されているアップデート制御コード（図８のＡ３）をＳＤＲＡＭ３００３ｂのワーク２（Ｃ１）へコピーする。次にステップＳ２５１に進み、フラッシュＲＯＭ３００３ａのアップデート処理を実行する。このステップＳ２５１では、ＰＣカード３０１１に格納された制御コードをフラッシュＲＯＭ３００３ｂに書き込むために、ＰＣカード３０１１に格納されている所定の形式のアップデートデータを読み出し、一旦、ＳＤＲＡＭ３００３ｂのワーク３（Work3）領域（図８のＣ３）に２Ｍバイトのフラッシュ ＲＯＭイメージのデータ（図８のＰ３に相当）として展開する。

【００５２】このアップデートには、フラッシュＲＯＭ３００３ａのＰ１を変更せずにＰ２だけを変更する部分アップデート方法と、フラッシュＲＯＭ３００３ａ全体（Ｐ３）を変更する全面アップデート方法があり、このアップデートデータの所定の制御コードにより、このようなアップデート方法が識別できるようになっている。ここで前者（部分アップデート）の場合には、フラッシュＲＯＭ３００３ａのＰ２部を消去し、ＳＤＲＡＭ３００３ｂのワーク領域（Ｃ３）に展開したＰ２部に相当する部分のみを、フラッシュＲＯＭ３００３ａのＰ２に書き込む。また後者（全体アップデート）の場合には、フラッシュＲＯＭ３００３ａの全領域（Ｐ３）を消去し、ＳＤＲＡＭ３００３ｂのワーク領域（Ｃ３）に展開したもの全てをフラッシュＲＯＭ３００３ａに書き込む。こうしてフラッシュＲＯＭ３００３ａのアップデートが正常に終了するとステップＳ２５２に進み、モードを「アップデートモード」としておく。

【００５３】またステップＳ２００において、図９のステップＳ１９の電源断処理にて、スイッチＩ／Ｆ（４００７ａ，ｂ）を電源スイッチ２００８の押下によりＣＰ

13

Ｕ３００２にリセットを掛ける設定として、不要なクロック動作を停止させて省電力モードに移行させる。その後、電源スイッチ２００８が再び押下されてリセットされたときには既にプリンタエンジン３００４のエンジンリセットが解除済みなので「モード０」と判定され、ステップＳ２６０に進んで、モードを「通常モード」にする。

【００５４】以上のようにして各種モードが確定するとステップＳ２７０に進み、各種モードをＩＲＡＭ３００２ａのＰＩＮＦ領域（Ｂ３）に格納する。次にステップＳ２７１に進み、それ以降の処理をできるだけ高速に実行させるように、図７に示すＩＭ４のマップに切り替えるために、２次キャッシュを４８ｋバイト設定にする。そしてステップＳ２７２に進み、フラッシュＲＯＭ３００３ａのＪＴＢＬ（Ａ５）～通常プログラム（Ａ７）部分をＳＤＲＡＭ３００３ｂの通常プログラム領域（Ｃ２）にコピーする。そしてC_INTへジャンプする。これにより図９のステップＳ３に進み、フラッシュＲＯＭ３００３ａに格納されているシステムベクタ部（Ａ４）をＩＲＡＭ３００２ａの先頭領域（Ｂ９）にコピーしてＣＰＵ３００２の割り込み処理などを実行できるようにしておく。

【００５５】次にステップＳ４に進み、以降のステップＳ５～Ｓ１８で示したタスクなどを動作させるべくＯＳを起動する。こうしてＯＳが起動されると、このＯＳのコンフィギュレーション情報に従って、ステップＳ５で初期化タスク（Initializer）が起動される。

【００５６】次に、図１２及び図１３を参照して、図９のステップＳ５の初期化タスク処理を説明する。

【００５７】図１２は、図９のステップＳ５の初期化処理（Initializer）を説明するフローチャートである。

【００５８】まずステップＳ３００で、ＡＳＩＣ３００１のエンジンリセットレジスタ（４０１１）及びスイッチＩ／Ｆ（４００７ａ，ｂ）以外のレジスタなどを必要に応じて初期化する。次にステップＳ３０１に進み、ＯＳの時間管理機能を動作させるためにタイマを起動する。そしてステップＳ３０２に進み、必要に応じてプリンタエンジン３００４のリセット解除してプリンタエンジン３００４を起動させる。

【００５９】図１３は、ステップＳ３０２のエンジン信号の初期化処理を説明するフローチャートである。

【００６０】まずステップＳ４００において、ステップＳ２７０でＩＲＡＭ３００２ａのＰＩＮＦ領域（Ｂ３）に格納されているモード情報を参照し、「検査モード１」若しくは「検査モード２」かどうかを調べ、そうであればこの処理を終了する。つまり「検査モード１」（「モード２」）若しくは「検査モード２」（「モード３」）のときはエンジンリセット解除しない。

【００６１】一方ステップＳ４００で、「通常モード」、「検査モード３」或いは「アップデートモード」の場合はステップＳ４０１に進み、スイッチＩ／Ｆ（４００７ａ，ｂ）をスルーモードに切り替える。次にステップＳ４０２進み、エンジンリセットレジスタ４０１１を参照してエンジンリセットが解除済みかどうか、即ち、「通常モード」かどうかを調べ、そうであればステップＳ４１０に進む。ステップＳ４１０では「アップデートモード」かどうかを調べ、そうでなければ本処理を終了する。

【００６２】ステップＳ４０２で、エンジンリセット解除済みでないとき、即ち、「検査モード３」若しくは「アップデートモード」の場合にはステップＳ４０３に進み、エンジンリセットを解除し、次にステップＳ４０４に進んで、プリンタエンジン３００４のリセット処理が終了して、電源スイッチ２００８がオンされたのを検知することによりプリンタエンジン３００４がパワーオン動作できるようになるまで約２秒ほど待つ。そしてステップＳ４１０に進み、「アップデートモード」かどうかをみる。そうでなければ、即ち、「通常モード」若しくは「検査モード３」であれば本処理を終了する。

【００６３】一方、ステップＳ４１０で「アップデートモード」であればステップＳ４１１～Ｓ４１６において、プリンタエンジン３００４を自動的にパワーオンさせる。即ち、ステップＳ４１１で、スイッチＩ／Ｆ（４００７ａ，ｂ）をＣＰＵモード（スイッチ信号をＣＰＵによりエミュレートする）に切り替え、次にステップＳ４１２で、プリンタエンジン３００４に対する電源スイッチ信号（信号線３０２３）をオン状態で出力する。そしてステップＳ４１３で、プリンタエンジン３００４が電源スイッチ２００８のオン状態を十分に認識できるように約５０ｍ秒の間待つ。そしてステップＳ４１４に進み、電源スイッチ信号（信号線３０２３）をオフ状態にする。そしてステップＳ４１５に進み、スイッチＩ／Ｆ（４００７ａ，ｂ）をスルーモードに切り替えてステップＳ４１６に進み、プリンタエンジン３００４がパワーオン状態に移行するのを待って本処理を終了する。

【００６４】以上のようにして、ステップＳ３０２のエンジン信号初期化処理が終了するとステップＳ３０３（図１２）に進み、ＩＲＡＭ３００２ａのＰＩＮＦ領域（Ｂ３）に格納されているモード情報を参照する。ここで「検査モード１」或いは「検査モード２」が格納されているときはステップＳ３０５に進み、チェッカタスク（図９のＳ１８）を起動する。このチェッカタスク（Ｓ１８）は、製造ラインなどにおけるテスタとＵＳＢＩ／Ｆ４００３を接続して、このインターフェースにより、特殊なコマンドの受信やステータスの送信を行うことにより、基板などのチェックなどを行うものである。例えば、「検査モード１」の時には、ステップＳ２２２で実行したＳＤＲＡＭ３００３ｂのチェックの結果を返送するコマンドやステータスの返送が用意されている。

【００６５】一方、ステップＳ３０３で、「通常モー

ド」、「検査モード３」或いは「アップデートモード」の場合はステップＳ３０４へ進み、通常の即ち、図９のステップＳ７～Ｓ１７で示した各種タスクを起動すべくシステムコントロールタスク（Ｓ６）を起動する。

【００６６】ステップＳ６～Ｓ１７は上記図６で説明した制御プログラムで、機能モジュールごとにタスク化したマルチタスク形式で構成されている。ＩＲＡＭ３００２ａのワーク領域（図７のＢ８）や、ＳＤＲＡＭ３００３ｂのワーク２領域（図８のＣ１）およびワーク３領域（図８のＣ３）は、プログラムが実行する上での作業メモリ領域として使用され、ここで実行されるプログラムは、ＳＤＲＡＭ３００３ｂの通常プログラム領域（図８のＣ２）に全て格納され、ＳＤＲＡＭ３００３ｂの全体に対して１次キャッシュ及び２次キャッシュの動作対象とするようにして装置全体の処理スピードを高速化している。

【００６７】図９のステップＳ６は、図６の８０００で示したシステムコントロールタスクで、各タスク間でのイベント発行、イベントの終了に伴うシーケンス制御や排他処理等、システム全体の調停を行っている。「通常モード」の場合にはステップＳ７～Ｓ１７で示す全てのタスクを起動して通常動作モードを実行する。また「検査モード３」若しくは「アップデートモード」の場合には、キーイベントタスク（Ｓ７）とＬＣＤディスプレイタスク（Ｓ８）のみを特殊モードで起動して、フラッシュＲＯＭ３００３ａのバージョン情報などを表示部１００６に表示して電源スイッチ２００８の押下を待つ。

【００６８】図９のステップＳ７は、図６の８００１で説明したキーイベントタスクを示し、操作パネル１０１０のキー操作により押下されたキーの解析等を行う。

【００６９】図９のステップＳ８は、図６の８００２で説明したＬＣＤ表示部１００６への表示タスクを示し、表示部１００６におけるＵＩ制御或はメッセージ表示要求等が発生した時点で起動され、ＬＣＤ表示部１００６への表示制御を実行している。

【００７０】図９のステップＳ９は、図６の８０１１で説明したビューワタスクで、ビューワ１０１１が接続されている状態で、ビューワ１０１１への表示制御を実行している。ステップＳ１０は、図６の８００３で説明したＰＣカード３０１１への読み書きによるデータの入出力により起動されるタスクを示す。またステップＳ１１は、図６の８００７で説明したファイルタスクで、ファイルのオープン、クローズ、リード、ライト等の入出力制御を行う。ステップＳ１２は、図６の８００４で説明したＵＳＢバスを介して接続されるＰＣ３０１０からのデータ転送により起動されるＵＳＢプリンタタスクで、ＵＳＢのプリンタ割り込みにより起動され、ＰＣプリンタとしての機能を実行する。またステップＳ１３は、図６の８００６で説明した擬似ＵＳＢホストタスクで、ＵＳＢを介して接続されるデジタルカメラ３０１２からのデータの読込みや各種通信制御等を実行する。

【００７１】図９のステップＳ１４は、図６の８００５で説明したＵＳＢストレージタスクで、システムコントロールタスク８０００からのメッセージに応じて、下位タスクであるＵＳＢコントロールタスク、ＵＳＢバルクタスクの起動・終了を行う。またステップＳ１５は、図６の８０１０で説明したページ・クリエイトタスクで、ＪＰＥＧデータを伸長して画像データに変換したり、或はＢＭＰ形式のデータからイメージデータを作成したり、或はＨＴＭＬ文書からイメージデータを作成するとともに、フォトデータの補正、階調補正等の画像処理やＲＧＢデータの作成等を行っている。またステップＳ１６は、図６の８００９で説明した画像処理タスクで、ＲＧＢデータを受取り、３Ｄ処理、四面体補完、色変換やスケーリング及び誤差拡散処理などによりＹＭＣＫデータを作成し、最終的にプリンタエンジン３００４に出力するラスタイメージデータを作成する。また、ここではＩＲＡＭ３００２ａのワーク１領域（図７のＢ８）を使用して画像処理速度を高速化している。更に、ステップＳ１７は、図６の８００８で説明したセントロタスクで、プリンタエンジン３００４と接続されるセントロニクス・インターフェースを制御し、印刷データのＤＭＡ送信、ステータス応答等を実行する。

【００７２】また、電源スイッチが押下されプリンタエンジン３００４がパワーオフ状態に遷移すると、その旨をキーイベントタスク（Ｓ７）が検知してパワーオフ要求をシステムコントロールタスク（Ｓ６）に送り、システムコントロールタスク（Ｓ６）は前述したステップＳ１９の電源断処理を実行し、スイッチＩ／Ｆ（４００７ａ，ｂ）を電源スイッチ２００８の押下によりＣＰＵ３００２にリセットを掛ける設定として、不要なクロック動作を停止させ省電力モードに移行させる。

【００７３】以上説明したように、本実施の形態に係るフォトダイレクトプリンタ装置１０００によれば、全体として高速に動作させることができる。

【００７４】（その他の実施の形態）本発明の目的は前述したように、実施形態の機能を実現するソフトウェアのプログラムコードを記録した記憶媒体をシステム或は装置に提供し、そのシステム或は装置のコンピュータ（又はＣＰＵやＭＰＵ）が記憶媒体に格納されたプログラムコードを読み出し実行することによっても達成される。この場合、記憶媒体から読み出されたプログラムコード自体が前述した実施形態の機能を実現することになり、そのプログラムコードを記憶した記憶媒体は本発明を構成することになる。このようなプログラムコードを供給するための記憶媒体としては、例えば、フロッピィディスク、ハードディスク、光ディスク、光磁気ディスク、ＣＤ－ＲＯＭ，ＣＤ－Ｒ、磁気テープ、不揮発性のメモリカード、ＲＯＭなどを用いることができる。

【００７５】また、コンピュータが読み出したプログラ

17

ムコードを実行することにより、前述した実施の形態の機能が実現されるだけでなく、そのプログラムコードの指示に基づき、コンピュータ上で稼動しているＯＳ（オペレーティングシステム）などが実際の処理の一部又は全部を行い、その処理によって前述した実施の形態の機能が実現される場合も含まれている。

【００７６】更に、記憶媒体から読み出されたプログラムコードが、コンピュータに挿入された機能拡張ボードやコンピュータに接続された機能拡張ユニットに備わるメモリに書きこまれた後、そのプログラムコードの指示に基づき、その機能拡張ボードや機能拡張ユニットに備わるＣＰＵなどが実際の処理の一部又は全部を行い、その処理によって前述した実施の形態の機能が実現される場合も含む。

【００７７】以上説明したように本実施の形態によれば、例えばＤＲＡＭの動作テストの場合は、キャッシュメモリを使用禁止状態に設定し、高速メモリにＤＲＡＭのチェックプログラムを読み込んで動作させることにより、ＤＲＡＭの動作テストを高速化できる効果がある。

【００７８】またリセット時の各種モード状態を、高速のキャッシュメモリの一部に格納することにより、高速に各種モードを判定することができる。

【００７９】更に、画像処理等に際して、高速のキャッシュメモリの一部を利用することで、機器のコストを上昇することなく高速な画像処理も可能となる効果がある。

【００８０】

【発明の効果】以上説明したように本発明によれば、高速メモリであるＣＰＵ内蔵メモリを効率良く使用して、処理の高速化を図ることができる。

【図面の簡単な説明】

18

【図１】本発明の実施の形態に係るフォトダイレクトプリンタ装置の概観斜視図である。

【図２】本実施の形態に係るフォトダイレクトプリンタ装置の操作パネルの概観図である。

【図３】本実施の形態に係るフォトダイレクトプリンタ装置の制御に係る主要部の構成を示すブロック図である。

【図４】図３に示すＣＰＵの主要部の構成を示すブロック図である。

【図５】図３に示すＡＳＩＣの構成を示すブロック図である。

【図６】本実施の形態に係るフォトダイレクトプリンタ装置の制御プログラムにおいて機能モジュールごとにタスク化されたマルチタスク構成を説明する図である。

【図７】本実施の形態に係るフォトダイレクトプリンタ装置のＣＰＵ内蔵ＲＡＭ（ＩＲＡＭ）のメモリマップを説明する図である。

【図８】本実施の形態に係るフォトダイレクトプリンタ装置のフラッシュＲＯＭ及びＳＤＲＡＭのメモリマップを説明する図である。

【図９】本実施の形態に係るフォトダイレクトプリンタ装置の制御動作を説明するフローチャートである。

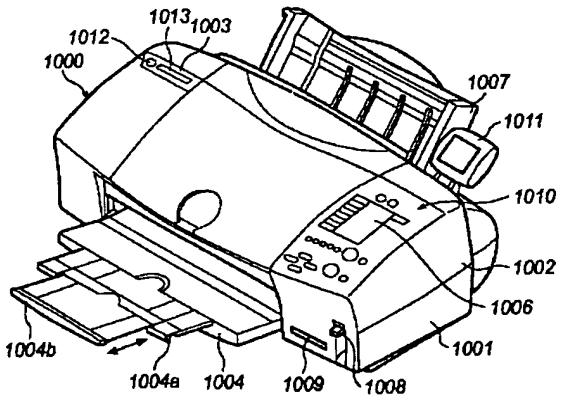
【図１０】図９のステップＳ１におけるローダ部の処理を説明するフローチャートである。

【図１１】図９のステップＳ２におけるスタートアップ部の処理を説明するフローチャートである。

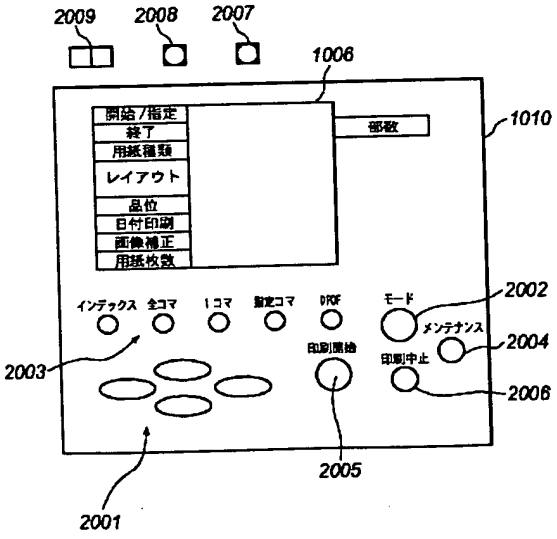
【図１２】図９のステップＳ５における初期化部の処理を説明するフローチャートである。

【図１３】図１２のステップＳ３０２におけるエンジン信号初期化部の処理を説明するフローチャートである。

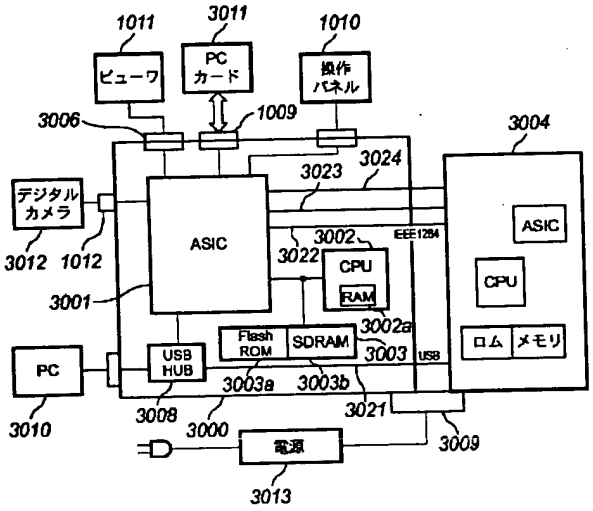
【図１】



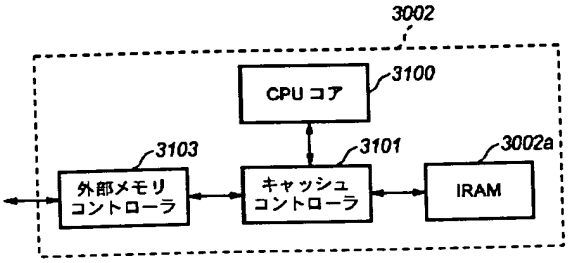
【図２】



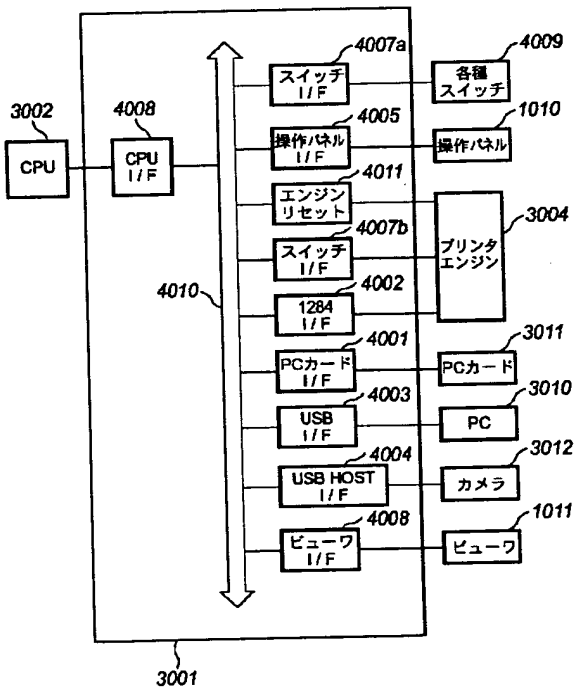
【図３】


1011
3011
1010
ビューワ
PC カード
操作 パネル
1009
3006
3004
3024
3023
デジタル カメラ
ASIC
ASIC
3002
EEE1284
3022
CPU
CPU
RAM
3012
1012
3001
3002a
Flash ROM
SDRAM
3003
USB
ロム
メモリ
PC
USB HUB
3003a
3003b
3021
3008
3000
3010
電源
3009
3013

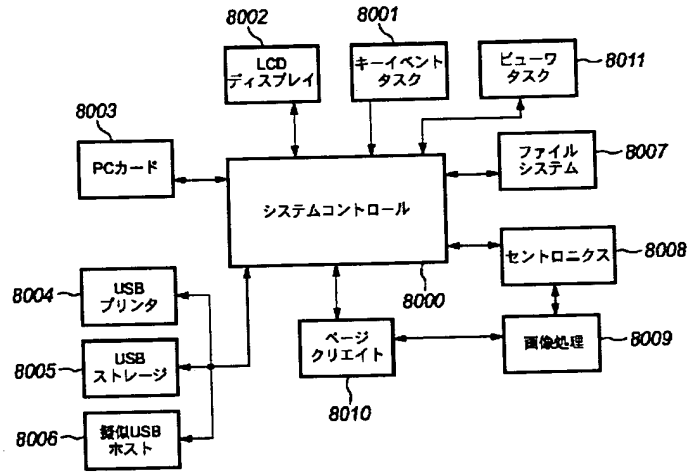
【図４】


3002
CPU コア
3100
3103
3101
3002a
外部メモリ コントローラ
キャッシュ コントローラ
IRAM

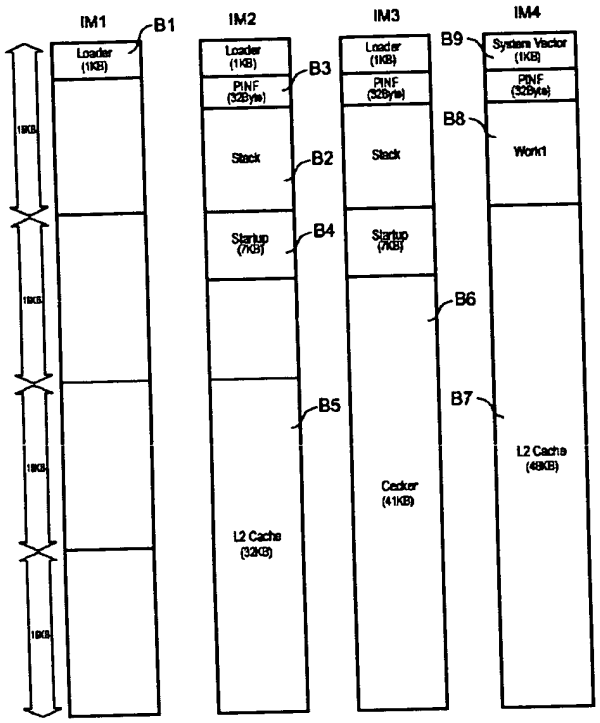
【図５】


4007a
4009
スイッチ I/F
各種 スイッチ
3002
4008
4005
1010
CPU
CPU I/F
操作パネル I/F
操作パネル
4011
エンジン リセット
3004
4007b
スイッチ I/F
プリンタ エンジン
4010
4002
1284 I/F
4001
3011
PCカード I/F
PCカード
4003
3010
USB I/F
PC
4004
3012
USB HOST I/F
カメラ
4008
1011
ビューワ I/F
ビューワ
3001

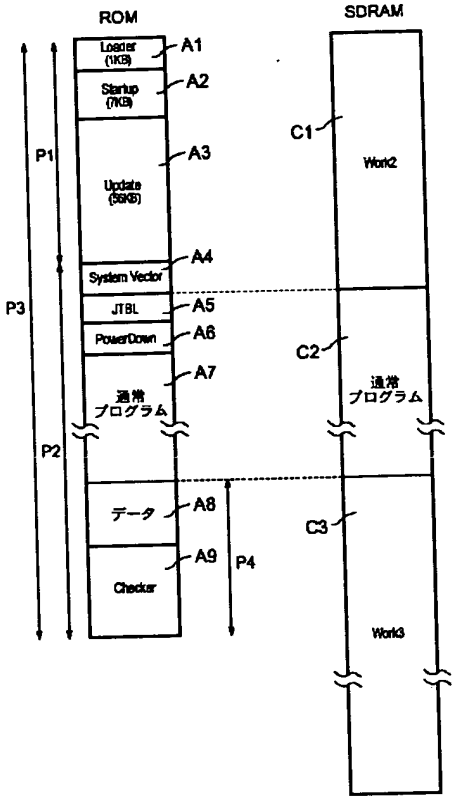
【図６】


8002
8001
LCD ディスプレイ
キーイベント タスク
ビューワ タスク
8011
8003
PCカード
システムコントロール
ファイル システム
8007
セントロニクス
8008
8004
USB プリンタ
8000
ページ クリエイト
画像処理
8009
8005
USB ストレージ
8010
8006
疑似USB ホスト

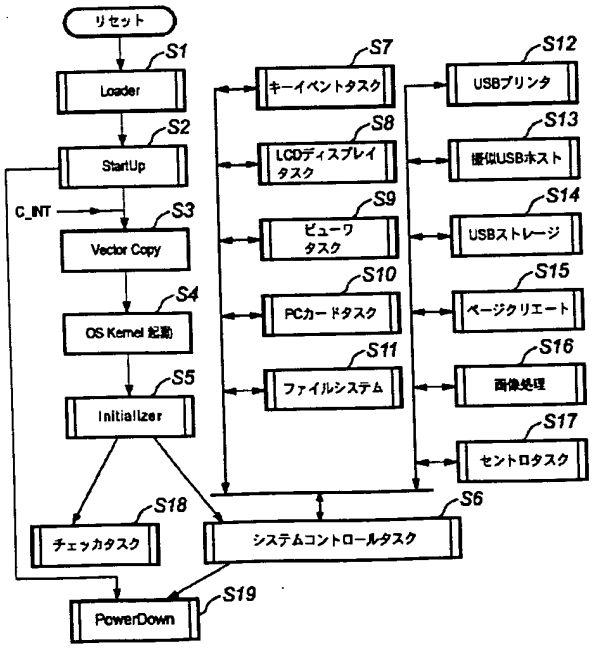
【図７】


IM1
IM2
IM3
IM4
B1
B2
B3
B4
B5
B6
B7
B8
B9
Loader (1KB)
PINF (32Byte)
Stack
Startup (7KB)
L2 Cache (32KB)
Cecker (41KB)
Work1
L2 Cache (48KB)
System Vector (1KB)
1MB
1MB
1MB
1MB

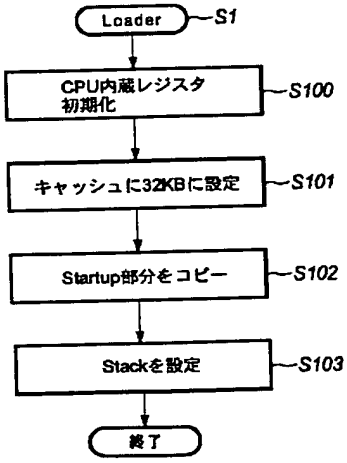
【図８】


ROM
SDRAM
A1
A2
A3
A4
A5
A6
A7
A8
A9
B1
C1
C2
C3
P1
P2
P3
P4
Loader (1KB)
Startup (7KB)
Update (50KB)
System Vector
JTBL
PowerDown
通常プログラム
データ
Checker
Work2
Work3

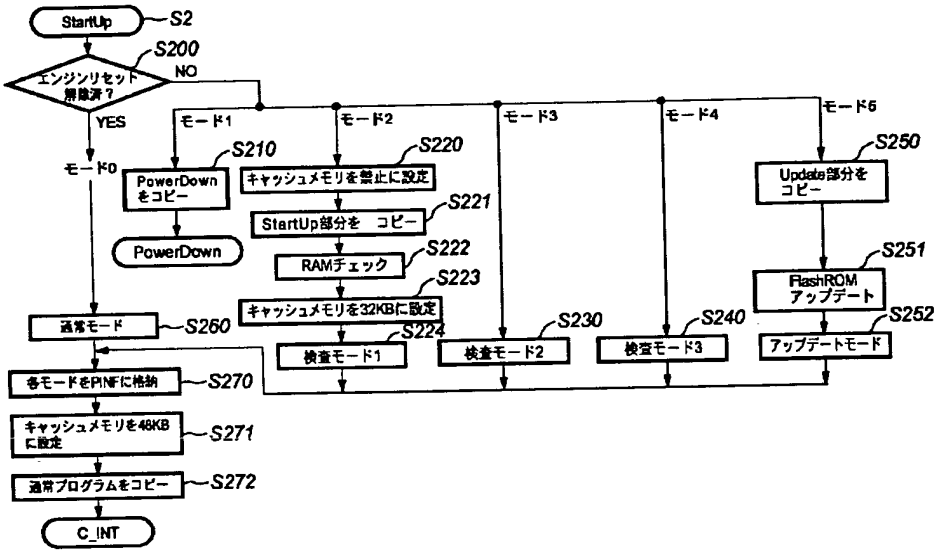
【図９】


リセット
S1
Loader
S2
StartUp
C_INT
S3
Vector Copy
S4
OS Kernel 起動
S5
Initializer
S6
システムコントロールタスク
S7
キーイベントタスク
S8
LCDディスプレイタスク
S9
ビューワタスク
S10
PCカードタスク
S11
ファイルシステム
S12
USBプリンタ
S13
擬似USBホスト
S14
USBストレージ
S15
ページクリエート
S16
画像処理
S17
セントロタスク
S18
チェッカタスク
S19
PowerDown

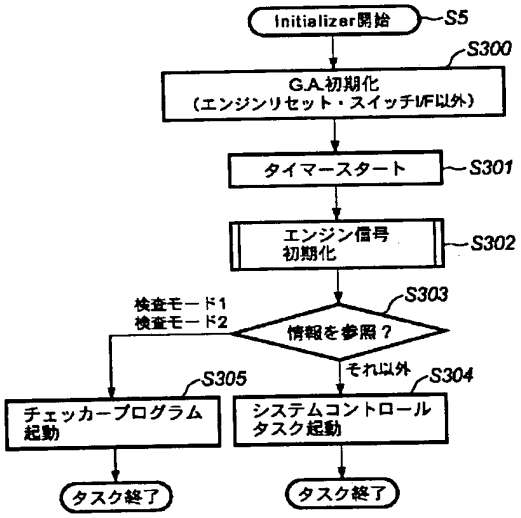
【図１０】


Loader
S1
CPU内蔵レジスタ初期化
S100
キャッシュに32KBに設定
S101
Startup部分をコピー
S102
Stackを設定
S103
終了

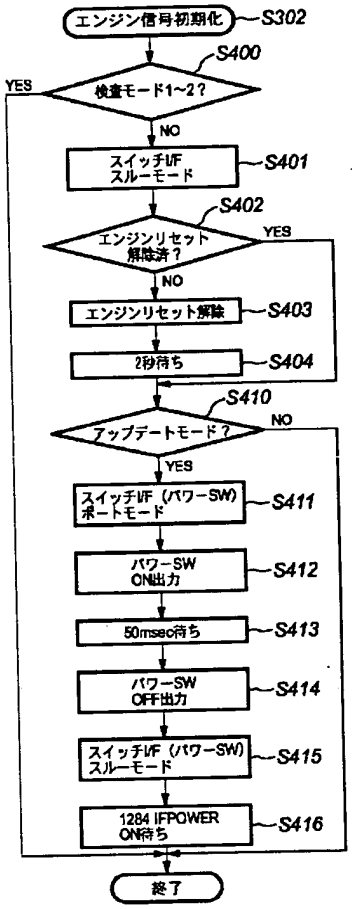
【図１１】



【図１２】



【図１３】



フロントページの続き

(72)発明者　桝本　和幸
東京都大田区下丸子３丁目30番２号　キヤノン株式会社内
(72)発明者　諏訪　徹哉
東京都大田区下丸子３丁目30番２号　キヤノン株式会社内
(72)発明者　濱本　昭彦
東京都大田区下丸子３丁目30番２号　キヤノン株式会社内
(72)発明者　日比　真
東京都大田区下丸子３丁目30番２号　キヤノン株式会社内
(72)発明者　大島　真人
東京都大田区下丸子３丁目30番２号　キヤノン株式会社内
(72)発明者　後藤　史博
東京都大田区下丸子３丁目30番２号　キヤノン株式会社内

(72)発明者　小野　光洋
東京都大田区下丸子３丁目30番２号　キヤノン株式会社内

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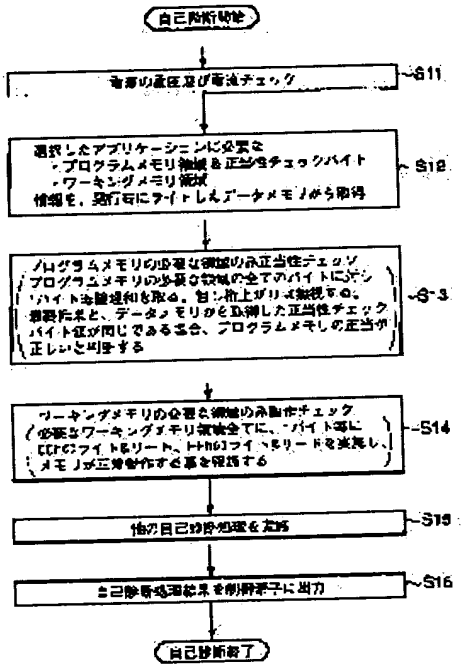
(71)Applicant : TOSHIBA CORP
(72)Inventor : UCHIDA HIROYASU

(54) PORTABLE ELECTRONIC DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a portable electronic device capable of shortening a self- diagnosis processing time even when memory capacity is increased.
SOLUTION: When an IC card is driven, validity check is performed respectively only to a region for storing a selected application program in a program memory shown by regional information and a region in a working memory corresponding to the selected application program, based on the regional information stored in a data memory.



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B42D 15/10	521	G06F 12/16	310	H	5B018
G06F 12/16	310		320	B	5B035
	320	G06K 19/00		N	

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(71)出願人　000003078
株式会社東芝
東京都港区芝浦一丁目１番１号
(72)発明者　内田　裕康
神奈川県川崎市幸区柳町70番地　株式会社東芝柳町事業所内
(74)代理人　100058479
弁理士　鈴江　武彦　（外６名）

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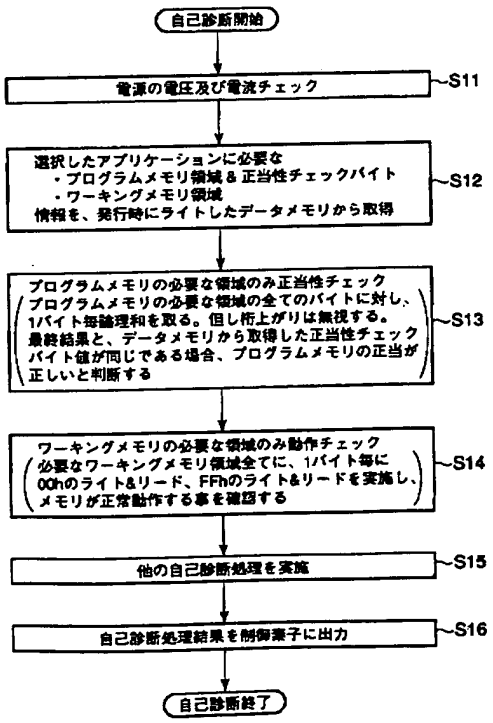
5B018 GA03 HA13 JA12 NA01 NA04
5B035 AA02 BB09 CA29 CA31

(54)【発明の名称】携帯可能電子装置

(57)【要約】
【課題】メモリ容量が大きくなっても、自己診断処理時間の短縮が可能となる携帯可能電子装置を提供する。
【解決手段】当該ＩＣカードが起動されると、データメモリに記憶されている領域情報に基づき、その領域情報で示されるプログラムメモリの選択されたアプリケーションプログラムが格納された領域、および、当該選択されたアプリケーションプログラムに対応するワーキングメモリの領域に対してのみそれぞれ正当性チェックを行なう。



1

【特許請求の範囲】

【請求項１】　複数の領域に分割され、かつ、これら複数の領域のうち少なくとも１つの領域が選択的に使用される第１のメモリと、少なくとも前記第１のメモリの各領域のうち選択された領域を示す領域情報を記憶している第２のメモリと、前記第１のメモリの選択された領域に対してアクセスを行なうための制御部とを有し、選択的に外部との間でデータの入出力を行なう携帯可能電子装置において、

当該携帯可能電子装置が起動されると、前記第２のメモリ内の領域情報に基づき、その領域情報で示される前記第１のメモリの選択された領域に対してのみ正当性チェックを行なう自己診断手段を具備したことを特徴とする携帯可能電子装置。

【請求項２】　前記第１のメモリは書換え不可能な不揮発性メモリおよび揮発性メモリの少なくともいずれか一方のメモリからなり、前記第２のメモリは書換え可能な不揮発性メモリからなることを特徴とする請求項１記載の携帯可能電子装置。

【請求項３】　少なくとも複数のアプリケーションプログラムが格納されたプログラムメモリと、このプログラムメモリに格納された複数のアプリケーションプログラムにそれぞれ対応し、そのアプリケーションプログラムの実行時に対応する領域が選択的に使用される複数の領域からなるワーキングメモリと、前記プログラムメモリに格納された複数のアプリケーションプログラムのうち選択されたアプリケーションプログラムが格納されている領域、および、当該選択されたアプリケーションプログラムに対応する前記ワーキングメモリの領域を示す各領域情報を記憶している記憶手段と、前記プログラムメモリに格納された複数のアプリケーションプログラムのうち選択されたアプリケーションプログラムを実行し、当該アプリケーションプログラムに対応する前記ワーキングメモリの領域を用いて所定の処理を行なう制御部とを有し、選択的に外部との間でデータの入出力を行なう携帯可能電子装置において、

当該携帯可能電子装置が起動されると、前記記憶手段内の領域情報に基づき、その領域情報で示される前記プログラムメモリの選択されたアプリケーションプログラムが格納された領域、および、当該選択されたアプリケーションプログラムに対応する前記ワーキングメモリの領域に対してのみそれぞれ正当性チェックを行なう自己診断手段を具備したことを特徴とする携帯可能電子装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、たとえば、データを記憶する書換え可能な不揮発性メモリを有し、このメモリに対してデータの読出しおよび書込みを行なって選択的に外部との間でデータの入出力を行なうＩＣカードなどの携帯可能電子装置に係り、特に複数のアプリケーションに対応した携帯可能電子装置に関する。

2

【０００２】

【従来の技術】最近、携帯可能電子装置として、書換え可能な不揮発性メモリ、および、これらを制御するＣＰＵ（セントラル・プロセッシング・ユニット）などの制御素子を有するＩＣチップを内蔵した、いわゆるＩＣカードが産業各方面で利用されている。

【０００３】一般に、この種のＩＣカードは、制御素子の制御プログラムや複数のアプリケーションプログラムを格納したプログラムメモリ、および、制御素子が処理を行なう際の処理データを一時的に保持するワーキングメモリを有しており、コマンドやレスポンスを用いて、外部装置（ＩＣカードリーダ・ライタ）との間でデータの入出力を行なうようになっている。

【０００４】

【発明が解決しようとする課題】最近のＩＣカードは、メモリの集積効率技術の向上と下記の理由から、メモリ容量の増大化が進んでいる。

（１）プログラムメモリ

・開発するＩＣカードのＩＣチップの品種を減らすため、１枚のＩＣカードに多数のアプリケーションプログラムを書込んでおき、必要なアプリケーションプログラムのみをカード発行時に選択する。そのため、大きなプログラムメモリ領域が必須。

・１つのアプリケーションプログラムに関しても複雑な制御が必要となり、プログラムメモリ領域が増大。

（２）ワーキングメモリ

・複雑な暗号化や計算が必要となり、ワーキングメモリ領域の増大が必須。

【０００５】以上のように、ＩＣカードのメモリ容量は増大する傾向にある。しかしながら、ＩＣカードは、通常、使用する前にプログラムメモリ内容の正当性、および、ワーキングメモリの動作チェックを、全メモリエリアに対し自己診断として行なうようになっている。そのため、メモリ領域が大きいと、自己診断処理時間が著しく増大し、以下の問題を抱えている。

・ＩＣカードの利用者は、自己診断処理による待ち時間が長くなる。

・ＩＣカードの初期化、発行作業時間の増加となり、製造行程の工数が多くなる。特に、ＩＣカードの初期化あるいは発行する枚数が１０万枚などになれば、その影響は極めて大きいものとなる。

そこで、本発明は、メモリ容量が大きくなっても、自己診断処理時間の短縮が可能となる携帯可能電子装置を提供することを目的とする。

【０００６】

【課題を解決するための手段】本発明の携帯可能電子装置は、複数の領域に分割され、かつ、これら複数の領域のうち少なくとも１つの領域が選択的に使用される第１のメモリと、少なくとも前記第１のメモリの各領域のう

ち選択された領域を示す領域情報を記憶している第２のメモリと、前記第１のメモリの選択された領域に対してアクセスを行なうための制御部とを有し、選択的に外部との間でデータの入出力を行なう携帯可能電子装置において、当該携帯可能電子装置が起動されると、前記第２のメモリ内の領域情報に基づき、その領域情報で示される前記第１のメモリの選択された領域に対してのみ正当性チェックを行なう自己診断手段を具備したことを特徴とする。

【０００７】

【発明の実施の形態】以下、本発明の実施の形態について図面を参照して説明する。図１は、本実施の形態に係る携帯可能電子装置としてのＩＣカードを取扱う端末装置の構成を概略的に示すものである。この端末装置は、ＩＣカード１をＩＣカードリーダ・ライタ２を介してＣＰＵなどからなる制御部３と接続可能にするとともに、制御部３にキーボード４、ＣＲＴ表示部５、プリンタ６を接続して構成される。

【０００８】ＩＣカード１は、たとえば、商品購入などの際にユーザが保持し、暗証番号によるユーザの照合や商品購入額によるサービスポイントの計算・データ蓄積などを行なうものであり、図２に示すように構成されている。すなわち、ＣＰＵなどの制御素子（制御部）１１、第１のメモリとしてのプログラムメモリ１２、第２のメモリ（記憶手段）としてのデータメモリ１３、第２のメモリ（記憶手段）としてのワーキングメモリ１４、および、ＩＣカードリーダ・ライタ２との電気的接触を得るためのコンタクト部１５によって構成されており、これらのうち制御素子１１、データメモリ１２、ワーキングメモリ１３、および、プログラムメモリ１４は１つのＩＣチップ（あるいは、複数のＩＣチップ）で構成されてＩＣカード本体内に埋設されている。

【０００９】プログラムメモリ１２は、制御素子１１の制御プログラムおよび複数のアプリケーションプログラムなどを記憶するものであり、たとえば、マスクＲＯＭなどのＩＣチップ製造時に最初に書込まれたら再度書換えることができない書換え不可能な不揮発性メモリで構成されている。

【００１０】データメモリ１３は、各種データの記憶に使用され、たとえば、ＥＥＰＲＯＭ（エレクトリカル・イレーザブル・プログラムＲＯＭ）やＦｅＲＡＭ（強誘電体ＲＡＭ）などの書換え可能な不揮発性メモリで構成されている。ワーキングメモリ１４は、制御素子１１が処理を行なう際の処理データなどを一時的に保持するためのメモリであり、たとえば、ＳＲＡＭ（スタティックＲＡＭ）などの書換え可能な揮発性メモリで構成されている。

【００１１】図３は、プログラムメモリ１２の構成を模式的に示すもので、ＯＳ（オペレーションシステム）プログラムが格納されるＯＳプログラム領域１２１、外部

装置と通信するためのＩ／Ｆ（インターフェース）プログラムが格納されるＩ／Ｆプログラム領域１２２、複数のアプリケーション、たとえば、第１、第２、第３のアプリケーションのプログラムが格納される第１のアプリケーションプログラム領域１２３、第２のアプリケーションプログラム領域１２４、第３のアプリケーションプログラム領域１２５、および、空き領域１２６から構成されている。

【００１２】このように、当該ＩＣカード１は、第１、第２、第３のアプリケーションの全てが使用できるように、プログラムメモリ１２内にそれらのプログラムが格納されているが、実際に使用するのは、たとえば、第２のアプリケーションのみの場合がある。そのような場合、第２のアプリケーションのプログラムが格納されている第２のアプリケーションプログラム領域１２４、および、全てのアプリケーションの動作に必要なＯＳプログラムが格納されているＯＳプログラム領域１２１、Ｉ／Ｆプログラムが格納されているＩ／Ｆプログラム領域１２２のみに対して正当性チェックを実施し、その他の領域（第１のアプリケーションプログラム領域１２３、第３のアプリケーションプログラム領域１２５、空き領域１２６）については、正当性チェックを実施しないようにすれば、プログラムメモリ１２の正当性チェック処理時間が大幅に短縮できることとなる。

【００１３】図４は、ワーキングメモリ１４の構成を模式的に示すもので、プログラムメモリ１２に格納された第１、第２、第３のアプリケーションプログラムにそれぞれ対応する複数（たとえば、３つ）の領域１４１，１４２，１４３、および、未使用領域１４４から構成されていて、使用する領域は各アプリケーションにより異なっている。この例では、たとえば、第１のアプリケーションプログラムは領域１４１、第２のアプリケーションプログラムは領域１４２、第３のアプリケーションプログラムは領域１４３をそれぞれ使用するようになっている。なお、領域１４２は、たとえば、領域１４１に所定の領域１４２ａを加えた領域となっており、また、領域１４３は、たとえば、領域１４２に所定の領域１４３ａを加えた領域となっている。

【００１４】前記プログラムメモリ１２の場合と同様に、第１、第２、第３のアプリケーションの全てが使用できるようになっているが、たとえば、第２のアプリケーションのみしか使用しない場合、第２のアプリケーションプログラムが使用する領域１４２のみ動作チェックを行なうことで、ワーキングメモリ１４の動作チェック処理時間が大幅に短縮できることとなる。

【００１５】次に、本実施の形態における自己診断処理について説明する。まず、プログラムメモリ１２の自己診断を行なうためのカード初期化時あるいは発行時における準備処理について説明する。ＩＣカード１の初期化時あるいは発行時に、たとえば、図５に示すように、デ

ータメモリ１３の先頭バイトに、今回発行した内容に合う必要なプログラムメモリ領域の数量ｎを、プログラムエリアチェック数量指定バイト１３１にセットする。たとえば、当該ＩＣカード１の運用時に使用するアプリケーションプログラムとして第２のアプリケーションプログラムのみが選択された場合、領域の数量ｎは「２」にセットされる。この場合、ＯＳプログラム領域１２１およびＩ／Ｆプログラム領域１２２を１つの領域としている。

【００１６】次に、プログラムエリアチェック数量指定バイト１３１にセットされた数量ｎが「２」の場合、２個のチェックする各領域のスタートアドレス（領域情報）１３２，１３４、および、ストップアドレス（領域情報）１３３，１３５をセットする。たとえば、図５において表記されたプログラム１スタートアドレス１３２、プログラム１ストップアドレス１３３には、ＯＳプログラム領域１２１およびＩ／Ｆプログラム領域１２２を１つの領域として、その先頭アドレス、最終アドレスが格納され、プログラム２スタートアドレス１３４、プログラム２ストップアドレス１３５には、上記例によれば第２のアプリケーションプログラム領域１２４の先頭アドレス、最終アドレスが格納される。次に、上記のように指定したプログラム領域の全てのバイトを順に、１バイトごとに論理和を取った値（ただし、桁上がりは無視）を、プログラムエリア正当性チェックバイト１３６としてセットする。

【００１７】次に、ワーキングメモリ１４の自己診断を行なうためのカード初期化時あるいは発行時における準備処理について説明する。上述したプログラムメモリ１２と同様に、ＩＣカード１の初期化時あるいは発行時に、図５に示すように、ワーキングエリアチェック数量指定バイト１３７に、今回発行した内容に必要なワーキングメモリ領域の数量ｎをセットする。次に、ワーキングエリアチェック数量指定バイト１３７にセットされた数量ｎが「１」の場合、１個のチェックする領域のスタートアドレス１３８およびストップアドレス１３９をセットする。たとえば、図５において表記されたワーキングメモリ１スタートアドレス１３８には、上記例によればワーキングメモリ１４の領域１４２の先頭アドレスが格納され、ワーキングメモリ１ストップアドレス１３９には、上記例によればワーキングメモリ１４の領域１４２の最終アドレスが格納される。

【００１８】次に、時間短縮を実現する自己診断処理について図６に示すフローチャートを参照して説明する。ＩＣカード１をＩＣカードリーダ・ライタ２へ挿入セットすると、ＩＣカードリーダ・ライタ２からＩＣカード１の制御素子１１へ電源、クロック信号、および、リセット信号などが供給される。そして、ＩＣカード１の制御素子１１がリセット信号のオンからオフへの変化点を検出すると（ステップＳ１）、リセット信号に対応した初期応答信号（Answer to Reset：ＡＴＲ）をＩＣカードリーダ・ライタ２へ出力する（ステップＳ２）。次に、制御素子１１は、ＩＣカードリーダ・ライタ２からコマンドを受信すると（ステップＳ３）、受信したコマンドの内容を解析して処理する（ステップＳ４）。

【００１９】また、ＩＣカード１の制御素子１１は、リセット信号のオンからオフへの変化点を検出すると（ステップＳ１）、ステップＳ２の処理と同時に、ＩＣカード１内の電源チェック、プログラムメモリ１２の正当性チェック、ワーキングメモリ１４の正当性チェックなどの自己診断処理を実施する（ステップＳ５）。そして、その自己診断処理結果を、ステップＳ２でのＡＴＲ出力後の最初のコマンド処理（ステップＳ３）の結果と併せてレスポンスとしてＩＣカードリーダ・ライタ２へ出力する（ステップＳ６）。なお、ステップＳ５の自己診断処理をステップＳ２の前に行ない、その自己診断処理結果をステップＳ２でＡＴＲとともにＩＣカードリーダ・ライタ２へ出力するようにしてもよい。

【００２０】次に、ステップＳ５における自己診断処理の詳細について図７に示すフローチャートを参照して説明する。まず、ＩＣカード１が正常に動作するのに必要な電源に関する電圧レベル、および、電流チェックを行なう（ステップＳ１１）。次に、プログラムメモリ１２およびワーキングメモリ１４の当該ＩＣカード１の運用時に使用するアプリケーションに関連する各領域のみをチェックするため、当該ＩＣカード１の初期化時あるいは発行時にデータメモリ１３内に書込まれたプログラムメモリ１２の領域情報１３２～１３５、および、プログラムエリア正当性チェックバイト１３６と、ワーキングメモリ１４の領域情報１３８，１３９をそれぞれ取得する（ステップＳ１２）。

【００２１】次に、取得した各領域情報に基づき、プログラムメモリ１２の選択されたアプリケーションに必要なアプリケーションプログラムが格納された領域、および、ＯＳプログラム領域１２１、Ｉ／Ｆプログラム領域１２２に対してのみ正当性チェックを行なうとともに（ステップＳ１３）、ワーキングメモリ１４の選択されたアプリケーションで用いる領域に対してのみ動作チェックを行なう（ステップＳ１４）。

【００２２】ステップＳ１３におけるプログラムメモリ１２の自己診断、すなわち、正当性を確認する方法は、具体的には以下のようにして行なわれる。プログラムメモリ１２の正当性チェックを行なう場合、データメモリ１３の先頭に配置されているプログラムエリアチェック数量指定バイト１３１を取得し、その数量ｎにしたがい、続いて配置されているスタートアドレス１３２、ストップアドレス１３３、および、ｎ＝２の場合、２個目のスタートアドレス１３４、ストップアドレス１３５の各情報をそれぞれ取得する。これにより、今回チェックを行なうプログラムメモリ１２の領域情報を得ることが

できる。

【００２３】次に、取得した各領域情報に基づき、プログラムメモリ１２の選択されたアプリケーションに必要なアプリケーションプログラムが格納された領域、この例では第２のアプリケーションプログラム領域１２４、および、ＯＳプログラム領域１２１、Ｉ／Ｆプログラム領域１２２に対して、順に１バイトごとに論理和を取り（桁上がりは無視）、データメモリ１３内のプログラムエリア正当性チェックバイト１３６の値と比較する。この比較の結果、両者が同一ならば、プログラムメモリ１２は初期化時あるいは発行時に対し変化がないものとみなし、正当性があると判断する。

【００２４】ステップＳ１４におけるワーキングメモリ１４の自己診断、すなわち、動作チェック方法は、具体的には以下のようにして行なわれる。ワーキングメモリ１４の動作チェックを行なう場合、データメモリ１３の先頭に配置されているワーキングエリアチェック数量指定バイト１３７を取得し、その数量ｎにしたがい、続いて配置されているスタートアドレス１３８、ストップアドレス１３９を取得する。これにより、今回チェックを行なうワーキングメモリ１４の領域情報を得ることができる。

【００２５】次に、取得した各領域情報に基づき、ワーキングメモリ１４の選択されたアプリケーションで用いる領域、この例では領域１４２のみに対し、たとえば、データ「００ｈｅｘ」の書込み／読出しを行なった後、データ「ＦＦｈｅｘ」の書込み／読出しを行なうことにより、メモリが正常に動作するかなどを確認する。

【００２６】次に、ステップＳ１３，Ｓ１４の自己診断が終了すると、それ以外のあらかじめ定められた他の部分（たとえば、演算部など）に対する自己診断を行なう（ステップＳ１５）。ステップＳ１５の自己診断が終了すると、それまで行なった自己診断の結果を制御素子１１へ出力し（ステップＳ１６）、自己診断処理を終了する。

【００２７】以上説明したように、上記実施の形態によれば、実際のカード運用時に選択されたアプリケーションに必要なプログラムメモリ領域、ワーキングメモリ領域のみに対して自己診断を行ない、実際のカード運用時に使用しない不要なメモリ領域に対しては自己診断を行なわないため、近年のメモリ容量の大きくなったＩＣカードに対しても、自己診断処理時間の短縮が可能となる。

【００２８】また、メモリサイズが大容量化すると、一般的に生産時の歩留まりが悪くなる。しかしながら、本実施の形態のように、実際のカード運用時に必要なアプリケーションのメモリ領域のみに対して自己診断することで、もし未使用のメモリ領域に不良（欠陥）が見られても、運用上において問題がないため、歩留まりの向上にもなる。

【００２９】

【発明の効果】以上詳述したように本発明によれば、メモリ容量が大きくなっても、自己診断処理時間の短縮が可能となる携帯可能電子装置を提供できる。

【図面の簡単な説明】

【図１】本発明の実施の形態に係るＩＣカードを取扱う端末装置の構成例を示すブロック図。

【図２】ＩＣカードの構成を概略的に示すブロック図。

【図３】プログラムメモリの構成を模式的に示す構成図。

【図４】ワーキングメモリの構成を模式的に示す構成図。

【図５】データメモリに対するチェックするメモリ領域の領域情報の格納方法を説明するための図。

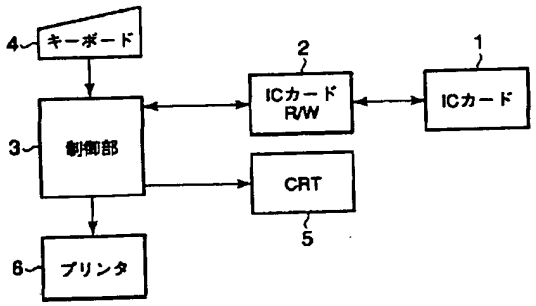
【図６】自己診断処理について説明するフローチャート。

【図７】図６における自己診断処理の詳細を説明するフローチャート。

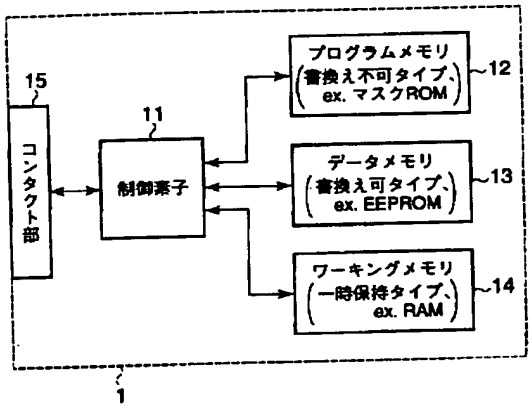
【符号の説明】

１…ＩＣカード（携帯可能電子装置）、２…ＩＣカードリーダ・ライタ、３…制御部、４…キーボード、５…ディスプレイ装置、６…プリンタ、１１…制御素子（制御部）、１２…プログラムメモリ（第１のメモリ）、１３…データメモリ（第２のメモリ、記憶手段）、１４…ワーキングメモリ、１５…コンタクト部、１２１…ＯＳプログラム領域、１２２…Ｉ／Ｆプログラム領域、１２３…第１のアプリケーションプログラム領域、１２４…第２のアプリケーションプログラム領域、１２５…第３のアプリケーションプログラム領域、１２６…空き領域、１４１，１４２，１４３…領域、１４４…未使用領域。

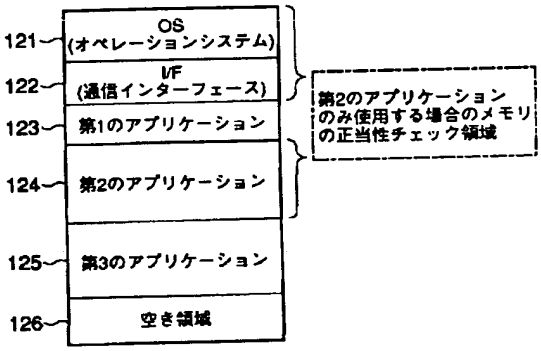
【図１】



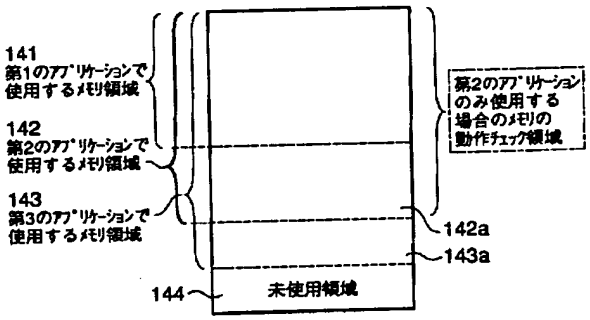
【図２】



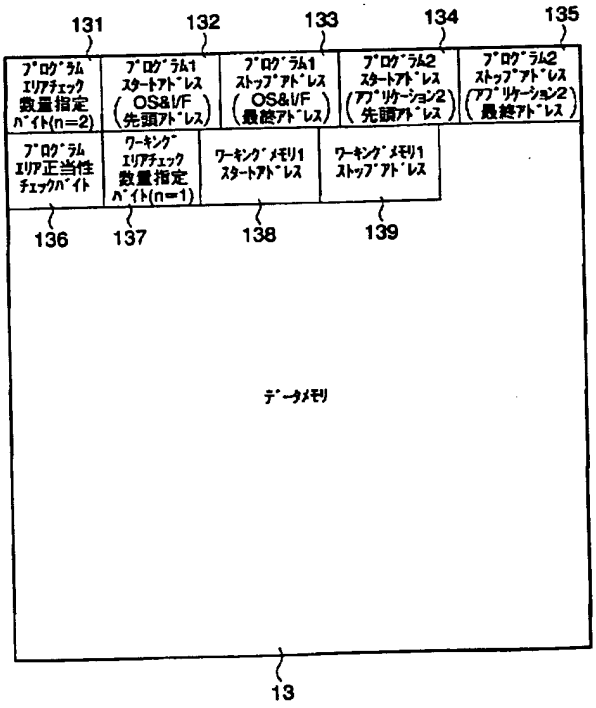
【図３】



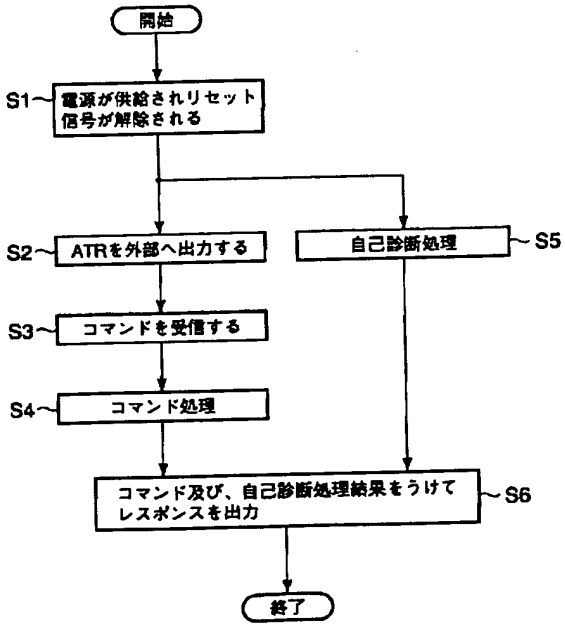
【図４】



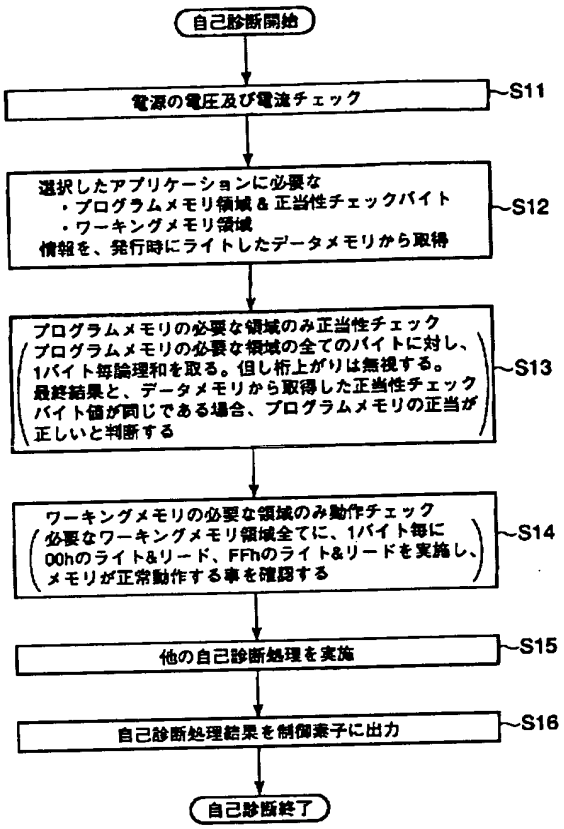
【図５】



【図６】



【図７】


自己診断開始
電源の電圧及び電流チェック
S11
選択したアプリケーションに必要な
・プログラムメモリ領域＆正当性チェックバイト
・ワーキングメモリ領域
情報を、発行時にライトしたデータメモリから取得
S12
プログラムメモリの必要な領域のみ正当性チェック
プログラムメモリの必要な領域の全てのバイトに対し、
1バイト毎論理和を取る。但し桁上がりは無視する。
最終結果と、データメモリから取得した正当性チェック
バイト値が同じである場合、プログラムメモリの正当が
正しいと判断する
S13
ワーキングメモリの必要な領域のみ動作チェック
必要なワーキングメモリ領域全てに、1バイト毎に
00hのライト&リード、FFhのライト&リードを実施し、
メモリが正常動作する事を確認する
S14
他の自己診断処理を実施
S15
自己診断処理結果を制御素子に出力
S16
自己診断終了

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FOR: INFORMATION PROCESS DEVICE

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Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Masayasu Mori
Registration No. 47,301

C. Irvin McClelland
Registration Number 21,124

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 11/04)

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願人 Applicant(s):	アルゼ株式会社

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【発明者】
　【住所又は居所】　東京都江東区有明３丁目１番地２５
　【氏名】　▲はい▼島　淳
【特許出願人】
　【識別番号】　598098526
　【氏名又は名称】　アルゼ株式会社
【代理人】
　【識別番号】　100098431
　【弁理士】
　【氏名又は名称】　山中　郁生
　【電話番号】　052-218-7161
【選任した代理人】
　【識別番号】　100097009
　【弁理士】
　【氏名又は名称】　富澤　孝
【選任した代理人】
　【識別番号】　100105751
　【弁理士】
　【氏名又は名称】　岡戸　昭佳
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【書類名】特許請求の範囲
【請求項１】
起動時に実行されるブートプログラムが記憶された第１記憶手段と、前記第１記憶手段が実装されたマザーボードと、前記マザーボードに接続されるとともにアプリケーションプログラムが記憶された第２記憶手段と、前記第２記憶手段の障害を点検する障害点検プログラムを実行する制御手段と、を有する情報処理装置において、
前記障害点検プログラムを前記第１記憶手段に記憶したことによって、前記制御手段が前記障害点検プログラムを起動時に実行すること、を特徴とする情報処理装置。
【請求項２】
請求項１に記載する情報処理装置であって、
業務用ゲーム装置として使用されること、を特徴とする情報処理装置。

【書類名】明細書
【発明の名称】情報処理装置
【技術分野】
【０００１】
本発明は、ハードウエアやソフトウエアの障害を点検する情報処理装置に関するものである。
【背景技術】
【０００２】
従来の情報処理装置においては、演算や制御に必要なプログラムやデータをハードディスクなどの記憶装置の一領域に記憶するとともに、それらのプログラムやデータの破損・変更・改竄などの障害の点検を行うプログラム（以下、「障害点検プログラム」という。）も当該記憶装置の別領域に記憶していた（例えば、特許文献１参照）。
【特許文献１】特開２００３－３３１２３６号公報（第３－４頁、第２図）
【発明の開示】
【発明が解決しようとする課題】
【０００３】
従って、当該記憶装置に破損などが発生した場合には、障害点検プログラムまでも破損していることがあり、このようなときには、障害点検プログラムの正当性を保証できなかった。
【０００４】
そこで、本発明は、上述した点を鑑みてなされたものであり、障害点検プログラムの点検対象である記憶装置に障害が発生しても、障害点検プログラムの正当性を保証できる情報処理装置を提供することを課題とする。
【課題を解決するための手段】
【０００５】
この課題を解決するために成された請求項１に係る発明は、起動時に実行されるブートプログラムが記憶された第１記憶手段（例えば、ＲＯＭ１３）と、前記第１記憶手段（例えば、ＲＯＭ１３）が実装されたマザーボード（例えば、マザーボード１１）と、前記マザーボード（例えば、マザーボード１１）に接続されるとともにアプリケーションプログラムが記憶された第２記憶手段（例えば、ハードディスク２４）と、前記第２記憶手段（例えば、ハードディスク２４）の障害を点検する障害点検プログラムを実行する制御手段（例えば、ＣＰＵ１２）と、を有する情報処理装置（例えば、情報処理装置１）において、前記障害点検プログラムを前記第１記憶手段（例えば、ＲＯＭ１３）に記憶したことによって、前記制御手段（例えば、ＣＰＵ１２）が前記障害点検プログラムを起動時に実行すること、を特徴としている。
【０００６】
尚、「第２記憶手段（例えば、ハードディスク２４）の障害を点検する」では、第２記憶手段（例えば、ハードディスク２４）というハードウエアの破損などの障害を点検したり、第２記憶手段（例えば、ハードディスク２４）に記憶されたソフトウエアの変更・改竄などの障害を点検したりする。
【０００７】
また、請求項２に係る発明は、請求項１に記載する情報処理装置（例えば、情報処理装置１）であって、業務用ゲーム装置として使用されること、を特徴としている。
【発明の効果】
【０００８】
すなわち、本発明の情報処理装置では、第２記憶手段とは別個のマザーボード上の第１記憶手段に障害点検プログラムが記憶されていることから、障害点検プログラムの点検対象である第２記憶手段に障害が発生しても、障害点検プログラムの正当性を保証できる。
【０００９】
特に、本発明の情報処理装置が業務用ゲーム装置として使用される場合には、障害点検

プログラムが起動時に実行されることによって、第２記憶手段の障害に対する点検を業務開始前に実行するので、遊技者に不快感を与えることなく、業務中のトラブルを事前に防止する対策を行うことができる。

【発明を実施するための最良の形態】

【００１０】

以下、本発明の実施の形態を図面を参照にして説明する。

図１は、本実施の形態に係る情報処理装置のブロック図である。図３は、本実施の形態に係る情報処理装置の斜視図である。図３に示すように、本実施の形態に係る情報処理装置１は、業務用ゲーム装置であるが、そのＯＳ（オペレーティング・システム）として市販のパーソナルコンピュータに搭載されるものを使用しており、その動作環境の下で、後述するハードディスクに記憶されたゲームソフトを動作させている。

【００１１】

また、図１に示すように、本実施の形態に係る情報処理装置１では、マザーボード１１上において、ＣＰＵ１２や、ＲＯＭ１３、ＲＡＭ１４、バス１５、コネクタ１６，１７、ポート１８、拡張スロット１９，２０などが配設されている。

【００１２】

この点、ＣＰＵ１２は、本実施の形態に係る情報処理装置１を制御するものであって、各種のプログラムを実行するものである。従って、ＣＰＵ１２は、「制御手段」に相当するものである。

【００１３】

また、ＲＯＭ１３は、本実施の形態に係る情報処理装置１を起動する際に必要な各種の制御プログラムなどが格納されている不揮発性メモリであり、「第１記憶手段」に相当するものである。そして、ＲＯＭ１３においては、図１に示すように、ブートプログラムが記憶されているブートプログラム記憶領域１３ａや、障害点検プログラムが記憶されている障害点検プログラム記憶領域１３ｂ、開始プログラムが記憶されている開始プログラム記憶領域１３ｃなどが形成されている。

尚、ＲＯＭ１３の各記憶領域１３ａ，１３ｂ，１３ｃに記憶されているブートプログラム、障害点検プログラム、開始プログラムについては、後述する。

【００１４】

また、ＲＡＭ１４は、ＣＰＵ１２でプログラムを実行した際に演算される各種データを一時的に記憶しておくメモリである。

【００１５】

また、バス１５は、周波数変換のブリッジ回路が設けられたＰＣＩバスであって、ＣＰＵ１２や、ＲＯＭ１３、ＲＡＭ１４、コネクタ１６，１７、ポート１８、拡張スロット１９，２０などとの間の信号のやりとりを行うための共通信号路である。

【００１６】

また、コネクタ１６は、ゲームソフトを動作させる際に必要な出力装置２１を接続する機器である。

ここでは、コネクタ１６に接続される出力装置２１は、液晶ディスプレイ（図３の符号２１参照）と、スピーカなどの音声出力装置（不図示）である。尚、液晶ディスプレイ（図３の符号２１参照）に代わって、ＣＲＴディスプレイなどを使用してもよい。

【００１７】

また、コネクタ１７は、ゲームソフトを動作させる際に必要な入力装置２２を接続する機器である。ここでは、コネクタ１７に接続される入力装置２２は、複数のボタンスイッチ（不図示）などを備えた操作テーブル２２（図３参照）である。尚、入力装置２２には、その他として、キーボードや、マウスなどがあるが、ゲームソフトの内容によっては、ジョイスティックなどをコネクタ１７に接続することもある。また、図１では、コネクタ１７は１個しか記載されていないが、入力装置２２が複数個であるときは、それぞれ専用のコネクタ１７が設けられる。

【００１８】

また、ポート１８には、フラットケーブル２３を介してハードディスク２４（ＨＤＤ）が接続されている。

【００１９】

そして、ポート１８に接続されたハードディスク２４においては、ＯＳ（オペレーティング・システム）が記憶されているＯＳ記憶領域２４ａや、拡張ＢＩＯＳ（ベーシック・インプット・アウトプット・システム）が記憶されている拡張ＢＩＯＳ記憶領域２４ｂ、ゲームソフトであるアプリケーションプログラムが記憶されているアプリケーション記憶領域２４ｃなどが形成されている。従って、ハードディスク２４は、「第２記憶手段」に相当するものである。

【００２０】

また、拡張スロット１９は、ビデオボード２５を接続するための挿入口である。

尚、拡張スロット１９を介して接続されたビデオボード２５は、出力装置２１の一つである液晶ディスプレイ（図３の符号２１参照）に絵や文字を表示するためのグラフィックス・アクセラレータを内蔵したボードであって、本実施の形態に係る情報処理装置１におけるゲームソフトの動作に耐え得るレベルの解像度や描画速度のパフォーマンスをもつものである。

【００２１】

また、拡張スロット２０は、サウンドボード２６を接続するための挿入口である。

尚、拡張スロット２０を介して接続されたサウンドボード２６は、出力装置２１の一つであるスピーカ（不図示）から出力されるＦＭ音源やＰＣＭ音源などのチップが載ったものであり、本実施の形態に係る情報処理装置１におけるゲームソフトの動作に耐え得るレベルのパフォーマンスをもつものである。

【００２２】

続いて、本実施の形態に係る情報処理装置１を起動する際の動作について、図２のフローチャートに基づいて説明する。図２は、本実施の形態に係る情報処理装置を起動する際に実行される開始プログラムのフローチャートを示した図である。

【００２３】

本実施の形態に係る情報処理装置１では、起動されると、ＲＯＭ１３の開始プログラム記憶領域１３ｃに記憶された開始プログラムがＣＰＵ１２によって実行される。

【００２４】

すなわち、図２に示すように、開始プログラムが実行されると、先ず、Ｓ１１において、ブートプログラムが実行される。

この点、ブートプログラムとは、ＲＯＭ１３のブートプログラム記憶領域１３ａに記憶されているものであり、ハードディスク２４内にある拡張ＢＩＯＳ（ベーシック・インプット・アウトプット・システム）を含めた各種デバイスの初期化や、ハードディスク２４内にあるＯＳ（オペレーティング・システム）の初期化が行われる。

【００２５】

このとき、ハードディスク２４内にあるＯＳ（オペレーティング・システム）はＲＡＭ１４にロードされ起動されることから、この観点からすれば、ＲＯＭ１３はブートＲＯＭと言える。

【００２６】

次に、開始プログラムでは、Ｓ１２に進むと、障害点検プログラムが実行される。

この点、障害点検プログラムとは、ＲＯＭ１３の障害点検プログラム記憶領域１３ａに記憶され、ハードディスク２４の障害に対する点検を行うものであり、ハードディスク２４自身の破損などの障害を点検したり、ハードディスク２４に記憶されたプログラムの変更・改竄などの障害を点検したりする。

【００２７】

次に、開始プログラムでは、Ｓ１３に進むと、ハードディスク２４の障害があるか否かを判断する。この判断は、上述したＳ１２の障害点検プログラムの実行結果に基づいて行われる。

【００２８】
このとき、ハードディスク２４の障害がないと判断する場合には（Ｓ１３：ＮＯ）、Ｓ１４に進んで、ハードディスク２４内にあるアプリケーションプログラムをＲＡＭ１４にロードして、アプリケーションプログラムの実行を開始する。一方、ハードディスク２４の障害があると判断する場合には（Ｓ１３：ＹＥＳ）、Ｓ１５に進んで、出力装置２１の一つである液晶ディスプレイ（図３の符号２１参照）にエラー表示をする。

【００２９】
以上詳細に説明したように、本実施の形態に係る情報処理装置１では、図１に示すように、ハードディスク２４とは別個のマザーボード１１上のＲＯＭ１１の障害点検プログラム記憶領域１３ａに障害点検プログラムが記憶されていることから、障害点検プログラムの点検対象であるハードディスク２４に障害が発生しても、障害点検プログラムの正当性を保証できる。

【００３０】
また、本実施の形態に係る情報処理装置１は、図３に示すように、業務用ゲーム装置として使用されており、さらに、図２に示すように、ＲＯＭ１３に記憶された障害点検プログラムは起動時に実行され、ハードディスク２４の障害に対する点検を業務開始前に実行する。従って、業務用ゲーム装置の遊技者に不快感を与えることなく、業務中のトラブルを事前に防止する対策を行うことができる。

【００３１】
尚、本発明は上記実施の形態に限定されるものでなく、その趣旨を逸脱しない範囲で様々な変更が可能である。

例えば、本実施の形態に係る情報処理装置１は、図３に示すように、業務用ゲーム装置として使用されているものであるが、この点、市販のパーソナルコンピュータであってもよく、この場合には、入力装置２２には、操作テーブル２２に代わって、キーボードや、マウス、ジョイスティックなどが使用され得る。

【００３２】
また、本実施の形態に係る情報処理装置１では、「第２記憶手段」としてハードディスク２４を使用しているが、この点、電気的に内容を変更できるフラッシュ・メモリなどを使用してもよく、この場合には、障害点検プログラムは、フラッシュ・メモリなどの障害に対する点検を行うことなる。

【産業上の利用可能性】

【００３３】
本発明は、情報処理装置における障害の点検に適用し得る。

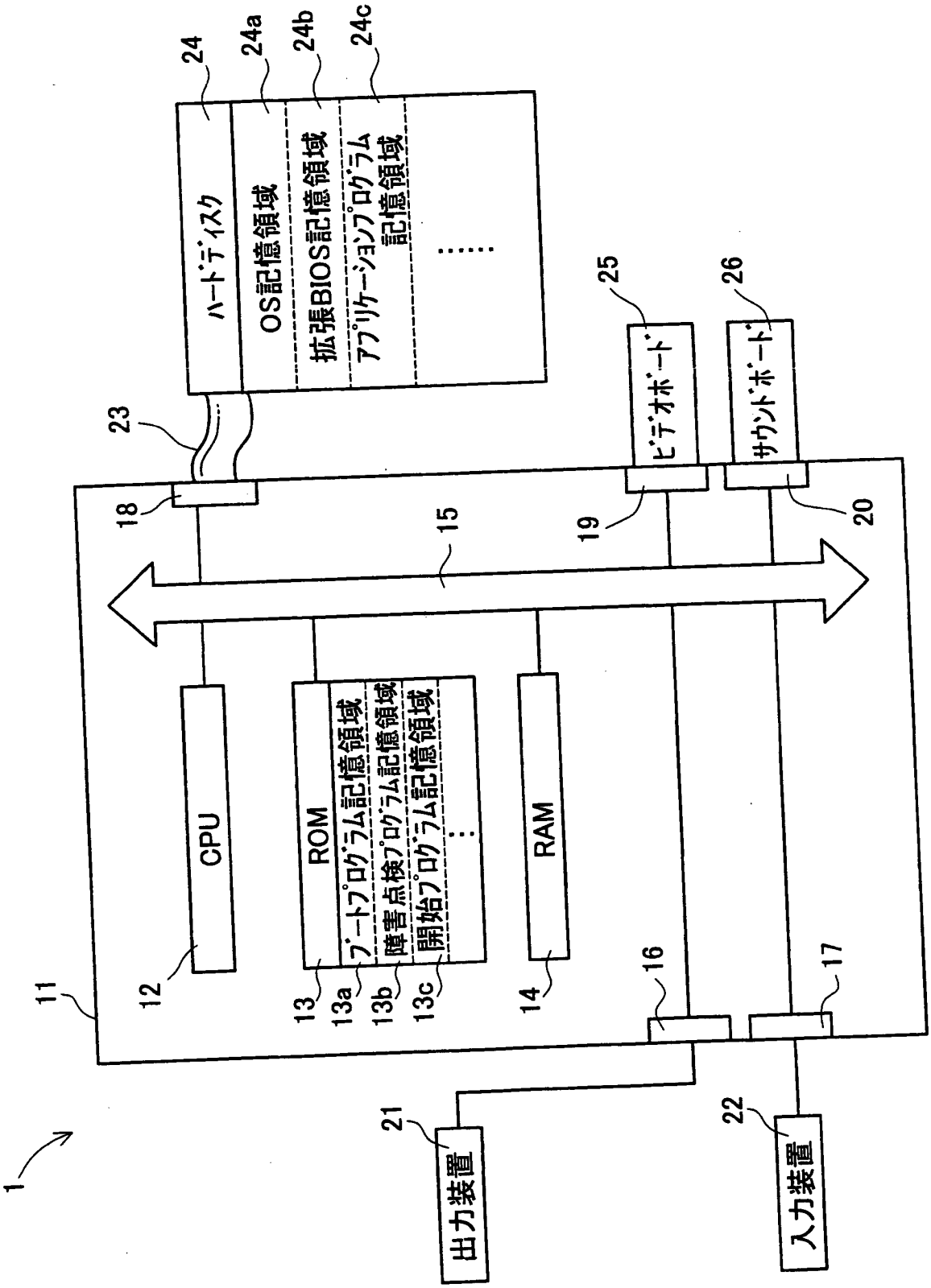
【図面の簡単な説明】

【００３４】
【図１】本実施の形態に係る情報処理装置のブロック図である。
【図２】本実施の形態に係る情報処理装置を起動する際に実行される開始プログラムのフローチャートを示した図である。
【図３】本実施の形態に係る情報処理装置の斜視図である。

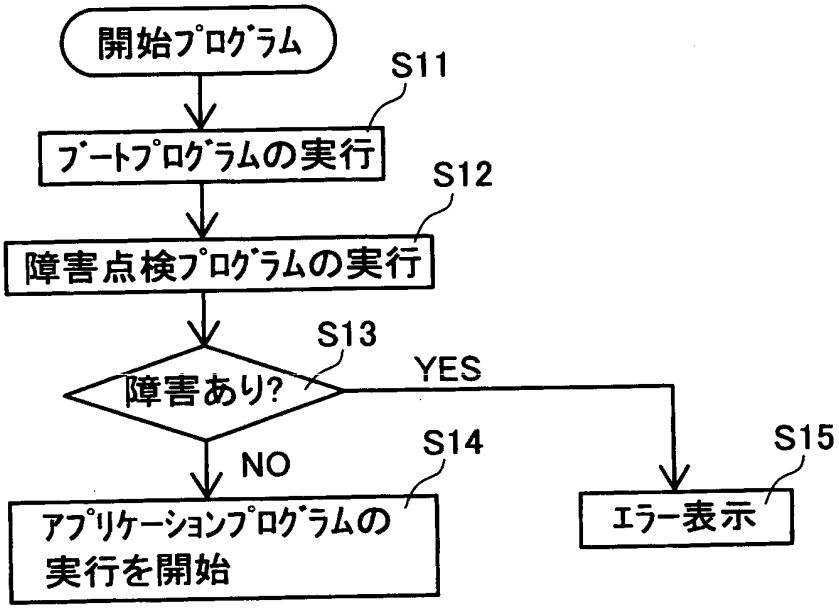
【符号の説明】

【００３５】
１　情報処理装置
１１　マザーボード
１２　ＣＰＵ
１３　ＲＯＭ
２４　ハードディスク

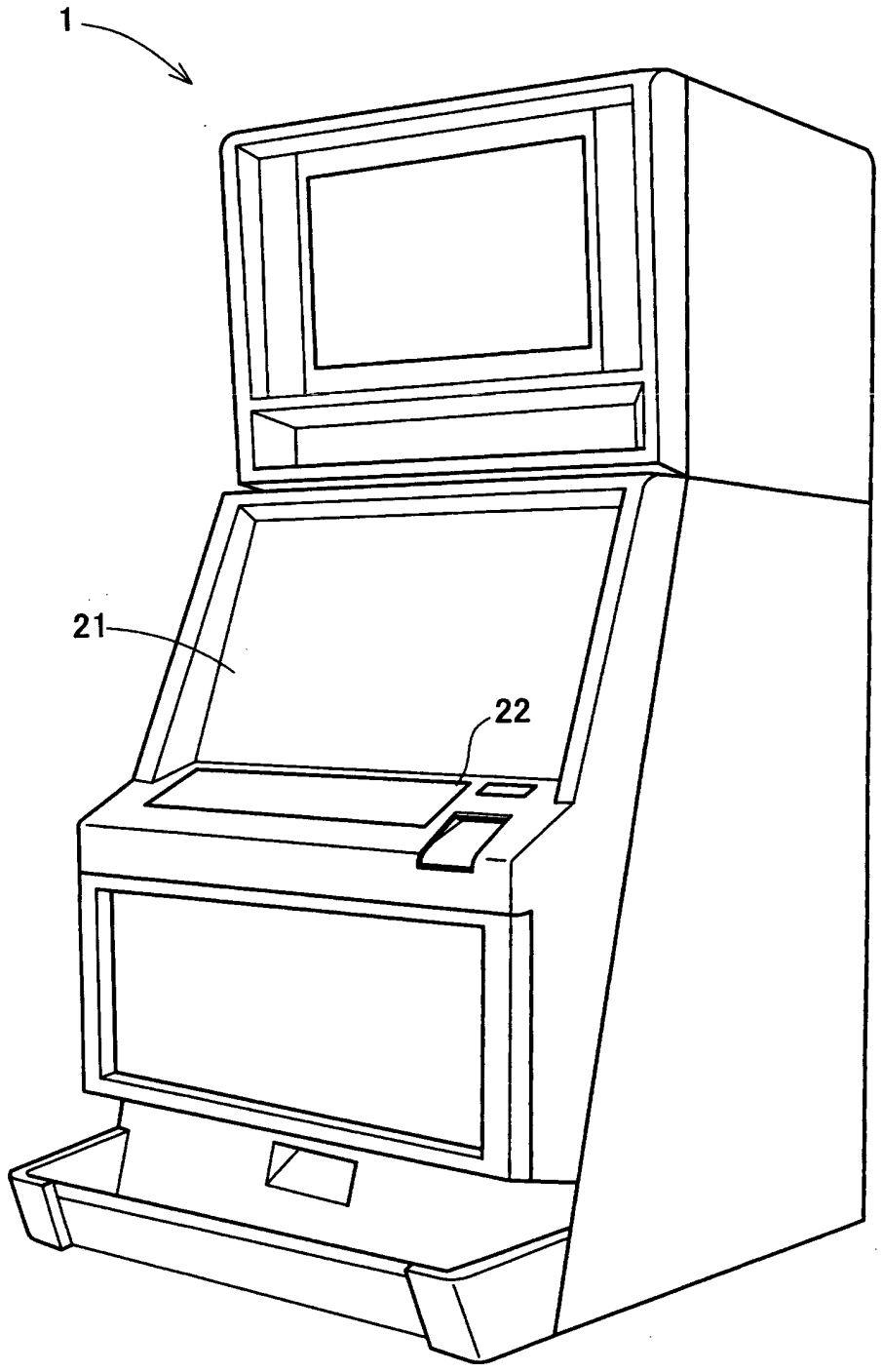
【書類名】図面
【図１】



【図２】



【図３】



【書類名】要約書
【要約】
【課題】　障害点検プログラムの点検対象である記憶装置に障害が発生しても、障害点検プログラムの正当性を保証できる情報処理装置を提供すること。
【解決手段】　情報処理装置１では、ハードディスク２４とは別個のマザーボード１１上のＲＯＭ１１の障害点検プログラム記憶領域１３ａに障害点検プログラムが記憶されていることから、障害点検プログラムの点検対象であるハードディスク２４に障害が発生しても、障害点検プログラムの正当性を保証できる。
【選択図】　図１

特願２００４－２４５３３７

出　願　人　履　歴　情　報

識別番号　［５９８０９８５２６］

１．変更年月日　１９９８年　７月２３日
［変更理由］　新規登録
住　所　東京都江東区有明３丁目１番地２５
氏　名　アルゼ株式会社

Docket No. 276900US8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jun HAISHIMA

SERIAL NO: 11/205,121 GAU: 2113

FILED: August 17, 2005 EXAMINER:

FOR: INFORMATION PROCESS DEVICE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:
Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the reference(s) cited in the attached Extended European Search Report and listed on the attached form PTO-1449. Copies of the listed reference(s) are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language reference(s).

☐ Online credit card payment is being made in the amount required under 37 CFR §1.17(p).

RELATED CASES

☐ Attached is a list of applicant's pending application(s), published application(s) or issued patent(s) which may be related to the present application. In accordance with the waiver of 37 CFR 1.98 dated September 21, 2004, copies of the cited pending applications are not provided. Cited published and/or issued patents, if any, are listed on the attached PTO form 1449.

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CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

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Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Bradley D. Lytle
Registration No. 40,073

Paul J. Killos
Registration No. 58,014

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 05/03)

Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO.	SERIAL NO.
		276900US8	11/205,121
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Jun HAISHIMA	
		FILING DATE	GROUP
		August 17, 2005	2113

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	US 6,449,735 B1	9/10/2002	David A. EDWARDS, et al.			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO	JP 9-319445	12/12/1997	Japan (with English Abstract)		x
	AP	JP 2000-35888	2/2/2000	Japan (with English Abstract)		x
	AQ	EP 0 774 716 A1	5/21/1997	Europe		
	AR	EP 0 801 387 A2	10/15/1997	Europe		
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	
	AX	
	AY	
	AZ	☐ Additional References sheet(s) attached

Examiner	Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EP 3614 A1

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EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 09319445
PUBLICATION DATE : 12-12-97

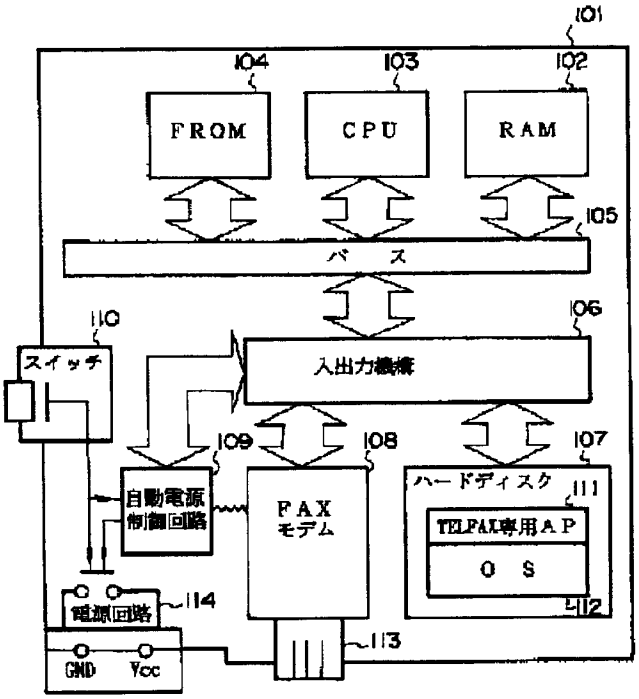
APPLICATION DATE : 27-05-96
APPLICATION NUMBER : 08132214

APPLICANT : NEC SHIZUOKA LTD;

INVENTOR : SUGIURA ETSUSHI;

INT.CL. : G06F 1/00 G06F 1/26 G06F 9/06
G06F 13/00 H04M 1/65 H04N 1/32

TITLE : INFORMATION PROCESSOR WITH AUTOMATIC RECORDING FUNCTION



ABSTRACT : PROBLEM TO BE SOLVED: To provide an information processor with an automatic recording function which can receive a telephone or a facsimile coming at random even without setting an operating state at all times.

SOLUTION: This information processor has an automatic power source control circuit 109 provided with a means for turning on/off a power source in response to a prescribed activation factor and a means for outputting the activation factor information of power source ON, hard disk 107 for storing an OS and an AP for performing automatic TEL recording and automatic FAX reception, and FROM 104 for storing a BOOT program containing a routine for starting the OS and the routine of high-speed diagnosis/initialization processing for diagnosing/initializing a hardware environment required for executing the AP. When the power source is turned on, a CPU 103 starts the BOOT program. When the activation factor shown by the activation factor information is the arrival of a ringer, the AP is executed after the routine of high-speed diagnosis/initialization processing, and the command for power source turning-off is sent to the automatic power source control circuit 109.

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平9－319445

(43)公開日　平成９年(1997)12月12日

(51)Int.Cl.[6]		識別記号	庁内整理番号	ＦＩ			技術表示箇所
Ｇ０６Ｆ	1/00	３７０		Ｇ０６Ｆ	1/00	３７０Ｂ	
	1/26				9/06	４１０Ｂ	
	9/06	４１０			13/00	３５４Ｚ	
	13/00	３５４		Ｈ０４Ｍ	1/65	Ｄ	
Ｈ０４Ｍ	1/65			Ｈ０４Ｎ	1/32	Ｚ	

審査請求　有　請求項の数４　ＯＬ　（全９頁）　最終頁に続く

(21)出願番号　特願平8－132214

(22)出願日　平成８年(1996)５月27日

(71)出願人　00019/366
静岡日本電気株式会社
静岡県掛川市下俣４番２号

(72)発明者　杉浦　悦志
静岡県掛川市下俣４番２号　静岡日本電気株式会社内

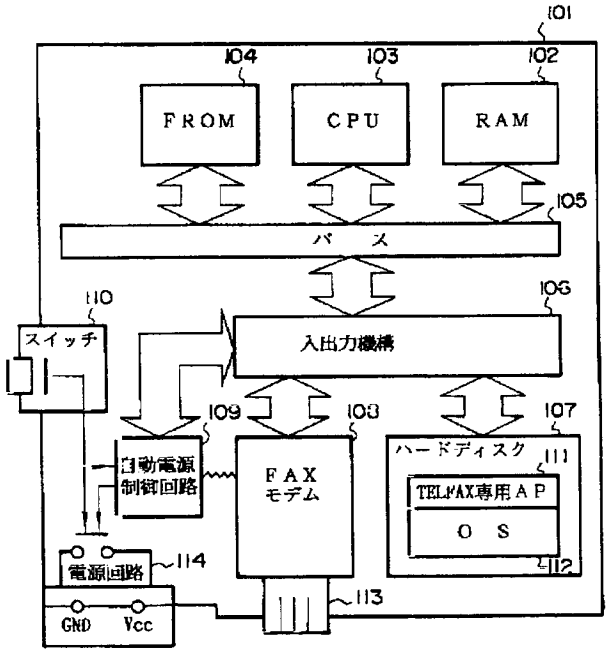
(74)代理人　弁理士　志賀　正武

(54)【発明の名称】　留守録機能付き情報処理装置

(57)【要約】

【課題】　常時稼働状態としなくても不定期に到来する電話やファクシミリの受信を行うことができる留守録機能付き情報処理装置を提供する。

【解決手段】　所定の起動要因に応答し電源の投入・切断をする手段および電源投入の起動要因情報を出力する手段を含む自動電源制御回路１０９と、ＯＳおよびＴＥＬ留守録，ＦＡＸ自動受信を行うＡＰを記憶するハードディスク１０７と、ＯＳを起動するルーチンおよびＡＰの実行に必要なハードウェア環境の診断・初期化のための高速・診断初期化処理のルーチンを含むＢＯＯＴプログラムを記憶するＦＲＯＭ１０４とを有する。ＣＰＵ１０３は、電源投入によりＢＯＯＴプログラムを起動し、起動要因情報が示す起動要因がリング到来の場合には、高速・診断初期化処理のルーチンを実行後、ＡＰを実行し、自動電源制御回路に電源切断の指令を送る。



【特許請求の範囲】
【請求項１】　所定の起動要因に応答して電源を投入または切断する手段および電源投入の起動要因を判別し、該判別結果を示す起動要因情報を出力する手段を備えた自動電源制御回路と、
ａ．オペレーティングシステム、
ｂ．電話の留守録処理およびファクシミリの自動受信処理を行うアプリケーションプログラム、および
ｃ．前記オペレーティングシステムを起動するためのルーチン並びに少なくとも前記アプリケーションプログラムの実行に必要とされるハードウェア環境の診断および初期化を高速に行う高速・診断初期化処理を行うためのルーチンを含んだＢＯＯＴプログラムを記憶する記憶手段と、
電源投入により前記ＢＯＯＴプログラムの実行を開始し、前記起動要因情報が示す起動要因がリンガの到来である場合には、前記高速・診断初期化処理を行うためのルーチンを実行した後、前記アプリケーションプログラムを実行し、この実行後、前記自動電源制御回路に電源切断の指令を送る制御手段とを具備することを特徴とする留守録機能付き情報処理装置。
【請求項２】　前記ＢＯＯＴプログラムは、前記高速・診断初期化処理を行うためのルーチンの他、システムの全てのハードウェア環境の診断と初期化を行うための充実診断処理のルーチンを含み、
前記制御手段は、当該ＢＯＯＴプログラムの実行の際、
ａ．前記起動要因情報が示す起動要因がリンガの到来である場合には、前記高速・診断初期化処理を行うためのルーチンを実行した後、前記アプリケーションプログラムを実行し、この実行後、前記自動電源制御回路に電源切断の指令を送り、
ｂ．前記起動要因情報が示す起動要因が電源投入のためのスイッチ操作である場合には、前記充実診断処理のルーチンを実行した後、前記オペレーティングシステムを起動することを特徴とする請求項１記載の留守録機能付き情報処理装置。
【請求項３】　電源が供給されない状況下においても記憶内容を保持する不揮発性記憶手段を具備し、
前記制御手段は、前記リンガの到来により前記ＢＯＯＴプログラムを実行し、その際のハードウェア環境の診断において異常を検出した場合には、異常があったことを示すリンガ起動エラー情報とその異常の内容を示す情報を前記不揮発性記憶手段に格納すると共に前記自動電源制御回路に電源切断の指令を送り、
前記スイッチ操作により前記ＢＯＯＴプログラムを実行し、その際のハードウェア環境の診断において異常を検出した場合は、その異常内容の表示を行うと共にシステムを停止させ、
前記ＢＯＯＴプログラムの実行において前記不揮発性記憶手段に前記リンガ起動エラー情報が記憶されている場合には前記不揮発性記憶手段に記憶された前記異常内容を示す情報の表示を行うことを特徴とする請求項２に記載の留守録機能付き情報処理装置。
【請求項４】　前記アプリケーションプログラムは、外来のリンガが電話に対応したものかファクシミリに対応したものかを判別し、当該リンガが電話に対応したものである場合には留守録着信処理を行い、ファクシミリに対応したものである場合には自動受信処理を行うものであることを特徴とする請求項１～３のいずれか１の請求項に記載の留守録機能付き情報処理装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は、ファクシミリ（以下、ＦＡＸと略する。）および電話（以下、ＴＥＬと略する。）の通信機能を有すると共にいわゆる留守録機能を有する情報処理装置に関する。
【０００２】
【従来の技術】従来、情報処理装置に留守録機能を持たせるためには、常時、情報処理装置の電源を投入状態にしておくと共にそのシステムを起動状態としておき、オペレーティングシステム（以下、ＯＳと略する。）とＴＥＬの留守録処理を備えたＦＡＸモデム用の業務用ＡＰ（以下、ＴＥＬＦＡＸ専用ＡＰと称する。）を稼働させておく必要があった。このための手段として、毎日、ある決まった時間に情報処理装置の電源を入れておくという方法を採っていた。
【０００３】この種の従来技術については、例えば特開平０５－０６１５６９号公報に開示されている。図６は同公報に開示された従来の装置の構成を示すものである。
【０００４】図６に示す情報処理装置は、現在の時刻データを送出する時計手段たる時計回路部６０１と、外部から設定される時刻データを保持する保持手段たる時刻設定回路部６０２と、この保持した時刻データと時計回路部６０１からの時刻データとを比較する比較手段たる自動起動回路部６０３と、この比較結果が一致したときに自装置の電源を投入する電源投入手段たる電源スイッチ部６０４とにより構成されている。この公報に記載の技術によれば、毎日、ある決まった時間に情報情報処理装置が自動起動されるため、結果的にシステムとＡＰとを常時稼働させておくことができる。
【０００５】また、レジューム技術を利用することにより高速に情報処理装置の起動を行うようにする技術も検討されていたが、この場合もなるべく消費電力を抑え、装置の高速な再起動を実現する必要がある。特開平０６－１６１５９０号公報にこの種のレジューム技術を利用した装置が開示されている。図７は同公報に開示された従来の装置の構成を示すものである。
【０００６】図７に示す装置においては、主記憶装置７０１のみに電源装置７０３から電源が供給され、主記憶

装置７０１以外への電源供給は遮断されており、これにより省電力化が図られている。そして、レジュームスイッチ７０７等からの起動要求があった場合、レジューム制御装置７０８の判断と制御により、そのまま主記憶装置７０１の主記憶情報の内容で高速に起動することでＡＰの作業再開が行われる。この場合、ＴＥＬＦＡＸ専用ＡＰを常に稼働させるには、ＴＥＬＦＡＸ専用ＡＰを常に主記憶上に常駐させる必要がある。

【０００７】

【発明が解決しようとする課題】ところで、上述した従来の留守録機能付き情報処理装置は以下の問題点を有していた。

【０００８】（１）従来の留守録機能付き情報処理装置は、起動中にかかってきたＴＥＬやＦＡＸの着信を失敗する可能性がある。すなわち、通常、情報処理装置の起動においては、環境の診断を行い、更にＯＳを起動し、その後に業務用のＡＰを起動し常駐させる、という一連の処理を必要とし、この処理には大変長時間を要する。このため、ある相手装置からの着信があった場合に、この一連の処理が長時間に及ぶことから、当該相手装置は大抵の場合にタイムアウトエラーとしての取扱い、すなわち、この情報処理装置の使用者が不在であるとみなし送信処理を止める取扱いをしてしまうからである。

【０００９】（２）従来の留守録機能付き情報処理装置は、リンガが来ない場合でも装置を稼働させておく必要があり、このために無駄な電力を消費してしまう。

【００１０】（３）上述したレジューム制御方式の装置は、レジュームで復帰する際、ハードウェア不調が発生したままで起動した場合に装置に異常が発生し、これにより業務用ＡＰが暴走してしまう可能性がある。

【００１１】この発明は、以上説明した事情に鑑みてなされたものであり、電源を常時投入状態とし、システムを稼働しておかなくても不定期に到来する電話やファクシミリの受信を行うことができ、また、留守録の際の異常発生による暴走の対策の施された留守録機能付き情報処理装置を提供することを目的とするものである。

【００１２】

【課題を解決するための手段】請求項１に係る発明は、所定の起動要因に応答して電源を投入または切断する手段および電源投入の起動要因を判別し、該判別結果を示す起動要因情報を出力する手段を備えた自動電源制御回路と、

ａ．オペレーティングシステム、

ｂ．電話の留守録処理およびファクシミリの自動受信処理を行うアプリケーションプログラム、および

ｃ．前記オペレーティングシステムを起動するためのルーチン並びに少なくとも前記アプリケーションプログラムの実行に必要とされるハードウェア環境の診断および初期化を高速に行う高速・診断初期化処理を行うためのルーチンを含んだＢＯＯＴプログラムを記憶する記憶手段と、電源投入により前記ＢＯＯＴプログラムの実行を開始し、前記起動要因情報が示す起動要因がリンガの到来である場合には、前記高速・診断初期化処理を行うためのルーチンを実行した後、前記アプリケーションプログラムを実行し、この実行後、前記自動電源制御回路に電源切断の指令を送る制御手段とを具備することを特徴とする留守録機能付き情報処理装置を要旨とする。

【００１３】請求項２に係る発明は、前記ＢＯＯＴプログラムは、前記高速・診断初期化処理を行うためのルーチンの他、システムの全てのハードウェア環境の診断と初期化を行うための充実診断処理のルーチンを含み、前記制御手段は、当該ＢＯＯＴプログラムの実行の際、

ａ．前記起動要因情報が示す起動要因がリンガの到来である場合には、前記高速・診断初期化処理を行うためのルーチンを実行した後、前記アプリケーションプログラムを実行し、この実行後、前記自動電源制御回路に電源切断の指令を送り、

ｂ．前記起動要因情報が示す起動要因が電源投入のためのスイッチ操作である場合には、前記充実診断処理のルーチンを実行した後、前記オペレーティングシステムを起動することを特徴とする請求項１記載の留守録機能付き情報処理装置を要旨とする。

【００１４】請求項３に係る発明は、電源が供給されない状況下においても記憶内容を保持する不揮発性記憶手段を具備し、前記制御手段は、前記リンガの到来により前記ＢＯＯＴプログラムを実行し、その際のハードウェア環境の診断において異常を検出した場合には、異常があったことを示すリンガ起動エラー情報とその異常の内容を示す情報を前記不揮発性記憶手段に格納すると共に前記自動電源制御回路に電源切断の指令を送り、前記スイッチ操作により前記ＢＯＯＴプログラムを実行し、その際のハードウェア環境の診断において異常を検出した場合は、その異常内容の表示を行うと共にシステムを停止させ、前記ＢＯＯＴプログラムの実行において前記不揮発性記憶手段に前記リンガ起動エラー情報が記憶されている場合には前記不揮発性記憶手段に記憶された前記異常内容を示す情報の表示を行うことを特徴とする請求項２に記載の留守録機能付き情報処理装置を要旨とする。

【００１５】請求項４に係る発明は、前記アプリケーションプログラムは、外来のリンガが電話に対応したものかファクシミリに対応したものかを判別し、当該リンガが電話に対応したものである場合には留守録着信処理を行い、ファクシミリに対応したものである場合には自動受信処理を行うものであることを特徴とする請求項１～３のいずれか１の請求項に記載の留守録機能付き情報処理装置を要旨とする。

【００１６】

【発明の実施の形態】以下、図面を参照し、本発明の実施の形態について説明する。

Ａ．第１の実施形態
図１は、本発明の第１の実施形態である留守録機能付き情報処理装置１０１の回路構成を示すブロック図である。同図において、１０３はこの情報処理装置１０１の制御中枢たるＣＰＵである。このＣＰＵ１０３からバス１０５が導出されており、このバス１０５にはＲＡＭ１０２、フラッシュＲＯＭ（以下、ＦＲＯＭと称する。）１０４および入出力機構１０６が接続されている。
【００１７】入出力機構１０６は、ＣＰＵ１０３と各種入出力装置との間で情報の授受が行われる際のインタフェースとしての役割を果す手段である。また、この入出力機構１０６は、後述する起動要因情報を保持し、ＣＰＵ１０３に通知する役割を果す。
【００１８】また、入出力機構１０６には、ハードディスク１０７と、ＦＡＸモデム１０８と、自動電源制御回路１０９とが接続されている。さらにこの情報処理装置１０１には、電源投入を指示するためのスイッチ１１０と、この情報処理装置内の各部に電源を供給する電源回路１１４が設けられている。電源回路１１４は、このスイッチ１１０の操作または上記自動電源制御回路１０９からの指令により電源投入／遮断が切り換えられるように構成されている。
【００１９】ＦＡＸモデム１０８は、コネクタたるＴＥＬ端子１１３を介して外部電話回線と接続されている。ＦＡＸモデム１０８は、この外部電話回線から到来するリンガを受信することにより、自動電源制御回路１０９にリンガ信号を供給する。
【００２０】自動電源制御回路１０９は、所定の起動要因があるとこれに応答して電源回路１１４の電源を自動に投入または切断する手段を有している。この起動要因の１つにＦＡＸモデム１０８からのリンガ信号の到来がある。自動電源制御回路１０９は、このリンガ信号を検出することにより、電源回路１１４のスイッチをＯＮ状態にして電源を投入し、この情報処理装置を自動起動させる。また、自動電源制御回路１０９は、電源回路１１４の電源投入が行われた場合にその起動要因が何であるかを判別する電源投入要因判別手段と、その判別結果を上述した起動要因情報として入出力機構１０６に通知する手段とを備えている。
【００２１】ハードディスク１０７は、周知の通り、記憶内容を変更することができ、かつ、電源が供給されない状況下においても記憶内容を保持することができる不揮発性の記憶手段である。このハードディスク１０７には、ソフトウェアとして、ＯＳ１１２と、ＴＥＬＦＡＸ専用ＡＰ１１１とが分割して記憶されている。これらのうちＴＥＬＦＡＸ専用ＡＰ１１１は、外来のリンガに応答して、ＦＡＸの受信またはＴＥＬの留守録を行うための一連の命令からなるアプリケーションプログラムである。
【００２２】ＦＲＯＭ１０４も、記憶内容を変更することができ、電源が供給されない状況下においても記憶内容を保持することができる不揮発性の記憶手段である。このＦＲＯＭ１０４には、ＯＳ１１２をロードするルーチン、少なくとも上記ＴＥＬＦＡＸ専用ＡＰ１１１の実行時に必要とされるシステムのハードウェア環境の診断と初期化を高速に行う高速・診断初期化処理をルーチンを含むＢＯＯＴプログラムが記憶されている。
【００２３】次に本実施形態の動作について、リンガによる電源ＯＮ時の場合とスイッチの投入による電源ＯＮ時の場合とに分けて説明する。図２は電源ＯＮ時のＢＯＯＴプログラムの処理フローを示し、図３はリンガ起動によるＴＥＬＦＡＸ専用ＡＰの処理フローを示してある。
【００２４】最初に図２を参照し、電源ＯＮ時の処理について説明する。外部の電話回線からのリンガが到来し、ＦＡＸモデム１０８から自動電源制御回路１０９にリンガ信号が送られると、自動電源制御回路１０９により電源回路１１４の電源投入が行われる。また、自動電源制御回路１０９の電源投入要因判別手段により、電源投入の起動要因の判別が行われ、その判別結果を示す起動要因情報、すなわち、この場合には起動要因がリンガの到来であることを示す起動要因情報が入出力機構１０６経由でＣＰＵ１０３に送られる。
【００２５】ＣＰＵ１０３は、電源が投入されたことにより、ＦＲＯＭ１０４内のＢＯＯＴプログラムの実行を開始する（ステップ２０１）。まず、ステップ２０２において、ＣＰＵ１０３は、ＦＲＯＭ１０４内にリンガ起動エラー情報が無いかどうかを判断する。このリンガ起動エラー情報がない場合にはステップ２０３に進み、入出力機構１０６から供給される起動要因情報に基づき起動要因を判別する。この場合、当該起動要因がリンガの到来であるとの判別結果が得られるため、ステップ２０３からステップ２０４に進み、実行対象を高速・診断初期化処理のルーチンに切り換え、少なくとも上記ＴＥＬＦＡＸ専用ＡＰ１１１の実行時に必要とされるハードウェア環境の診断と初期化を極めて短時間で処理する高速診断処理を実行する。この診断の最後に、正常に終了したかどうかを判断し（ステップ２０５）、正常に終了した場合にはステップ２０６でＦＲＯＭ１０４内のリンガ起動エラー情報をクリアする。
【００２６】診断が終了するとステップ２０７でリンガでの起動かどうかを再度調べ、リンガでの起動の場合はステップ２０８でＴＥＬＦＡＸ専用ＡＰを起動し、処理を終了する（ステップ２０９）。このようにリンガ起動の場合には、極めて所要時間の短い高速診断処理を実行した後、ＯＳを起動することなく、直ちにＴＥＬＦＡＸ専用ＡＰ１１１の実行に移行するので、相手装置がタイムアウトエラーとして取扱うこともない。
【００２７】一方、電源の起動がスイッチ１１０の押下により行われた場合には、起動要因がスイッチ押下であ

ることを示す起動要因情報が入出力機構１０６経由でＣＰＵ１０３に送られる。このため、ＢＯＯＴプログラムの実行においてステップ２０３に進んだ際、その起動要因の判別において当該起動がリンガ起動でないとの判別結果が得られることからステップ２１１に進むこととなる。そして、ステップ２１１に進むと、ＯＳが動作するために必要な全てのハードウェア環境の診断と初期化を行う充実診断処理を行う。その後、ステップ２０５に進み、正常に終了したかどうかを判断し正常に終了した場合、ステップ２０６でリンガ起動エラー情報をクリアする。そして、診断が終了するとステップ２０７でリンガでの起動かどうかを再度調べ、リンガでの起動でない場合はステップ２１８でＯＳを起動し、処理を終了する（ステップ２０９）。

【００２８】次に起動中に異常が発生した場合の処理を説明を行う。最初にリンガによる起動中にハードウェアの異常が発生した場合を説明する。ステップ２０４のハードウェア診断で異常が発生した場合、その後、ステップ２０５で正常終了かどうかを調べる。ここで、異常が発生した場合、ステップ２１２で異常内容のエラー表示を行う。このエラー表示処理の後、ステップ２１３で起動の要因を調べ、リンガ起動の場合は、ステップ２１４でＦＲＯＭ１０４内にリンガ起動エラー情報をセットし、ステップ２１５で異常内容の情報をＦＲＯＭ１０４内に格納する。次にステップ２１６に進むと、ＣＰＵ１０３はこのＢＯＯＴプログラムに従って自動電源制御回路１０９に電源切断の指令を送る。この結果、自動電源制御回路１０９は、電源回路１１４のスイッチをＯＦＦ状態とし、この情報処理装置を自動停止させる。これにより処理が終了することとなる。

【００２９】もし、スイッチ１１０の押下により起動が行われた場合において、ステップ２１１のハードウェア診断で異常が発生した場合も、その後、ステップ２０５で正常終了かどうかを調べる。異常が発生した場合ステップ２１２で異常内容のエラー表示を行う。そして、エラー表示処理後、ステップ２１３で起動の要因を調べ、リンガ起動でない場合は、ＦＲＯＭ１０４内にステップ２１９でリンガ起動エラー情報をクリアし、ステップ２２０でこのままシステムを停止させる。

【００３０】その後、再びこの情報処理装置の起動が行われると、ＢＯＯＴプログラムの実行の際、ステップ２０２でリンガ起動エラー情報が無いかどうかを判断する。ここで、情報処理装置のリンガ起動は過去行われ、その際のＢＯＯＴプログラムの実行においてハードウェアの異常が検出された場合、同ＢＯＯＴプログラムのステップ２１４、２１５においてリンガ起動エラー情報および異常内容を示す情報がＦＲＯＭ１０４に格納される。このＦＲＯＭ１０４は不揮発性の記憶手段であるため、その後の電源断によって消滅しない。そして、今回のＢＯＯＴプログラムの起動においてステップ２０２でその内容を確認することとなり、その際にＦＲＯＭ１０４内にリンガ起動エラー情報があれば、ステップ２１０で異常内容のエラー表示を行い、ステップ２０３に処理が移行する。

【００３１】次に、図３を用いて、リンガで起動した場合のＴＥＬＦＡＸ専用ＡＰの処理フローを説明する。ステップ３０１でＢＯＯＴプログラムからＴＥＬＦＡＸ専用ＡＰが起動される。ステップ３０２で受信がＴＥＬかＦＡＸかを調べる。ＴＥＬの場合はステップ３０３で留守録の処理を行う。もし、ステップ３０２でＦＡＸの場合は、ステップ３０５でＦＡＸの受信処理を行う。次にステップ３０４に進むと、ＣＰＵ１０３はこのＢＯＯＴプログラムに従って自動電源制御回路１０９に電源切断の指令を送る。この結果、自動電源制御回路１０９は、電源回路１１４のスイッチをＯＦＦ状態とし、この情報処理装置を自動停止させる。これにより処理が終了することとなる。

【００３２】Ｂ．第２の実施形態

図４は、本発明の第２の実施形態である情報処理装置４０１の回路構成を示すブロック図である。上記第１の実施形態では、ハードディスク１０７にＴＥＬＦＡＸ専用ＡＰ１１１を搭載した。本実施形態は、このようにする代わりに、図４に示すように、ＢＯＯＴプログラムが存在するＦＲＯＭ４０４の空き領域を用いてＴＥＬＦＡＸ専用ＡＰ４１１を搭載するものである。他の構成については、上記第１の実施形態と同様である。従って、図４に示す構成において、前掲図１において示した各部と対応する各部分には、図１において使用している各符号と十の位および一の位の数字を同じくする４００番台の符号を付すことにより上記第１の実施形態との対応関係を明確化し、構成の説明に代える。本実施形態においても上述した第１の実施形態と同様な作用効果が得られる。

【００３３】Ｃ．第３の実施形態

図５は、この発明の第３の実施形態である留守録機能付き情報処理装置の構成を示すブロック図である。本実施形態は、上述の第１の実施形態におけるＦＲＯＭ１０４を、バッテリー５１５によってバックアップされ、電源を落としても内容が消去されないように構成した不揮発性メモリ（以下、ＢＵＭと称する。）５１６と、内容を書き替えることができないＲＯＭ５０４に置き換えたものである。上記第１の実施形態においては、リンガ起動エラー情報と異常内容の情報をＦＲＯＭ１０４に格納したが、本実施形態ではこれらの情報をＢＵＭ５１６に格納するようにしている。また、上記第１の実施形態においてＢＯＯＴプログラムはＦＲＯＭ１０４に格納したが、本実施形態ではこのＢＯＯＴプログラムをＲＯＭ５０４に格納している。他の構成については、上記第１の実施形態と同様である。従って、図５に示す構成において、前掲図１において示した各部と対応する各部分には、図１において使用している各符号と十の位および一

の位の数字を同じくする５００番台の符号を付すことにより上記第１の実施形態との対応関係を明確化し、構成の説明に代える。本実施形態においても上述した第１の実施形態と同様な作用効果が得られる。

【００３４】

【発明の効果】本発明によれば以下の効果が得られる。

（１）本発明によれば、リンガが入った時に自動電源制御回路によって装置が起動されると共に起動要因の判定が行われ、リンガによる起動であるとの判定結果が得られた場合には、装置の高速起動が行われ、タイムアウトを生じさせることなく、ＴＥＬＦＡＸ専用ＡＰを稼動させ、リンガ処理が行われ、業務終了後には装置の電源がＯＦＦとされる。従って、本発明によれば、情報処理装置を常時稼働状態にしておかなくても、留守録機能を行わせることができる。

（２）本発明によれば、情報処理装置を無駄に稼働させることがないため、無駄な電力消費を減らすことができる。

（３）本発明によれば、リンガ起動時にハードウェア環境の診断や初期化を行い、異常を検出した場合にその旨の記録を残し、自動電源制御回路により装置の電源を切断するようにしたので、留守録起動中に装置に異常が発生した場合でもハードウェアを暴走させることなく、暴走によるデータ破壊等を防止することができる。

【図面の簡単な説明】

【図１】この発明の第１の実施形態である留守録機能付き情報処理装置の構成を示すブロック図である。

【図２】同実施形態における電源ＯＮ時のＢＯＯＴプログラムの処理フローを示すフローチャートである。

【図３】同実施形態においてリンガ起動時に実行されるＴＥＬＦＡＸ専用ＡＰの処理フローを示すフローチャートである。

【図４】この発明の第２の実施形態である留守録機能付き情報処理装置の構成を示すブロック図である。

【図５】この発明の第３の実施形態である留守録機能付き情報処理装置の構成を示すブロック図である。

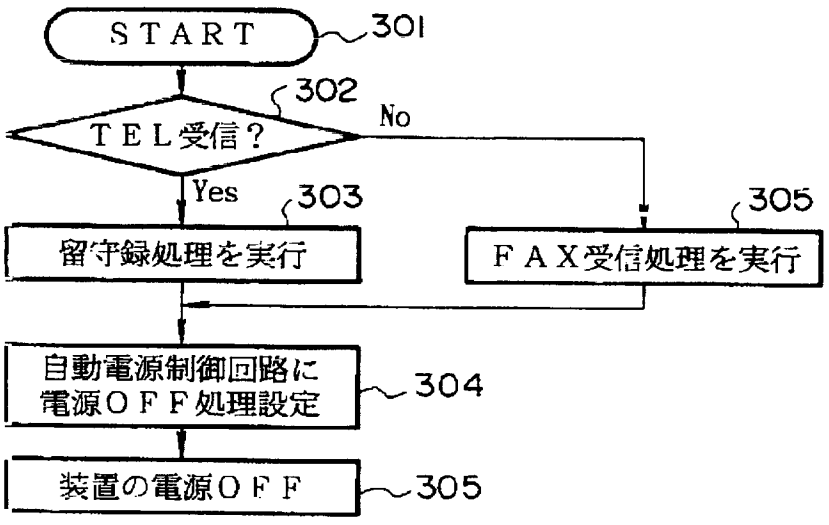
【図６】従来の情報処理装置の構成を示すブロック図である。

【図７】従来の情報処理装置の構成を示すブロック図である。

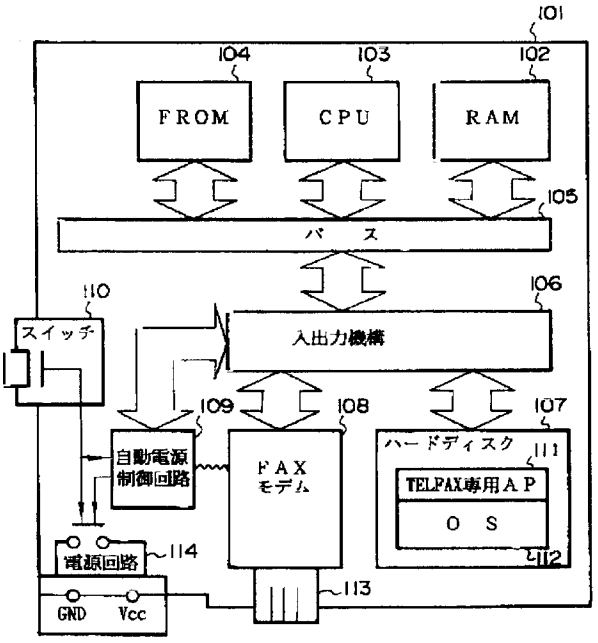
【符号の説明】

１０１，４０１，５０１	留守録機能付き情報処理装置
１０２，４０２，５０２	ＲＡＭ
１０３，４０３，５０３	ＣＰＵ（制御手段）
１０４，４０４	ＦＲＯＭ（書替可能な不揮発性記憶手段）
５０４	ＲＯＭ
５１６	ＢＵＭ（書替可能な不揮発性記憶手段）
１０５，４０５，５０５	バス
１０６，４０６，５０６	入出力機構
１０７，４０７，５０７	ハードディスク
１０８，４０８，５０８	ＦＡＸモデム
１０９，４０９，５０９	自動電源制御回路
１１０，４１０，５１０	スイッチ
１１１，４１１，５１１	ＴＥＬＦＡＸ専用ＡＰ（アプリケーションプログラム）
１１２，４１２，５１２	ＯＳ（オペレーティングシステム）
１１３，４１３，５１３	ＴＥＬ端子
１１４，４１４，５１４	電源回路

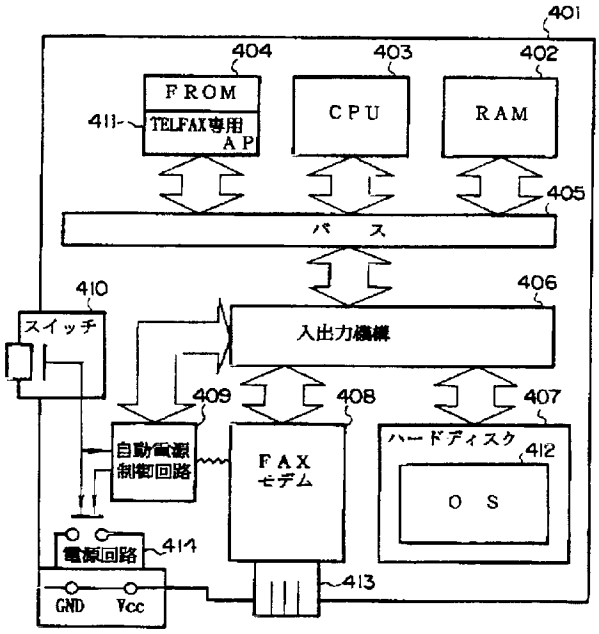
【図３】



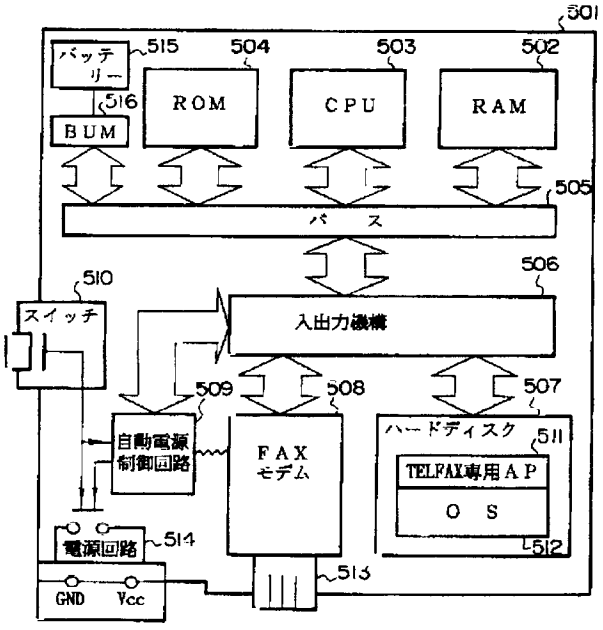
【図1】



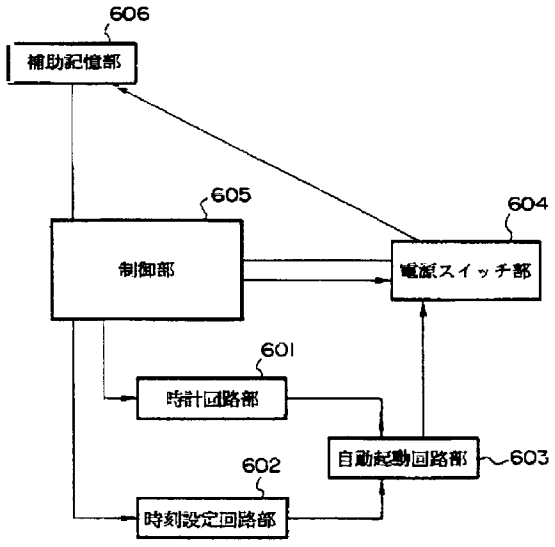
【図4】



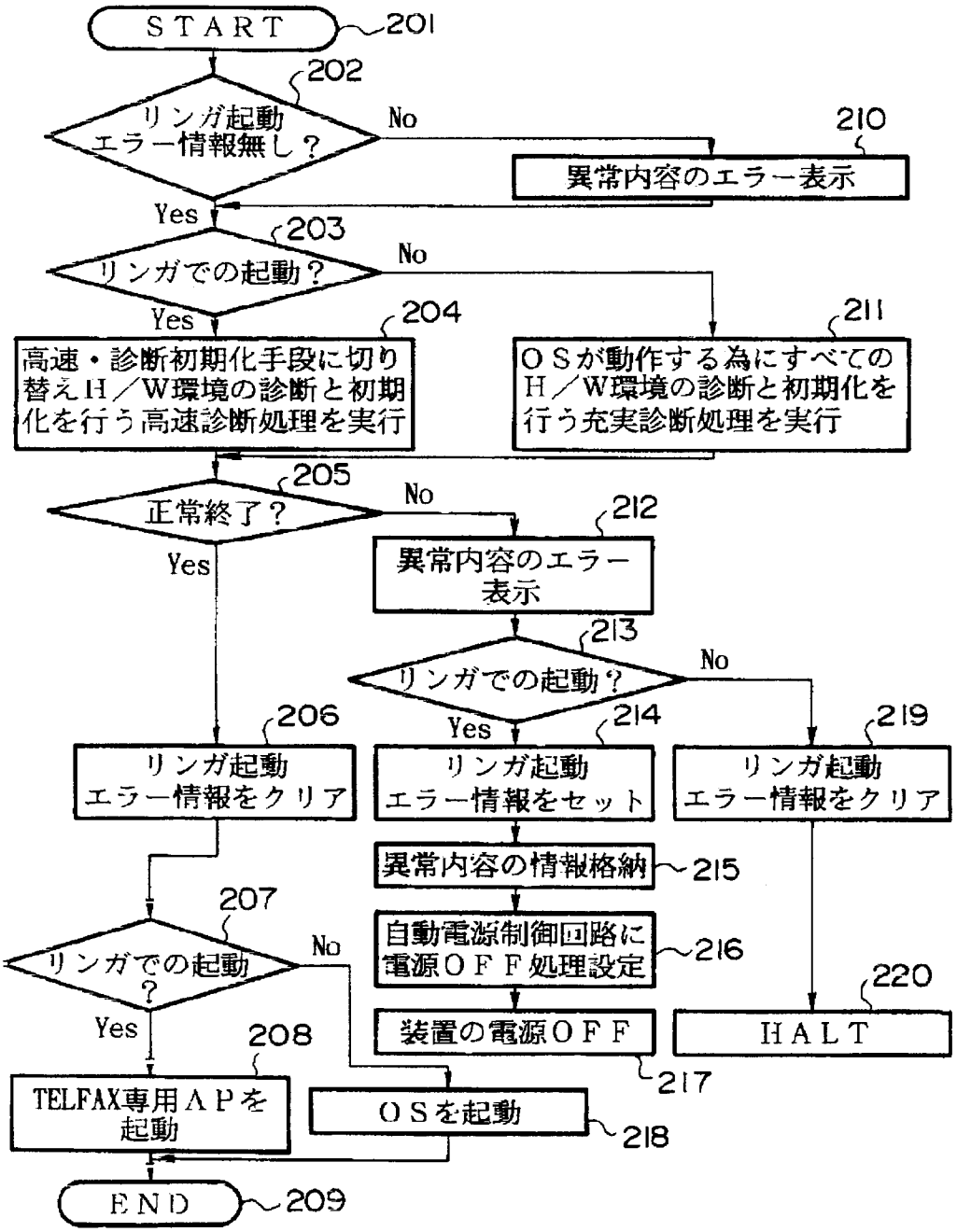
【図5】



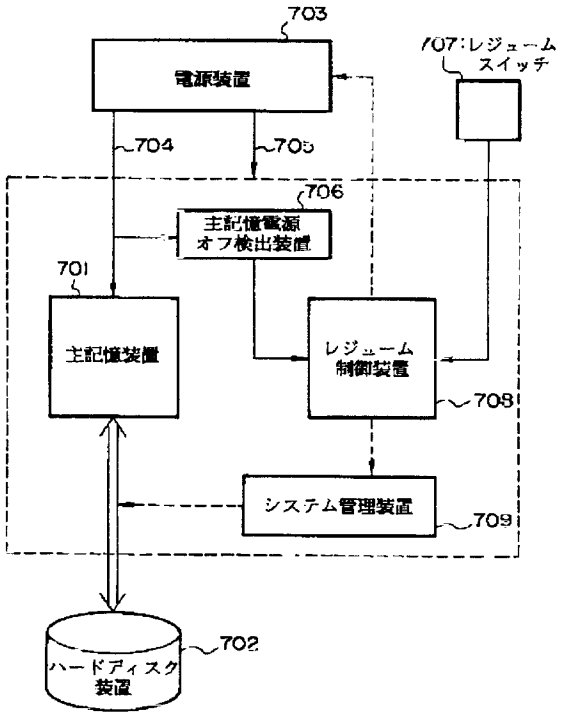
【図6】



【図２】


START
201
202
リンガ起動
エラー情報無し？
No
210
異常内容のエラー表示
Yes
203
リンガでの起動？
No
Yes
204
高速・診断初期化手段に切り替えH／W環境の診断と初期化を行う高速診断処理を実行
211
ＯＳが動作する為にすべてのH／W環境の診断と初期化を行う充実診断処理を実行
205
正常終了？
No
212
異常内容のエラー表示
Yes
213
リンガでの起動？
No
Yes
206
リンガ起動
エラー情報をクリア
214
リンガ起動
エラー情報をセット
219
リンガ起動
エラー情報をクリア
215
異常内容の情報格納
207
リンガでの起動？
No
216
自動電源制御回路に電源ＯＦＦ処理設定
220
Yes
208
装置の電源ＯＦＦ
217
HALT
TELFAX専用ＡＰを起動
ＯＳを起動
218
END
209

【図７】



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INVENTOR : SUGIYAMA TADASHI;

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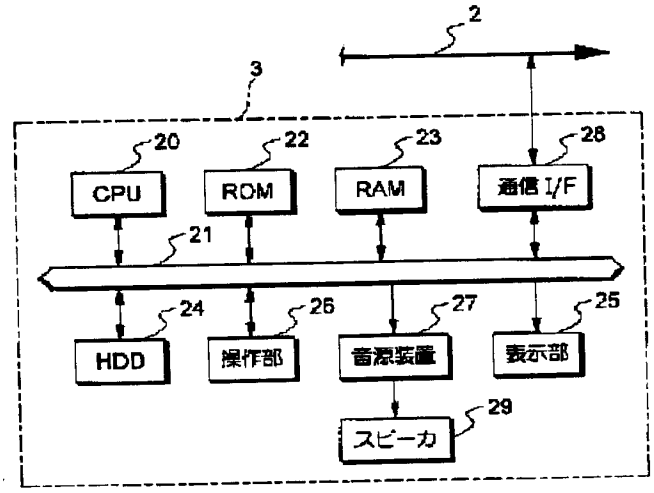
TITLE : COMMUNICATION TERMINAL AND COMMUNICATION SYSTEM



ABSTRACT : PROBLEM TO BE SOLVED: To reduce trouble and cost which are needed for the updation of a service program that makes a processing means execute a fault diagnosis, repair, etc., in a communication terminal.

SOLUTION: A karaoke terminal 3 has a ROM 22 and the ROM 22 stores a service program which makes a CPU 20 execute processing that checks and repairs the failure, etc., of a hard disk drive 24. The drive 24 stores an area where an application program which makes the CPU 20 carry out karaoke play processing, etc., is stored and the service program which makes the CPU 20 execute processing that checks and repairs the failure, etc., of the terminal 3. In the case of updating the service program, a new service program transmitted from a public line network 2 is inputted to the CPU 20 through a communication interface 28 and the CPU 20 writes the new service program in the drive 24.

は、このようなアプリケーションプログラムにしたがってＣＰＵ２０により実行される処理が正常に実行されているかをテストする故障診断プログラムＰ３や、アプリケーションプログラムにしたがった処理が正常に実行されていない場合に、ＣＰＵ２０に修復処理を実行させる修復プログラムＰ４などが記憶されている。

【００１３】図１において、操作部２６は、テンキーやモード切換キーなどの各種のキースイッチを備えており、使用者がこれらのスイッチを操作して、予約するカラオケ曲の曲番号等を入力することができる。上述したように、カラオケ端末３の電源がオンされると、ハードディスク装置２４に記憶されたアプリケーションプログラムがＲＡＭ２３にロードされ、カラオケ演奏処理が開始されるが、カラオケ端末３の起動時に操作部２６で特殊なキー操作を行うことにより、ハードディスク装置２４またはＲＯＭ２２からサービスプログラムがＲＡＭ２３にロードされ、故障診断等のサービスプログラムが実行されるようになっている。このように本実施形態では、通常のカラオケ演奏処理を行う場合と、故障診断等のサービスプログラムを実行する場合との起動方法を分けている。本実施形態によれば、サービスプログラムの起動時に特殊なキー操作を必要とするので、通常時に誤ってサービスプログラムが実行されてしまうといった誤操作を低減できる。なお、サービスプログラムを実行させる専用のスイッチ等を操作部２６に設け、このスイッチを押下することによりサービスプログラムが実行されるようにしてもよい。この場合、専用スイッチにカバー等を設けておき、誤って押下される可能性を少なくすることが好ましい。

【００１４】音源装置２７は、カラオケ曲データに含まれる楽音データに基づいて、楽音信号を生成するものである。ＲＡＭ２３にロードされたカラオケ曲データが順次音源装置２７に入力され、これにより音源装置２７は楽音信号を順次生成し、生成した楽音信号をスピーカ２９に出力する。スピーカ２９は、音源装置２７において生成された楽音信号をアナログデータに変換した後増幅して放出し、これによりカラオケ曲データに対応した演奏がなされる。

【００１５】表示部２５はモニタを備えており、カラオケ演奏時にＣＤ－ＲＯＭ等から読み出した映像をモニタに出力する。このとき、モニタに表示される映像には、カラオケ曲データに含まれる歌詞データに基づいた歌詞が合成されて出力される。また、このカラオケ端末３に異常が発生した場合には、その異常内容等を表示する。

【００１６】公衆回線網２からカラオケ端末３に送信されるデータは、通信インターフェース２８を介してＲＡＭ２３やハードディスク装置２４に書き込まれるようになっている。

【００１７】Ｃ．カラオケ端末の動作

次に、上述した構成のカラオケ端末３の動作について説明する。

Ｃ－１．サービスプログラム配信処理

まず、センタ１から公衆回線網２を介して送信されたサービスプログラムをハードディスク装置２４のサービス記憶エリア２４ｃに書き込むサービスプログラム配信処理について説明する。上述したようにセンタ１から公衆回線網２を介してサービスプログラム含んだサービスプログラムデータがカラオケ端末３に送信される。このようにセンタ１から送信されるサービスプログラムデータのヘッダには、上述した故障診断プログラムＰ３や修復プログラムＰ４などのプログラムの種類が書き込まれている。

【００１８】センタ１から送信されるサービスプログラムデータは、通信インターフェース２８を介してＣＰＵ２０に入力される。ＣＰＵ２０は入力されるサービスプログラムデータのヘッダから、このサービスプログラムを書き込むエリアを指定し、ハードディスク装置２４のサービス記憶エリア２４ｃに書き込む。例えば、送信されたサービスプログラムが故障診断プログラムＰ３である場合には、サービス記憶エリア２４ｃに既に書き込まれている故障診断プログラムＰ３上に新たに送信された故障診断プログラムＰ３を上書きする。このようにして、ハードディスク装置２４に記憶されたサービスプログラムが更新される。

【００１９】本実施形態に係る通信カラオケシステムでは、ハードディスク装置２４に関するサービスプログラム以外のサービスプログラムを書き換え可能なハードディスク装置２４に記憶するようにしたので、サービスプログラムを更新する場合にも、センタ１から公衆回線網２を介してサービスプログラムを送信すればよい。従来のカラオケ装置では、サービスプログラムがＲＯＭに記憶されていたので、サービスプログラムを更新する場合には、ＲＯＭ交換を行う必要があったが、このカラオケ端末３ではそのような作業を行う必要がなく、簡単かつ低コストでサービスプログラムを更新することができる。また、従来では、サービスプログラムの更新が困難または不可能な場合があり、新たなアプリケーションプログラムの変更や周辺機器の追加を行う自由度が制限されることもあった。しかし、このカラオケ端末３では、サービスプログラムの更新が簡易かつ低コストで実施できるため、アプリケーションプログラムの変更や周辺機器の追加などの自由度が大きくなる。

【００２０】なお、上述したようにセンタ１から公衆回線網２を介して送信されるサービスプログラムデータに限らず、ＣＤ－ＲＯＭ等に記憶されたサービスプログラムデータを図示せぬＣＤ－ＲＯＭドライブ等により読み出して、ハードディスク装置２４に記憶されたサービスプログラムを更新するようにしてもよい。

【００２１】また、本実施形態においては、ハードディスク装置２４のサービス記憶エリア２４ｃに既にサービ

域、およびサービスプログラムを記憶する第２の領域を有する磁気記憶手段と、前記磁気記憶手段に関するサービスプログラムを記憶する不揮発性メモリと、前記磁気記憶手段に記憶された前記アプリケーションプログラム、前記サービスプログラム、または前記不揮発性メモリに記憶された前記磁気記憶手段に関するサービスプログラムにしたがった処理を実行する処理手段と、通信網を介して送信されるサービスプログラムを受信した場合に、前記磁気記憶手段における第２の領域に、受信したサービスプログラムを書き込む書込手段とを具備することを特徴としている。

【０００６】また、請求項２に記載の通信端末は、請求項１に記載の通信端末において、前記不揮発性メモリは、書き換え可能なフラッシュメモリであり、通信網を介して送信される前記磁気記憶手段に関するサービスプログラムを受信した場合、前記書込手段は、前記不揮発性メモリに、受信した前記磁気記憶手段に関するサービスプログラムを書き込むことを特徴としている。

【０００７】また、請求項３に記載の通信端末は、請求項１または２に記載の通信端末において、前記アプリケーションプログラム、前記サービスプログラムまたは前記磁気記憶手段に関するサービスプログラムにしたがった処理の実行開始を前記処理手段に指示する入力手段をさらに具備し、前記処理手段は、第１の処理手順により前記入力手段から処理開始指示が入力された場合、前記アプリケーションプログラムにしたがった処理を実行し、前記第１の処理手順と異なる第２の処理手順により前記入力手段から処理開始指示が入力された場合、前記サービスプログラムまたは前記磁気記憶手段に関するサービスプログラムにしたがった処理を実行することを特徴としている。

【０００８】また、請求項４に記載の通信システムは、通信網を介して送信されるデータを受信する通信端末であって、所定のアプリケーションプログラムを記憶する第１の領域、およびサービスプログラムを記憶する第２の領域を有する磁気記憶手段と、前記磁気記憶手段に関するサービスプログラムを記憶する不揮発性メモリと、前記磁気記憶手段に記憶された前記アプリケーションプログラム、前記サービスプログラム、または前記不揮発性メモリに記憶された前記磁気記憶手段に関するサービスプログラムにしたがった処理を実行する処理手段と、通信網を介して送信されるサービスプログラムを受信した場合に、前記磁気記憶手段における第２の領域に、受信したサービスプログラムを書き込む書込手段とを有する通信端末と、前記通信端末に通信網を介してサービスプログラムを送信するデータ送信装置とを具備することを特徴としている。

【０００９】

【発明の実施の形態】以下、図面を参照して本発明の実施形態について説明する。

Ａ．通信システム

まず、図１は本発明の一実施形態に係る通信ケシステムの構成を示す図であり、この実施形態においては、本発明が適用される通信システムが通信カラオケシステムである場合について説明する。同図において、符号１は通信カラオケシステムのセンタ局（データ送信装置）を示す。センタ１には、公衆電話回線あるいはＩＳＤＮ等の公衆回線網（通信網）２を介して複数のカラオケ端末（通信端末）３が接続されており、センタ１は公衆回線網２を介して各カラオケ端末３に後述するアプリケーションプログラムやサービスプログラムを配信することができるようになっている。

【００１０】Ｂ．カラオケ端末の構成

次に、カラオケ端末３について説明する。図２に示すように、カラオケ端末３は、アプリケーションプログラムやサービスプログラムなどの各種プログラムにしたがって装置各部を制御するＣＰＵ（処理手段、書込手段）２０を備えている。ＣＰＵ２０には、バス２１を介してＲＯＭ（不揮発性メモリ）２２、ＲＡＭ２３、ハードディスク装置（磁気記憶手段）２４、表示部２５、操作部（入力手段）２６、音源装置２７および通信インターフェース２８が接続されている。

【００１１】図３に示すように、ＲＯＭ２２には、当該カラオケ端末を起動するために必要な起動プログラムが記憶されている。また、ＲＯＭ２２には、上述した起動プログラム以外にも、ハードディスク装置２４を初期化する初期化プログラムＰ１、およびハードディスク装置２４を検査するＨＤＤ検査プログラムＰ２などが記憶されている。これらの初期化プログラムＰ１およびＨＤＤ検査プログラムＰ２は、図１に示すハードディスク装置２４に対して検査処理や初期化処理などを行うサービスプログラムである。ＲＡＭ２３は、上述したプログラムデータや、カラオケ曲データを一時的に記憶するためなどに使用する。

【００１２】図４に示すように、ハードディスク装置２４は、アプリケーションプログラムを記憶するアプリケーション記憶エリア（第１の領域）２４ａと、多数のカラオケ曲データを記憶するカラオケ曲記憶エリア２４ｂと、サービスプログラムを記憶するサービス記憶エリア（第２の領域）２４ｃとを有している。通常、カラオケ端末３の電源がオンされると、図１に示すＲＯＭ２２に記憶された起動プログラムが読み出され、これによりアプリケーション記憶エリア２４ａに記憶されたアプリケーションプログラムがＲＡＭ２３にロードされるようになっている。また、使用者にカラオケ曲番号が指定されると、ＣＰＵ２０がＲＡＭ２３にロードされたアプリケーションプログラムにしたがって行う制御により、カラオケ曲記憶エリア２４ｂから指定されたカラオケ曲データが読み出され、ＲＡＭ２３にロードされる。サービス記憶エリア２４ｃに記憶されているサービスプログラム

【特許請求の範囲】
【請求項１】　通信網を介して送信されるデータを受信する通信端末であって、
所定のアプリケーションプログラムを記憶する第１の領域、およびサービスプログラムを記憶する第２の領域を有する磁気記憶手段と、
前記磁気記憶手段に関するサービスプログラムを記憶する不揮発性メモリと、
前記磁気記憶手段に記憶された前記アプリケーションプログラム、前記サービスプログラム、または前記不揮発性メモリに記憶された前記磁気記憶手段に関するサービスプログラムにしたがった処理を実行する処理手段と、
通信網を介して送信されるサービスプログラムを受信した場合に、前記磁気記憶手段における第２の領域に、受信したサービスプログラムを書き込む書込手段とを具備することを特徴とする通信端末。
【請求項２】　前記不揮発性メモリは、書き換え可能なフラッシュメモリであり、
通信網を介して送信される前記磁気記憶手段に関するサービスプログラムを受信した場合、前記書込手段は、前記不揮発性メモリに、受信した前記磁気記憶手段に関するサービスプログラムを書き込むことを特徴とする請求項１に記載の通信端末。
【請求項３】　前記アプリケーションプログラム、前記サービスプログラムまたは前記磁気記憶手段に関するサービスプログラムにしたがった処理の実行開始を前記処理手段に指示する入力手段をさらに具備し、
前記処理手段は、第１の処理手順により前記入力手段から処理開始指示が入力された場合、前記アプリケーションプログラムにしたがった処理を実行し、前記第１の処理手順と異なる第２の処理手順により前記入力手段から処理開始指示が入力された場合、前記サービスプログラムまたは前記磁気記憶手段に関するサービスプログラムにしたがった処理を実行することを特徴とする請求項１または２に記載の通信端末。
【請求項４】　通信網を介して送信されるデータを受信する通信端末であって、所定のアプリケーションプログラムを記憶する第１の領域、およびサービスプログラムを記憶する第２の領域を有する磁気記憶手段と、前記磁気記憶手段に関するサービスプログラムを記憶する不揮発性メモリと、前記磁気記憶手段に記憶された前記アプリケーションプログラム、前記サービスプログラム、または前記不揮発性メモリに記憶された前記磁気記憶手段に関するサービスプログラムにしたがった処理を実行する処理手段と、通信網を介して送信されるサービスプログラムを受信した場合に、前記磁気記憶手段における第２の領域に、受信したサービスプログラムを書き込む書込手段とを有する通信端末と、
前記通信端末に通信網を介してサービスプログラムを送信するデータ送信装置とを具備することを特徴とする通信システム。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、故障診断や修復などをコンピュータに実行させるサービスプログラムを記憶した通信端末、およびこの通信端末を備えた通信システムに関する。
【０００２】
【従来の技術】近年、いわゆるカラオケ装置には通信機能を有するものがあり、ホスト局から通信網を介して送信される曲データに基づいて、端末であるカラオケ装置が演奏を実行する通信カラオケシステムが普及している。このような通信カラオケシステムでは、新しいアプリケーションプログラム、例えばカラオケ演奏処理プログラムや歌唱採点プログラムなどを各端末であるカラオケ装置に供給する場合、センタ局から通信網を介して新しいアプリケーションプログラムデータを送信している。端末であるカラオケ装置側では、このアプリケーションプログラムを受信して、ハードディスク装置などに記憶させている。
【０００３】
【発明が解決しようとする課題】ところで、上述したような通信カラオケシステムにおいては、カラオケ装置の故障診断、検査、修復、およびアプリケーションプログラムに対するテストや故障診断などをコンピュータに実行させるサービスプログラムは、カラオケ装置内のＲＯＭに記憶されており、書き換えることが不可能であった。従って、上述したように新しいアプリケーションプログラムを通信網を介してホスト局から送信した場合にも、そのアプリケーションプログラムに対してテストや故障診断等を実行させるサービスプログラムを更新するには、カラオケ装置内のＲＯＭを、新しいサービスプログラムが記憶されたＲＯＭに交換する必要があった。このため、サービスプログラムの更新には、手間やコストがかかっていた。また、ＲＯＭはハードディスクなどと比較して小容量であるため、サービスプログラムが大容量の記憶領域を必要とする場合には、サービスプログラムを記憶させることはできなかった。
【０００４】本発明は、上記の事情を考慮してなされたものであり、故障診断や修復などを処理手段に実行させるサービスプログラムの更新にかかる手間やコストを低減することが可能であり、かつ大容量のサービスプログラムを記憶することが可能な通信端末、およびこの通信端末を備える通信システムを提供することを目的とする。
【０００５】
【課題を解決するための手段】上記課題を解決するため、本発明の請求項１に記載の通信端末は、通信網を介して送信されるデータを受信する通信端末であって、所定のアプリケーションプログラムを記憶する第１の領

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(71)出願人　000004075
ヤマハ株式会社
静岡県浜松市中沢町10番１号
(72)発明者　杉山　正
静岡県浜松市中沢町10番１号　ヤマハ株式会社内
(74)代理人　100098084
弁理士　川▲崎▼　研二　（外１名）

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5B089 GA17 HA01 JA10 JA34 JB07
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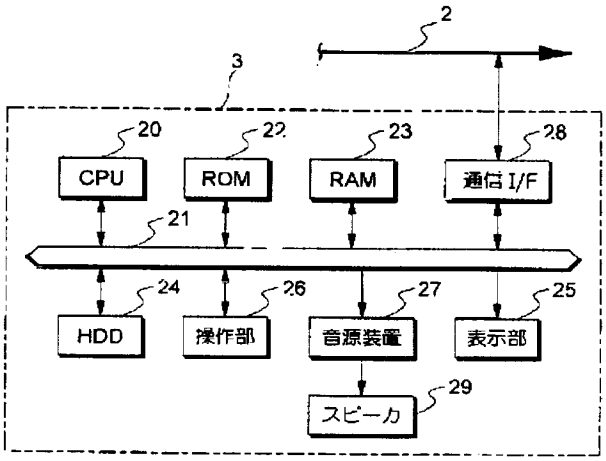
5D108 BF20 BG06

(54)【発明の名称】　通信端末および通信システム

(57)【要約】
【課題】　通信端末において、故障診断や修復などを処理手段に実行させるサービスプログラムの更新にかかる手間やコストを低減する。
【解決手段】　カラオケ端末３は、ＲＯＭ２２を有しており、ＲＯＭ２２には、ハードディスク装置２４の故障等を検査・修復する処理をＣＰＵ２０に実行させるサービスプログラムが記憶されている。ハードディスク装置２４には、ＣＰＵ２０にカラオケ演奏処理等を実行させるアプリケーションプログラムを記憶するエリアと、このカラオケ端末３の故障等を検査・修復する処理をＣＰＵ２０に実行させるサービスプログラムが記憶されている。サービスプログラムを更新する場合には、公衆回線網２から送信される新たなサービスプログラムを通信インターフェース２８を介してＣＰＵ２０に入力され、ＣＰＵ２０が新しいサービスプログラムをハードディスク装置２４に書き込む。



スプログラムが記憶されており、記憶されたサービスプログラムを、送信される新たなサービスプログラムに書き換える場合について説明したが、サービス記憶エリア２４ｃにサービスプログラムが記憶されていない状態で、公衆回線網２を介して送信されるサービスプログラムを書き込むようにしてもよい。また、サービス記憶エリア２４ｃに既に記憶されたサービスプログラムに加えて、公衆回線網２を介して送信されるサービスプログラムを書き込むようにしてもよい。

【００２２】Ｃ－２．カラオケ端末異常時の復旧処理

次に、このカラオケ端末３を起動したときに、何らかの異常が発生した場合の復旧処理について図５を用いて説明する。同図に示すように、まず、使用者によりカラオケ端末３の電源がオンされると、ＲＯＭ２２に記憶された起動プログラムが読み出される（ステップＳａ１）。この後、カラオケ端末３に異常が発生しない場合には（ステップＳａ２）、ハードディスク装置２４のアプリケーション記憶エリア２４ａに記憶されたアプリケーションプログラムがＲＡＭ２３にロードされ、通常のカラオケ演奏処理がなされる（ステップＳａ３）。

【００２３】一方、このカラオケ端末３に異常が発生した場合（ステップＳａ２）、その異常がハードディスク装置２４に関する異常であるか否かを判断する（ステップＳａ４）。ここで、ハードディスク装置２４に関する異常であると判断した場合、ＣＰＵ２０によりＲＯＭ２２に記憶されたＨＤＤ検査プログラムＰ２が実行され（ステップＳａ５）、ハードディスク装置２４の異常内容がチェックされる。そして、異常内容が確認されると、確認された内容が表示部２５のモニタに表示される（ステップＳａ６）。

【００２４】この後、表示部２５のモニタに表示された異常内容がハードディスク装置２４自体の損傷でない場合、例えば記憶されているデータが破壊された場合などには、ＣＰＵ２０により初期化プログラムＰ１が実行され（ステップＳａ７）、ハードディスク装置２４を初期化する。この後、ハードディスク装置２４の初期化が正常に終了したかが確認され（ステップＳａ８）、初期化が正常に終了した場合、ハードディスク装置２４のバックアップデータが記憶されたＣＤ－ＲＯＭから、ＣＤ－ＲＯＭドライブ（図示略）によりバックアップデータを読み出し、ハードディスク装置２４へ書き込む（ステップＳａ９）。このようにして、ハードディスク装置２４の異常に対する復旧処理が終了する。一方、ハードディスク装置２４の初期化が不可能な場合には、表示部２５のモニタに修復不能であることが表示される（ステップＳａ１０）。修復不可能が表示された場合、例えばハードディスク装置２４自体が損傷している場合には、カラオケ端末３の製造者や修理会社等に修理を依頼する。

【００２５】このようにして、ハードディスク装置２４の復旧処理が行われた後、ハードディスク装置２４以外の異常が発生しているか否かが判断される（ステップＳａ１１）。ここで、他に異常が発生していない場合には、ハードディスク装置２４からアプリケーションプログラムがＲＡＭ２３にロードされ、通常のカラオケ演奏処理が行われる（ステップＳａ３）。

【００２６】一方、ステップＳａ９でハードディスク装置２４以外の異常があると判断された場合には、ＣＰＵ２０によりハードディスク装置２４に記憶された故障診断プログラムＰ３が実行される（ステップＳａ１２）。故障診断プログラムＰ３が実行されると、カラオケ端末３のハードディスク装置２４以外の各部について故障診断が行われ、表示部２５にモニタに異常内容が表示される（ステップＳａ１３）。

【００２７】そして、ハードディスク装置２４に記憶された修復プログラムＰ４が実行され、ステップＳａ１３で診断された異常内容の修復処理が行われる（ステップＳａ１４）。そして、修復プログラムＰ４に基づく修復処理により、異常が修復されると（ステップＳａ１５）、通常のカラオケ演奏処理が実行される（ステップＳａ３）。修復プログラムＰ４による修復が不可能な場合、表示部２５のモニタにその旨が表示される（ステップＳａ１６）。この場合、使用者は、カラオケ端末３の製造者や修理会社等に修理を依頼する必要がある。

【００２８】なお、カラオケ端末３を起動したときに（ステップＳａ１）、発生した異常がハードディスク装置２４以外の異常である場合（ステップＳａ４）には、ＣＰＵ２０は上述したステップＳａ１２以下の処理を実行する。

【００２９】上述したようにカラオケ端末３は、ハードディスク装置２４にサービスプログラムを記憶しているので、サービスプログラムをＲＯＭに記憶した従来装置と比較して、サービスプログラムを記憶するエリアを大きくすることが可能である。つまり、大容量のサービスプログラムを記憶させることも可能となる。しかし、ＲＯＭ等と比較して故障等が発生する可能性が高いハードディスク装置２４にサービスプログラムを記憶させた場合、ハードディスク装置２４のデータが破壊されるなどの異常が発生することも考えられる。この点を考慮して、このカラオケ端末３では、ハードディスク装置２４に関するサービスプログラムはＲＯＭ２２に記憶させている。これにより、ハードディスク装置２４のデータが破壊された場合にも、上述したようにハードディスク装置２４の復旧処理を行うことができる。ハードディスク装置２４を復旧した後には、ハードディスク装置２４に記憶されたサービスプログラムを実行することが可能となり、ハードディスク装置２４以外の故障に対しても修復等の処理を行うことができる。

【００３０】なお、上述したカラオケ端末３における異常時の復旧処理は、使用者が操作部２６を操作することにより、図４に示すフローチャートにしたがって、初期

化プログラムＰ１、ＨＤＤ検査プログラムＰ２、故障診断プログラムＰ３、修復プログラムＰ４などをそれぞれ実行させるようにしてもよいし、ＲＯＭ２２に上述したような復旧処理をＣＰＵ２０に実行させる復旧処理プログラムを記憶させておき、異常が発生した場合には、この復旧処理プログラムにしたがって上述した復旧処理がなされるようにしてもよい。

【００３１】また、カラオケ端末３に異常が発生していない場合にも、使用者が操作部２６を操作することにより、初期化プログラムＰ１、ＨＤＤ検査プログラムＰ２、故障診断プログラムＰ３および修復プログラムＰ４などをＣＰＵ２０に実行させることも可能である。

【００３２】Ｄ．変形例

上述した実施形態におけるＲＯＭ２２の代わりに書き換え可能なフラッシュメモリを用いるようにしてもよい。このようにすれば、フラッシュメモリに記憶されたハードディスク装置２４に関するサービスプログラムを書き換えることが可能となる。これにより、センタ１からハードディスク装置２４に関するサービスプログラムデータをカラオケ端末３に配信すれば、フラッシュメモリに記憶されたサービスプログラムが更新されるので、サービスプログラムの更新にかかる手間やコスト低減することできる。

【００３３】

【発明の効果】以上説明したように、本発明によれば、磁気記憶手段に記憶されたサービスプログラムを書き換えることにより、サービスプログラムを更新することができるため、故障診断や修復などを処理手段に実行させるサービスプログラムの更新にかかる手間やコストを低減することが可能である。また、磁気記憶手段にサービスプログラムを記憶しているので、大容量のサービスプログラムを記憶することが可能である。

【図面の簡単な説明】

【図１】　本発明の一実施形態に係る通信システムの構成を示す図である。

【図２】　前記通信システムにおけるカラオケ端末の構成を示すブロック図である。

【図３】　前記カラオケ端末の構成要素であるＲＯＭの内部構成を示す図である。

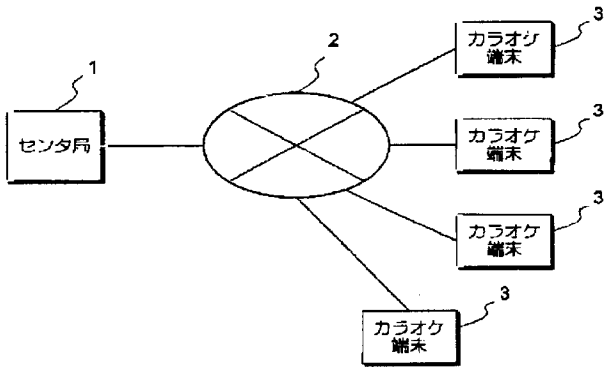
【図４】　前記カラオケ端末の構成要素であるハードディスク装置の内部構成を示すブロック図である。

【図５】　前記カラオケ端末に異常が発生した場合の、復旧処理の一例を示すフローチャートである。

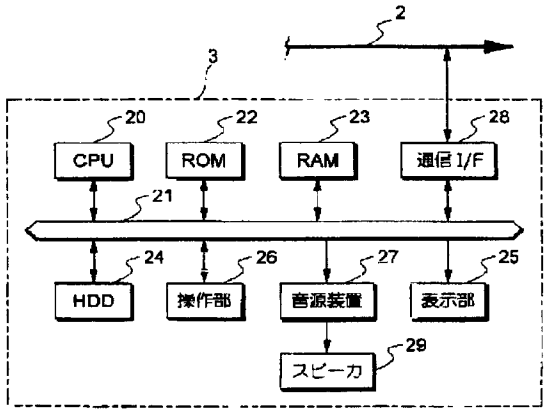
【符号の説明】

１…センタ（データ送信装置）、２…公衆回線網（通信網）、３…カラオケ端末（通信端末）、２０…ＣＰＵ（処理手段、書込手段）、２１…バス、２２…ＲＯＭ（不揮発性メモリ）、２３…ＲＡＭ、２４…ハードディスク装置、２４ａ…アプリケーション記憶エリア（第１の領域）、２４ｃ…サービス記憶エリア（第２の領域）、２５…表示部、２６…操作部（入力手段）、２７…音源装置、２８…通信インターフェース、２９…スピーカ

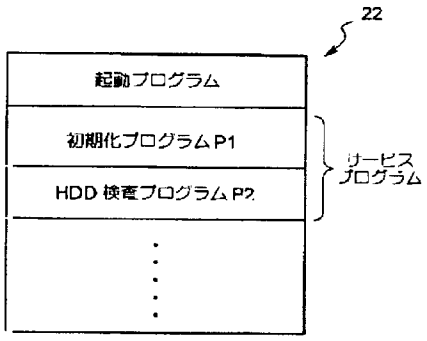
【図１】



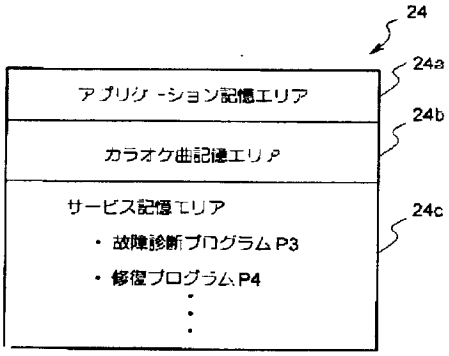
【図２】



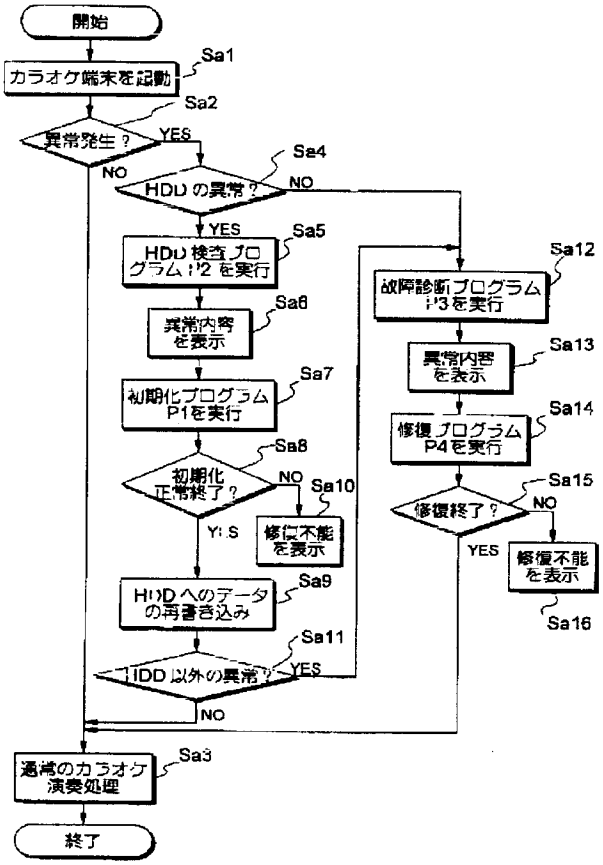
【図3】


22
起動プログラム
初期化プログラムP1
HDD検査プログラムP2
サービスプログラム

【図4】


24
24a
アプリケーション記憶エリア
24b
カラオケ曲記憶エリア
24c
サービス記憶エリア
・故障診断プログラムP3
・修復プログラムP4

【図5】


開始
Sa1
カラオケ端末を起動
Sa2
異常発生？
YES
NO
Sa4
HDDの異常？
NO
YES
Sa5
HDD検査プログラムP2を実行
Sa6
異常内容を表示
Sa7
初期化プログラムP1を実行
Sa8
初期化正常終了？
NO
Sa10
修復不能を表示
YES
Sa9
HDDへのデータの再書き込み
Sa11
HDD以外の異常？
YES
NO
Sa12
故障診断プログラムP3を実行
Sa13
異常内容を表示
Sa14
修復プログラムP4を実行
Sa15
修復終了？
NO
YES
修復不能を表示
Sa16
通常のカラオケ演奏処理
Sa3
終了

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(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
Kadoma-shi, Osaka-fu, 571 (JP)

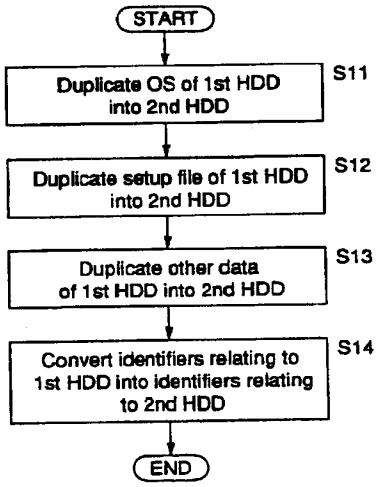
(72) Inventors:
- **Owada, Kiyoshi**
  Osakafu, Hirakatashi 573 (JP)
- **Kobayashi, Susumu**
  Osakafu, Osakashi, Asahiku, 535 (JP)

(74) Representative: **Kügele, Bernhard et al**
NOVAPAT INTERNATIONAL SA,
9, Rue du Valais
1202 Geneve (CH)

(54) Back-up unit

(57) A backup unit comprises a first storage means (10) containing at least one program (11) and a setup file (12) in which the operating environment of this program is written; a second storage means (20) used when the first storage means (10) has a fault; a duplication means (31) for duplicating the program (11) and the setup file (12) contained in the first storage means (10) into the second storage means (20); and an identifier conversion means (31) for converting identifiers included in the setup file (12) of the first storage means (10) and relating to the first storage means (10) into identifiers relating to the second storage means (20), when the duplication is performed. Therefore, when the operation of an information processor is stopped due to a fault in the first storage means (10), the second storage means (20) enables temporary operation of the information processor. In addition, it is possible to employ, as the second storage means (20), a recording medium that is lower in price and writing speed than the first storage means (10).

Fig.2



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Description

FIELD OF THE INVENTION

The present invention relates to a backup unit having a countermeasure against a fault in an external storage unit, such as a hard disk drive (hereinafter referred to as HDD).

BACKGROUND OF THE INVENTION

Since an operating system (hereinafter referred to as OS) for an information processor is contained in an external storage unit, such as an HDD, if the HDD itself or the content of the HDD is destroyed, the information processor cannot be started.

As a precaution against such an accident, a duplicate of the contents of the external storage unit is usually retained in a tape unit or the like. Such a duplicate is called a backup.

A description is given of a procedure for generating a backup with reference to figure 10. Initially, a tape unit for backup is mounted on an information processor equipped with an HDD (step S81). Then, data in the HDD is copied to backup tapes (step S82). In this method, two backup tapes are employed, i.e., a tape to which the OS of the HDD is copied and a tape to which user's data is copied. Hereinafter, the former is called an OS installation tape and the latter is called a user's data tape.

When the HDD has a fault after generation of the backup, a user executes a procedure shown in figure 11, as a countermeasure against the fault.

Initially, the user checks the extent of the fault (step S91). When the fault is destruction of data stored in the HDD, the user immediately sets the OS installation tape in a tape drive unit which is mounted on the information processor (step S93). When the HDD itself is destroyed physically, the user replaces the HDD with another one (step S92) and sets the OS installation tape (step S93). Thereafter, the user starts an OS installing tool from the OS installation tape (step S94), whereby the OS is installed in the HDD (step S95).

Further, the user resets the system of the information processor according to his work (step S96). Thereafter, the user sets the user's data tape (step S97) and restores the data from this tape into the HDD (step S98).

Another countermeasure against the fault in the external storage unit is to duplicate the external storage unit. More specifically, two external storage units having equal performances are prepared, and data of the same contents are written in both the external storage units simultaneously. In this case, even when one of the external storage units is out of order, the user can operate the information processor continuously using the other storage unit operating normally.

However, the conventional method employing the backup tapes have the following drawbacks.

Firstly, when the external storage unit is destroyed, since the external storage unit must be replaced with another one, the operation of the information processor is stopped until the replacement is completed.

Secondly, when the contents of the external storage unit are destroyed, after reinstallation of the OS, the user resets the system of the information processor according to his work, so that resetting of the present file is necessary. For the resetting, the operation of the information processor must be stopped for half a day.

On the other hand, the method of duplicating the external storage unit has the following drawback.

In this method, since data of the same contents are written simultaneously, two (first and second) external storage units having equal writing performances must be used. Hence, it is impossible to use an expensive and high-speed HDD as the first storage unit while using an inexpensive and low-speed optical disk for the second storage unit. Therefore, the cost of the external storage units is doubled according to the amount of data duplicated.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a backup unit equipped with first and second storage means, that enables temporary operation of an information processor using the second storage means when the first storage means is out of order, and that reduces the time during which the operation of the information processor is stopped.

It is another object of the present invention to provide a backup unit employing, for the second storage means, a storage unit having a writing speed lower than that of the first storage means.

It is a further object of the present invention to provide a backup unit that facilitates restoration of the contents of the first storage means from the contents of the second storage means.

Other objects and advantages of the invention will become apparent from the detailed description that follows. The detailed description and specific embodiments described are provided only for illustration since various additions and modifications within the scope of the invention will be apparent to those of skill in the art from the detailed description.

According to a first aspect of the present invention, a backup unit comprises a first storage means containing at least one program and a setup file in which the operating environment of this program is written; a second storage means used when the first storage means has a fault; a duplication means for duplicating the program and the setup file contained in the first storage means, into the second storage means; and an identifier conversion means for converting identifiers included in the setup file of the first storage means and relating to the first storage means, into identifiers relating to the second storage means, when the duplication is performed. Therefore, when the operation of an information

processor is stopped due to a fault in the first storage means, the second storage means enables temporary operation of the information processor. In addition, it is possible to employ, as the second storage means, a recording medium that is lower in price and writing speed than the first storage means.

According to a second aspect of the present invention, the above-mentioned backup unit further comprises a setup file managing means for judging whether at least one setup file contained in the first storage means has been updated. When the setup file managing means judges that the setup file has been updated, the duplication means duplicates the updated file of the first storage means, into the second storage means. Therefore, it is possible to store the latest setup file without troubling the user.

According to a third aspect of the present invention, the above-mentioned backup unit further comprises a switch means for selecting one of the first storage means and the second storage means as a storage means for booting. Therefore, when the operation of an information processor is stopped due to a fault in the first storage means, the second storage means enables temporary operation of the information processor without bothering the user with conversion of identifiers and other processes, so that the time during which the operation is stopped is reduced.

According to a fourth aspect of the present invention, the above-mentioned backup unit further comprises a fault detecting means for detecting a fault in the first storage means. When a fault is detected in the first storage means by the fault detecting means, the switch means selects the second storage means as a storage means for booting. Therefore, when the operation of an information processor is stopped due to a fault in the first storage means, the second storage means enables temporary operation of the information processor without troubling the user.

According to a fifth aspect of the present invention, in the above-mentioned backup unit, the program includes at least a program of an operating system, and the setup file includes at least a setup file of the operating system.

According to a sixth aspect of the present invention, the above-mentioned backup unit further comprises means for designating one of the first storage means and the second storage means as a source of duplication while designating the other as a target of duplication, and the duplication means duplicates the program and the setup file in the storage means designated as a source of duplication, into the storage means designated as a target of duplication. Therefore, data in the backup storage means can be restored in the other storage means. In addition, changes given to the data in the backup storage means during the temporary operation thereof are reflected in the restored data.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating an information processor employing a backup unit according to a first embodiment of the invention.

Figure 2 is a flowchart illustrating a procedure for generating a backup using the backup unit according to the first embodiment.

Figure 3 is a flowchart illustrating a procedure of a countermeasure against a fault in the backup unit according to the first embodiment.

Figures 4(a) and 4(b) are tables illustrating a setup file before conversion by the backup unit according to the first embodiment and a setup file after the conversion, respectively.

Figure 5 is a block diagram illustrating an information processor employing a backup unit according to a second embodiment of the invention.

Figure 6 is a flowchart illustrating a procedure for generating a backup using the backup unit according to the second embodiment.

Figure 7 is a flowchart illustrating a procedure for detecting a fault in the backup unit according to the second embodiment when the information processor is started.

Figure 8 is a flowchart illustrating a procedure of a countermeasure against a fault in the backup unit according to the second embodiment.

Figure 9 is a flowchart illustrating a procedure for updating backup data by the backup unit according to the second embodiment.

Figure 10 is a flowchart illustrating a procedure for generating a backup using a conventional backup unit.

Figure 11 is a flowchart illustrating a procedure of a countermeasure against a fault in the conventional backup unit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment 1]

Figure 1 is a block diagram illustrating an information processor employing a backup unit according to a first embodiment of the invention.

The backup unit comprises a first HDD 10 serving as a storage means when the information processor operates normally, a second HDD 20 serving as a storage means when the first HDD 10 is out of order, a central control unit 30 for instructing duplication of data and other processes, and an internal memory unit 50.

The first HDD 10 contains an OS 11 and a setup file 12 on the basis of the OS 11. The second HDD 20 contains an OS 21 which is a duplicate of the OS 11, a setup file 22 which is a duplicate of the setup file 12, and a setup file 23 which is obtained by converting the setup file 12.

The central control unit 30 comprises a duplication and conversion unit 31 for duplication of data, conver-

sion of data, and other processes, and a system loading switch unit 32 for selecting one of the HDD 10 and the HDD 20 as a storage unit for booting (i.e., starting).

The first HDD 10, the second HDD 20, the central control unit 30, and the internal memory unit 50 are connected with each other through an internal bus 60 and an external bus 70.

In the information processor equipped with the backup unit so constructed, when the first HDD 10 has a fault, the user takes a countermeasure against the fault, which will be described hereinafter using figures 2, 3, and 4(a) and 4(b). Figure 2 is a flowchart showing a procedure for generating a backup using the backup unit according to the first embodiment. Figure 3 is a flowchart showing a procedure of a countermeasure adopted by the user when the HDD 10 has a fault. Figure 4(a) shows an example of a setup file 12 before it is converted by the backup unit, and figure 4(b) shows an example of a setup file 23 after conversion.

First of all, a procedure for generating a backup against a fault in the HDD 10 will be described using figure 2.

The user instructs the duplication and conversion unit 31 to duplicate and convert the contents of the first HDD 10. Receiving the instruction, the duplication and conversion unit 31 duplicates the OS 11 to generate the OS 21 (step S11) and duplicates the setup file 12 to generate the setup file 22 (step S12). When the HDD 10 contains user's data, this data is also duplicated and stored in the HDD 20 (step S13).

Thereafter, as shown in figures 4(a) and 4(b), the duplication and conversion unit 31 converts a portion of data in the setup file 22 in the HDD 20, which portion is coded in device identifiers of the HDD 10, into data coded in device identifiers of the HDD 20, thereby generating the setup file 23 (step S14). After the conversion, the duplication and conversion unit 31 stores the setup file 23 in the HDD 20 to complete the backup.

In case where the information processor includes a third external storage unit (not shown), the setup file 12 includes device identifiers of the third storage unit, but these device identifiers are not converted.

Next, the process of user's countermeasure against the fault in the HDD 10 will be described using figure 3.

When the HDD 10 has a fault, the user changes the target of OS loading from the first HDD 10 to the second HDD 20 by the system loading switch unit 32 (step S21), and the user loads the OS 21 and the setup file 23 to boot the system from the second HDD 20 (step S22). Then, the user decides whether the HDD 10 should be recovered or not (step S23). When the decision is not to recover the HDD 10, the user operates the information processor temporarily using the second HDD until an HDD for replacement is prepared.

On the other hand, when the decision is to recover the HDD 10, the user judges the extent of the fault in the HDD 10 (step S24). When the HDD 10 is physically destroyed and another HDD for replacement is not available soon (step S30), the user operates the information processor temporarily using the second HDD until an HDD for replacement is prepared. When an HDD for replacement is available, the user stops the operation of the system (step S31) and replaces the first HDD 10 with the new HDD (step S32). Then, the user returns to step S21.

When the fault is destruction of data in the HDD 10, the user restores the contents of the HDD 10. In this case, it is necessary to restore the contents of the HDD 20 into the HDD 10. Hereinafter, a procedure of regenerating the first HDD 10 using the system booted for the temporary operation of the second HDD 20 will be described.

Initially, the user designates the second HDD 20 as a source of duplication and conversion and the first HDD 10 as a target of duplication and conversion. Then the user instructs the duplication and conversion unit 31 to duplicate the contents of the second HDD 20 into the first HDD 10. Receiving the instruction, the duplication and conversion unit 31 duplicates the OS 21 to generate the OS 11 (step S25) and duplicates the setup file 22 to generate the setup file 12 (step S26). When the HDD 20 contains user's data, this data is also duplicated and stored in the HDD 10 (step S27). Finally, the target of OS loading is returned to the first HDD 10 by the system loading switch unit 32 (step S28).

In the above-mentioned backup unit, the HDD 10 (first storage means) contains at least one program and a setup file in which an operating environment of this program is written. The duplication and conversion unit 31 (duplication means) duplicates the program and the setup file of the first HDD 10 into the second HDD 20 (second storage means). When the setup file is duplicated, if the setup file includes identifiers relating to the first HDD 10, the duplication and conversion unit 31 (identifier conversion means) converts these identifiers to identifiers relating to the second HDD 20. Further, the system loading switch unit 32 (switch means) selects the second HDD 20 as a storage unit for booting and boots the system from the second HDD 20. Therefore, it is possible for the user to operate the information processor temporarily, so that the inoperable time of the information processor can be reduced.

Furthermore, the duplication and conversion unit 31 (designation means) designates the second HDD 20 as a source of duplication and the first HDD 10 as a target of duplication, and duplicates the contents of the second HDD 20 into the first HDD 10. Therefore, the contents of the backup storage unit can be restored into the other storage unit. In addition, any changes to the data in the backup storage unit which has been temporarily operated will be reflected in the restored data.

[Embodiment 2]

Figure 5 is a block diagram illustrating an information processor employing a backup unit according to a second embodiment of the present invention.

The backup unit comprises an HDD 10 serving as a

first storage means when the information processor operates normally, a rewritable optical disk 40 serving as a second storage means when the first HDD 10 is out of order, a central control unit 30 for instructing duplication of data and other processes, and an internal memory unit 50.

The HDD 10 contains an OS 11 and a setup file 12 on the basis of the OS 11. The optical disk 40 contains an OS 41 which is a duplicate of the OS 11 and a setup file 42 which is a duplicate of the setup file 12.

The central control unit 30 comprises a duplication and conversion unit 31 for duplication of data, conversion of data, and other processes, a system loading switch unit 32 for selecting one of the HDD 10 and the optical disk 40 as a storage unit for booting, a setup file correction detector 33, and an HDD fault detector 34.

The HDD 10, the optical disk 40, the central control unit 30, and the internal memory unit 50 are connected with each other through an internal bus 60 and an external bus 70.

In the information processor equipped with the backup unit so constructed, when the HDD 10 has a fault, the user takes a countermeasure against the fault, which will be described hereinafter using figures 6 through 8. Figure 6 is a flowchart showing a procedure for generating a backup using the backup unit according to the second embodiment. Figure 7 is a flowchart showing the operation of the HDD fault detector 34 when the information processor is started. Figure 8 is a flowchart showing a procedure of a countermeasure against HDD fault. Figure 9 is a flowchart showing a procedure for updating a backup.

First of all, a procedure for generating a backup against HDD fault will be described using figure 6.

The user mounts the rewritable optical disk 40 as a second storage means (step S41) and instructs the duplication and conversion unit 31 to duplicate and convert the contents of the HDD 10. Receiving the instruction, the duplication and conversion unit 31 duplicates the OS 11 to generate an OS 41 (step S42). Subsequently, the unit 31 generates a setup file 42 by converting a portion of data in the setup file 12, which portion is coded in device identifiers of the HDD 10, into data coded in device identifiers of the optical disk 40, and stores the setup file 42 in the optical disk 40 (step S43). In this second embodiment, in order to save the storage region of the optical disk 40, duplication of the setup file 12 is not performed. When the HDD 10 contains user's data, this data is also duplicated and stored in the optical disk 40 (step S44).

Next, the operation of the HDD fault detector 34 will be described using figure 7.

When the information processor is started, the HDD fault detector 34 judges whether the HDD 10 has a fault or not by detecting, for example, "reading or writing error" of the HDD 10 or "access time out" to the HDD 10 (step S45). When the HDD 10 has no fault, the information processor is started by the HDD 10 (step S47). On the other hand, when the HDD 10 has a fault, the HDD fault detector 34 instructs the system loading switch unit 32 to change the target of OS loading from the HDD 10 to the optical disk 40 (step S46). The system loading switch unit 32 loads the OS 41 and the setup file 42 to boot the system from the optical disk 40 (step S48). Thereafter, the information processor is operated temporarily by the optical disk 40 until the HDD 10 is replaced with another HDD.

After the detection of the HDD fault, the user takes a countermeasure against the fault, which will be described hereinafter using figure 8.

When a fault is detected in the HDD 10, the user changes the target of OS loading from the HDD 10 to the optical disk 40 by the system loading switch unit 32 (step S61), and the user loads the OS 41 and the setup file 42 to boot the system from the optical disk 40 (step S62). Then, the user decides whether the HDD 10 should be recovered or not (step S63). When the decision is not to recover the HDD 10, the user operates the information processor temporarily using the optical disk 40 until an HDD for replacement is prepared.

On the other hand, when the decision is to recover the HDD 10, the user judges the extent of the fault (step S64). When the HDD 10 is physically destroyed and an HDD for replacement is not available soon (step S69), the user operates the information processor temporarily using the optical disk 40 until an HDD for replacement is prepared. If an HDD for replacement is available, the user stops the operation of the system (step S70) and replaces the HDD 10 with the new HDD (step S71). Then, the user returns to step S61.

When the fault is destruction of data in the HDD 10, the user restores the contents of the HDD 10. In this case, it is necessary to restore the contents of the optical disk 40 into the HDD 10. Hereinafter, a procedure of regenerating the first HDD 10 using the system booted for the temporary operation of the optical disk 40 will be described.

Initially, the user designates the optical disk 40 as a source of duplication and conversion and the HDD 10 as a target of duplication and conversion. Then, the user instructs the duplication and conversion unit 31 to duplicate and convert the contents of the optical disk 40 into the HDD 10. Receiving the instruction, the duplication and conversion unit 31 duplicates the OS 41 to generate the OS 11 (step S65) and duplicates the setup file 42 to generate the setup file 12 (step S66). At this time, the duplication and conversion unit 31 converts a portion of data in the setup file 12, which portion is coded in device identifiers of the optical disk 40, into data coded in device identifiers of the HDD 10 (step S67). When the optical disk 40 contains user's data, this data is also duplicated and stored in the HDD 10. To complete the processing, the system loading switch unit 32 returns the target of OS loading to the HDD 10 (step S68).

When data in the HDD 10 is updated, backup data corresponding to the updated, i.e., latest, data must be stored in the optical disk 40. Hereinafter, a procedure for updating backup data will be described using figure 9.

When the user corrects the setup file 12 in the HDD 10 during operation of the information processor, the setup file correction detector 33 detects the correction of the setup file 12 by, for example, comparing the change time of the setup file 12 with the generation time of the setup file 42 (step S51). In the case where the correction of the setup file 12 is done after the backup, the duplication and conversion unit 31 duplicates the setup file 12 in the HDD 10 into the setup file 42 in the optical disk 40 while converting identifiers relating to the HDD to identifiers relating to the optical disk (step S52), whereby the setup file 42 is updated. On the other hand, in the case where the correction of the setup file 12 is done before the backup, the setup file 12 is not updated.

As described above, according to the second embodiment of the invention, the HDD 10 (first storage means) contains at least one program and a setup file in which an operating environment of this program is written. The duplication and conversion unit 31 (duplication means) duplicates the program and the setup file of the HDD 10 into the optical disk 40 (second storage means). When the setup file includes identifiers relating to the HDD 10, the duplication and conversion unit 31 (identifier conversion means) converts these identifiers to identifiers relating to the optical disk 40. Therefore, it is possible to employ, as the second storage means, a recording medium that is lower in price and writing speed than the first storage means.

Further, when the HDD fault detector 34 (fault detecting means) detects a fault in the HDD 10, the system loading switch unit 32 (switch means) loads the OS 41 and the setup file 42 from the optical disk 40 to boot the system. Therefore, even when the operation of the information processor is stopped due to the HDD fault, the optical disk 40 enables temporary operation of the information processor without bothering the user with conversion of identifiers and other processes.

Furthermore, the setup file correction detector 33 (setup file managing means) checks whether or not the setup file in the HDD 10 is updated and, when it is updated, the updated file is duplicated in the optical disk 40. Therefore, it is possible to store the setup file 42 corresponding to the latest setup file 12, without troubling the user. In addition, when the user restores the HDD 10 using the system of the optical disk 40, which system is booted for the temporary operation, since changes given to the setup file 42 by the user during the temporary operation are reflected in the setup file 12 as latest data, the HDD 10 can be regenerated with no necessity of changing the setup file 12.

The backup unit of the present invention is not restricted to those described for the first and second embodiments. Although in the first and second embodiments an HDD or an optical disk is used as the second external storage unit, a floppy disk or a rewritable ROM, such as an EEPROM or a flash ROM, may be used with the same effects as mentioned above.

In the first and second embodiments of the invention, the duplication and conversion unit 31, the system loading switch unit 32, the setup file correction detector 33, and the HDD fault detector 34 are implemented by software, i.e., programs loaded to the central control unit 30. However, these constituents may be implemented by hardware. Further, when these constituents are implemented by software, their programs may be stored in the HDD 10. In addition, a program for generating the system loading switch unit 32 may be stored in a ROM in the information processor.

Claims

1. A backup unit (Fig.1) comprising:

   a first storage means (10) containing at least one program (11) and a setup file (12) in which the operating environment of this program (11) is written;
   a second storage means (20) used when the first storage means (10) has a fault;
   a duplication means (31) for duplicating the program (11) and the setup file (12) contained in the first storage means (10) into the second storage means (20); and
   an identifier conversion means (31) for converting identifiers included in the setup file (12) of the first storage means (10) and relating to the first storage means (10), into identifiers relating to the second storage means (20), when the duplication is performed.

2. A backup unit as defined in claim 1 (Fig.5) comprising:

   a setup file managing means (33) for judging whether at least one setup file (12) contained in the first storage means (10) has been updated;
   wherein, when the setup file managing means (33) judges that the setup file (12) has been updated, the duplication means (31) duplicates the updated file (12) of the first storage means (10) into the second storage means (40).

3. A backup unit as defined in claim 1 comprising a switch means (32) for selecting one of the first storage means (10) and the second storage means (40) as a storage means for booting.

4. A backup unit as defined in claim 3 comprising:

   a fault detecting means (34) for detecting a fault in the first storage means (10);
   wherein, when a fault is detected in the first storage means (10) by the fault detecting means (34), the switch means (32) selects the second storage means (40) as a storage means for booting.

5. A backup unit as defined in any of claims 1 to 4

wherein the program (11) includes at least a program of an operating system, and the setup file (12) includes at least a setup file of the operating system.

6. A backup unit as defined in claim 1 comprising:

means (31) for designating one of the first storage means (10) and the second storage means (40) as a source of duplication while designating the other as a target of duplication;
wherein said duplication means (31) duplicates the program (11 or 41) and the setup file (12 or 42) in the storage means (10 or 40) designated as a source of duplication, into the storage means (10 or 40) designated as a target of duplication.

Fig.1

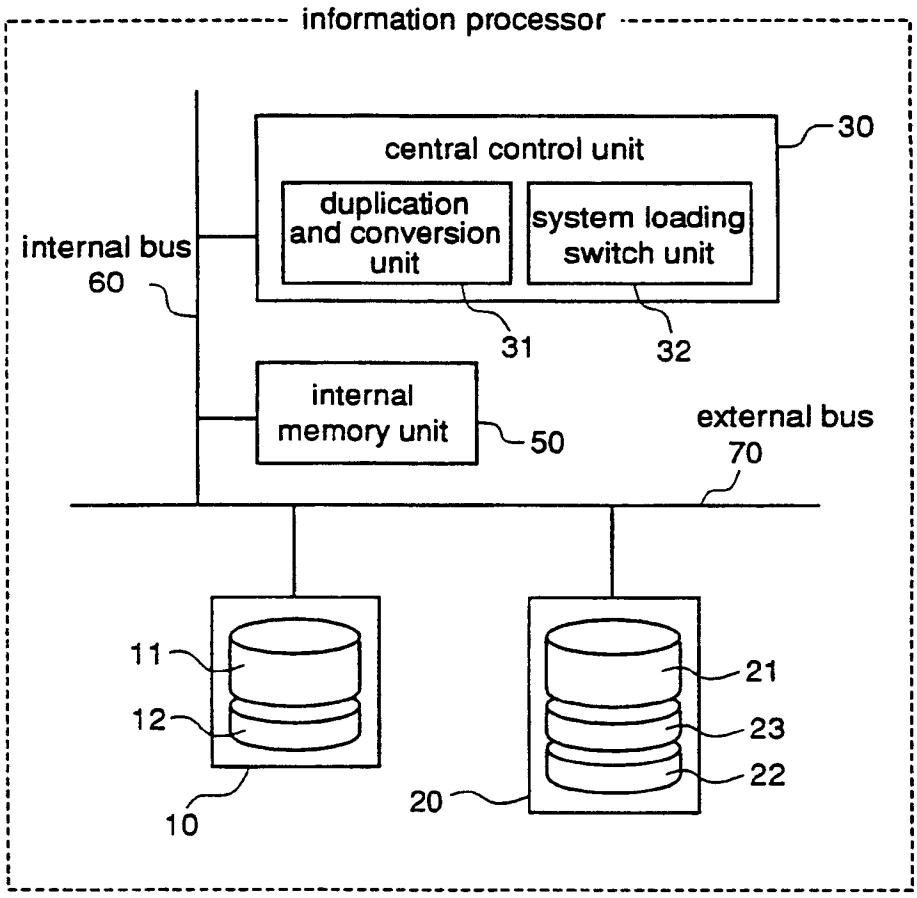


Fig.2

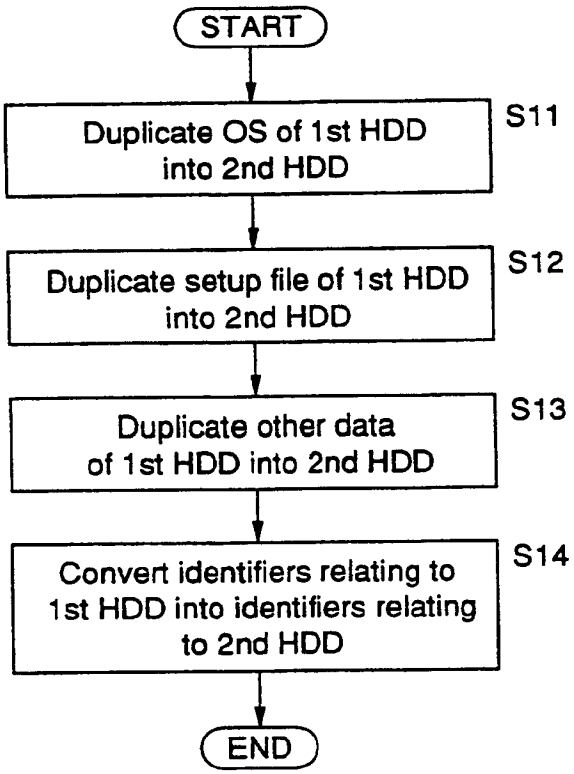


Fig.3

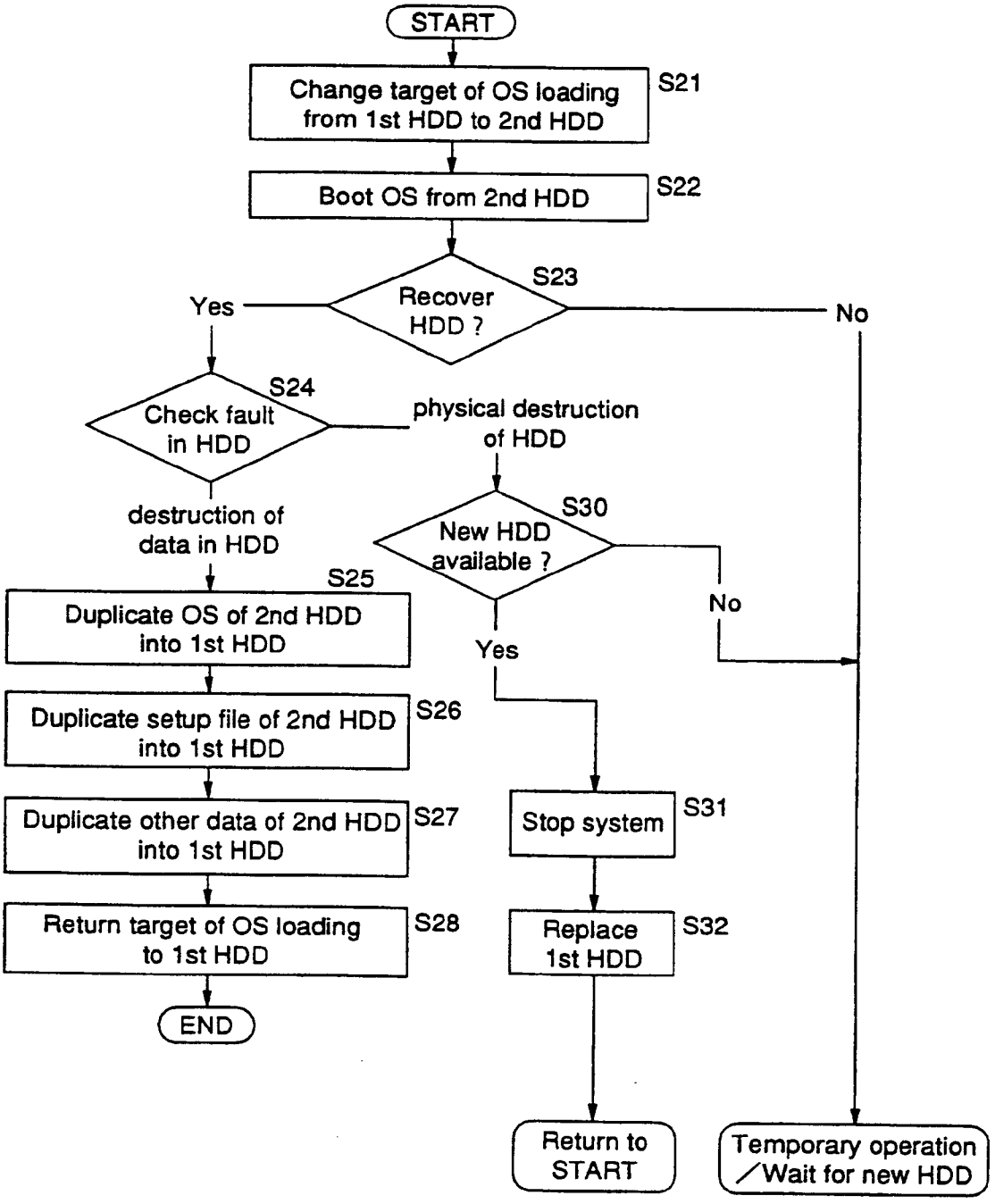


Fig.4 (a)

setup file before conversion :

setup file for mounting HDD

identifiers relating to first external storage unit

# device	device	mount	FS	fsck	mount	mount
# to mount	to fsck	point	type	pass	at boot	options
#						
/dev/dsk/c0t1d0s0	/dev/rdsk/c0t1d0s0	/	ufs	1	no	—
/dev/dsk/c0t1d0s6	/dev/rdsk/c0t1d0s6	/usr	ufs	1	no	—
/dev/dsk/c0t1d0s7	/dev/rdsk/c0t1d0s7	/export/home	ufs	2	yes	—
/dev/dsk/c0t1d0s1	—	—	swap	—	no	—
/dev/dsk/c0t5d0s2	/dev/rdsk/c0t5d0s2	/data1	ufs	1	yes	—

identifiers relating to third external storage unit

Fig.4 (b)

setup file after conversion :

identifiers relating to second external storage unit (converted)

# device	device	mount	FS	fsck	mount	mount
# to mount	to fsck	point	type	pass	at boot	options
#						
/dev/dsk/c0t2d0s0	/dev/rdsk/c0t2d0s0	/	ufs	1	no	—
/dev/dsk/c0t2d0s6	/dev/rdsk/c0t2d0s6	/usr	ufs	1	no	—
/dev/dsk/c0t2d0s7	/dev/rdsk/c0t2d0s7	/export/home	ufs	2	yes	—
/dev/dsk/c0t2d0s1	—	—	swap	—	no	—
/dev/dsk/c0t5d0s2	/dev/rdsk/c0t5d0s2	/data1	ufs	1	yes	—

identifiers relating to third external storage unit (not converted)

Fig.5

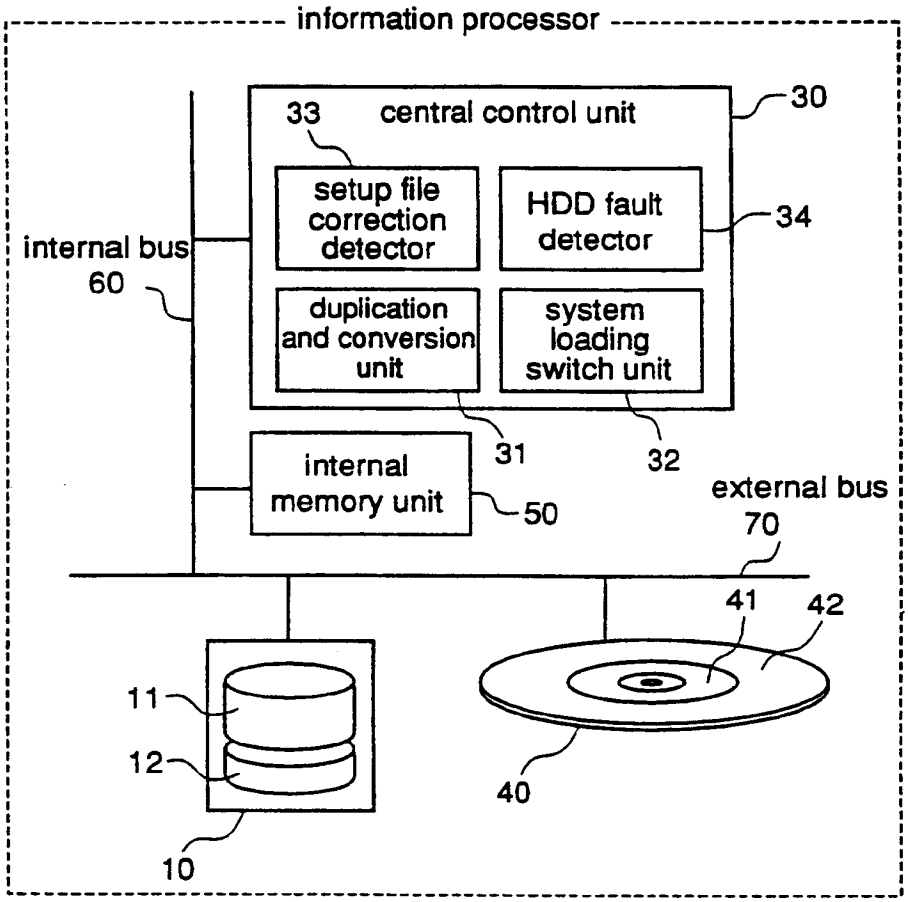


Fig.6

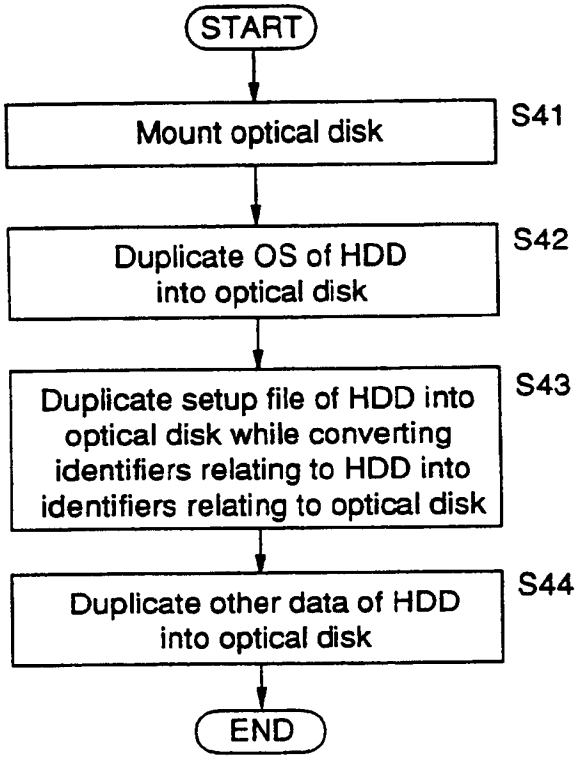


Fig.7

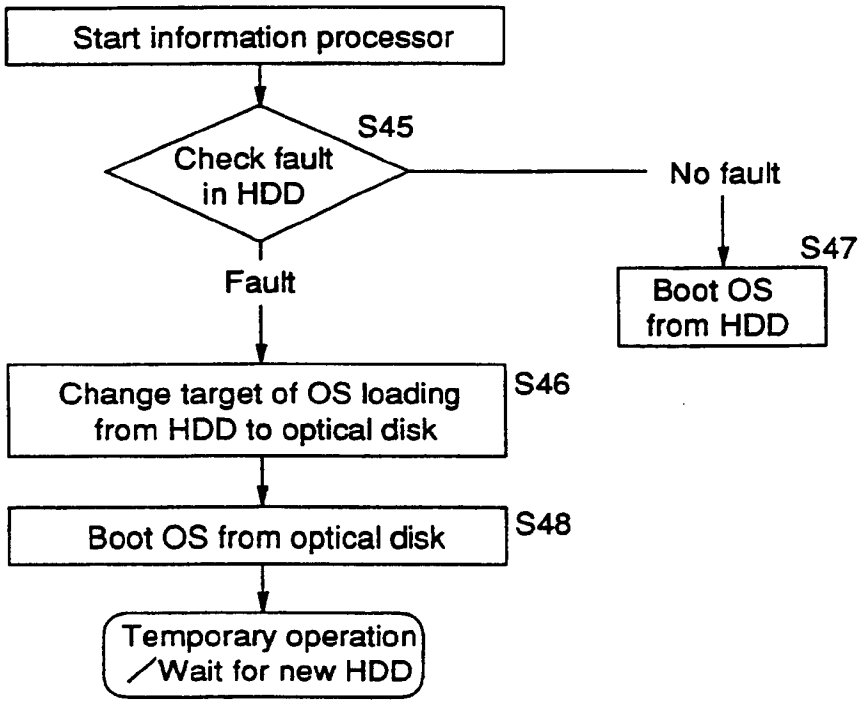


Fig.8

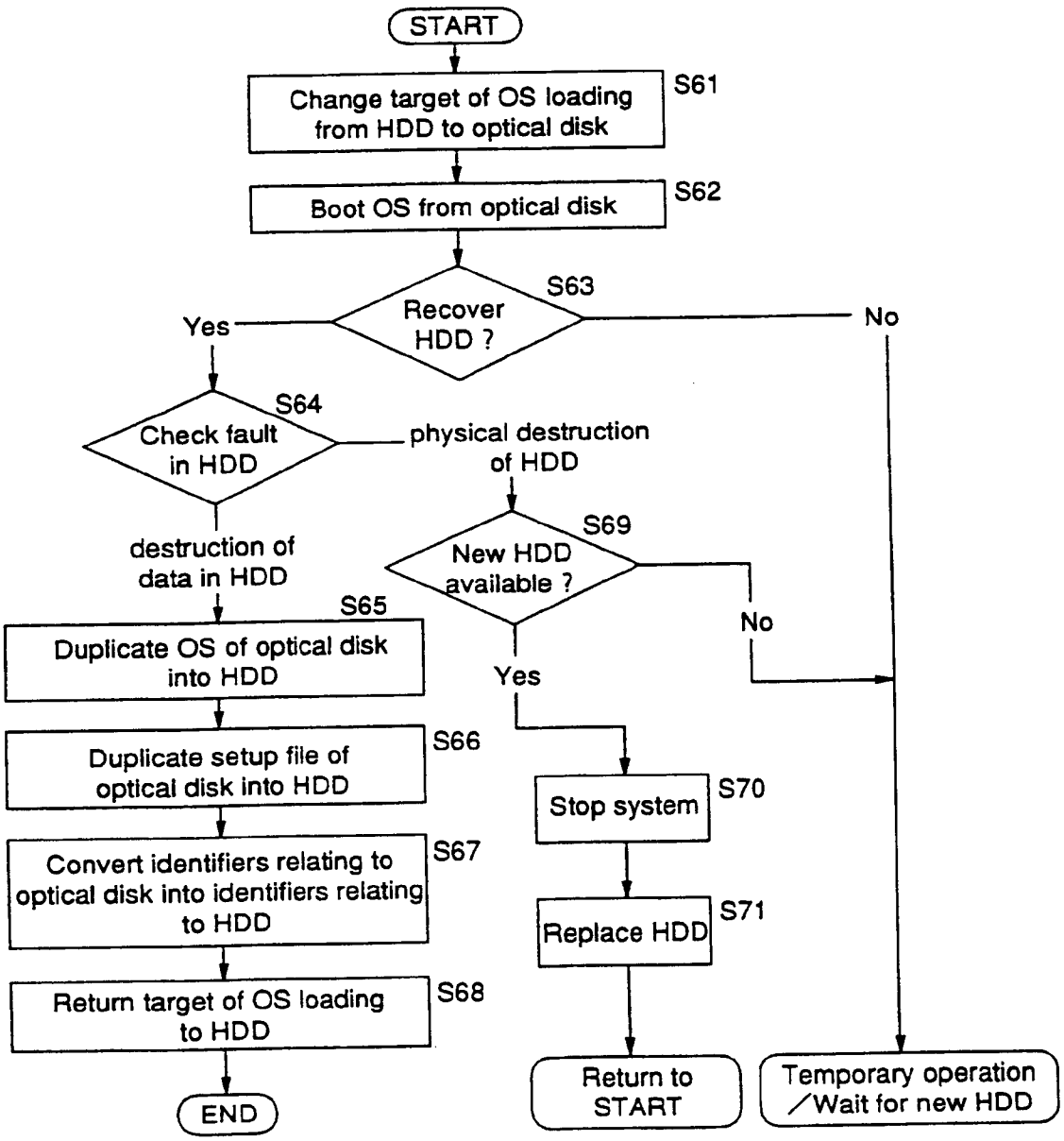


Fig.9

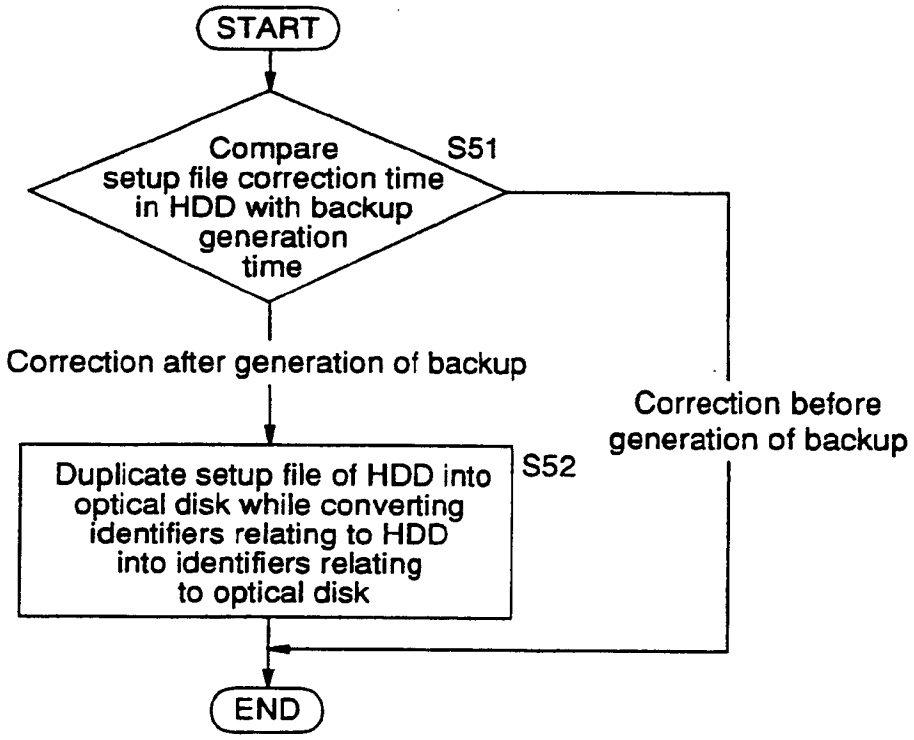


Fig.10 Prior Art

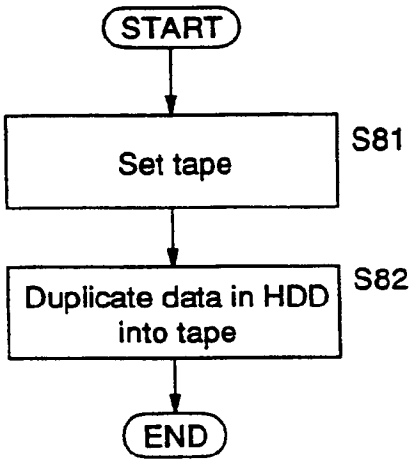
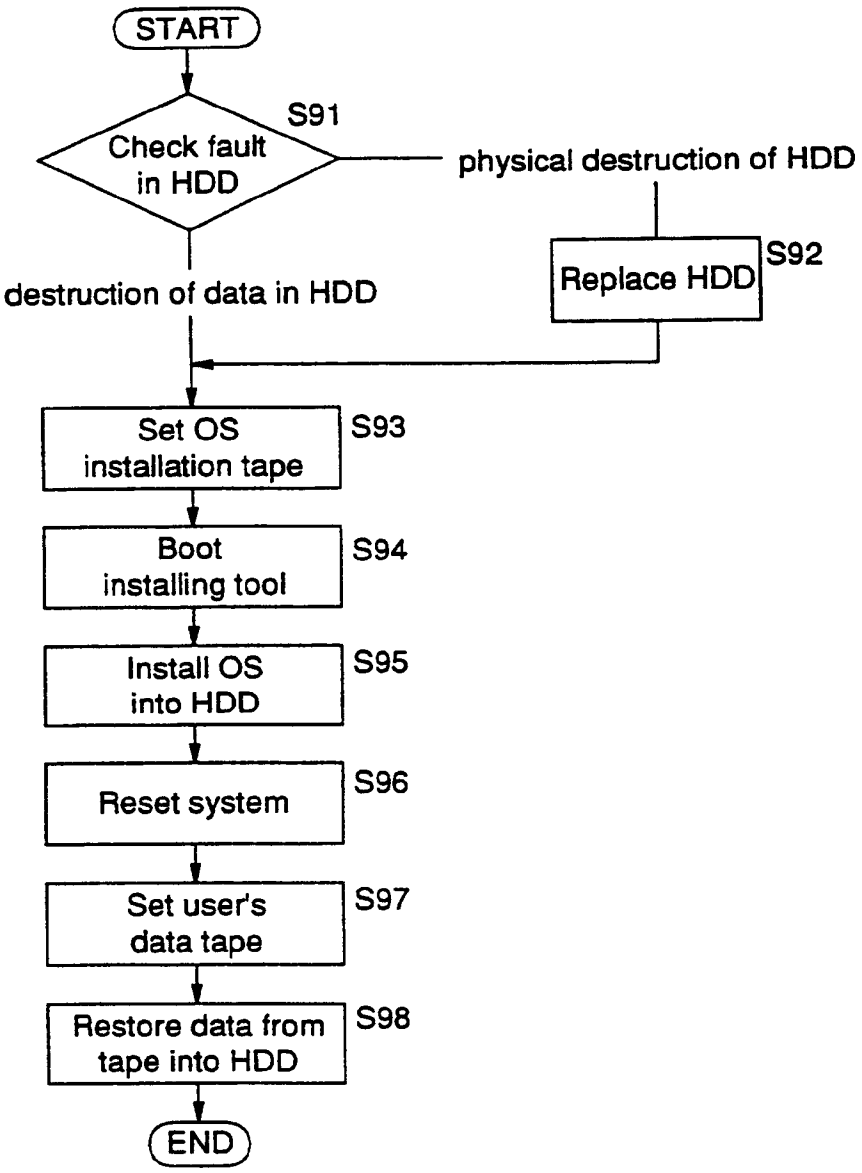


Fig.11 Prior Art



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 11 8255

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 37, no. 7, 1 July 1994, page 5/6 XP000455419 "AUTOMATIC IPL DRIVE SWITCH" * the whole document * ---	1,3,4,6	G06F11/20 G06F11/14
A	EP 0 586 907 A (ROLAND MAN DRUCKMASCH) 16 March 1994 * column 3, line 19 - line 36 * * column 4, line 41 - column 6, line 7 * ---	1,3,4,6	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 36, no. 10, 1 October 1993, page 329/330 XP000412279 "METHOD TO RECOVER FROM FAILED BOOT DRIVE USING DISKETTES" * the whole document * ---	1,4	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 37, no. 10, 1 October 1994, pages 5-8, XP000475557 "INITIAL MICROCODE LOAD OVERLAY EXECUTION FOR PERSONAL COMPUTERS" * page 7, line 8 - line 14 * * page 8, line 1 - line 6 * * figure 7 * -----	1,5	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	21 February 1997	Masche, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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(71) Applicant: **CANON KABUSHIKI KAISHA**
Tokyo (JP)

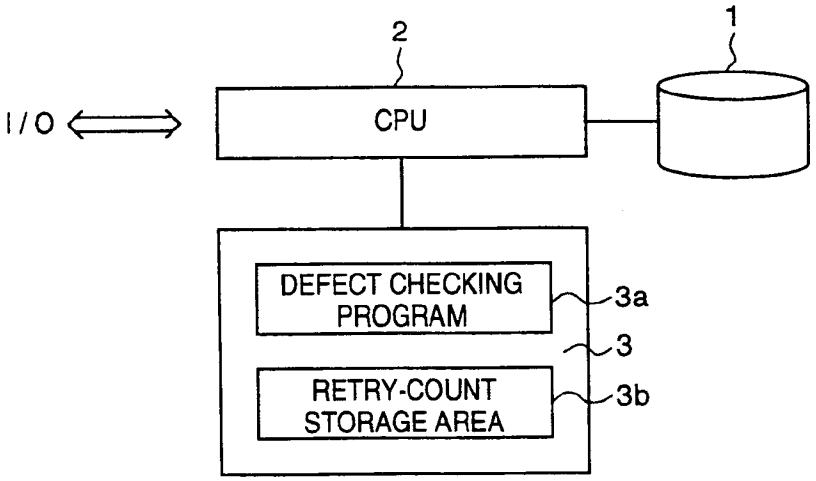
(72) Inventor: **Inoue, Sunao**
Ohta-ku, Tokyo (JP)

(74) Representative:
Beresford, Keith Denis Lewis et al
BERESFORD & Co.
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

(54) Storage device, method of controlling same, storage system and method of controlling same

(57) All storage areas constituting a storage medium 1 are checked for defects by successively reading and writing data. If an error that has occurred owing to the checking operation is an error for which retry is possible, the number of times this occurs is accumulated in a retrial-count storage area 36 of a memory. A faulty storage area is detected based upon the type of error that has occurred by checking or the number of occurrences that have been accumulated.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

This invention relates to a storage device equipped with a storage medium, a method of controlling the device, a storage system and a method of controlling the storage system.

In a magnetic storage device accommodating a storage medium such as a hard disk, it is usual for the storage medium to have defective storage areas that do not implement the storage function. To deal with a storage area having such a defect, substitution processing is executed. In substitution processing, a substitute storage area is prepared and is substituted for the defective storage area. In addition to substitution processing set when the product is shipped, substitution processing can be performed also with regard to defects that occur afresh during use of the device.

Substitution processing according to the prior art will be described with reference to Fig. 7.

Shown in Fig. 7 are a storage device 71 having ordinary storage areas 72 and substitute storage areas 73 set aside in order that substitution processing may be executed if some of the ordinary storage areas 72 develop defects. Shown at 74 is a substitute-area management area (referred to as a "defect list" or the like) for storing information indicating which areas have defects and which of the substitute storage areas 73 have been substituted for them.

Defective areas are of two types, namely a defective area 75 which existed from the outset at shipping of the storage device 71 from the factory, and a defective area 76 which developed subsequently during use of the device. When each of these areas is subjected to substitution processing, the defective area is replaced by a substitute storage area and information relating to the substitution is stored in the substitute-area management area 74.

By way of example, Japanese Patent Application Laid-Open (KOKAI) No. 4-266117 describes a storage device in which the storage areas of the storage device are monitored to determine, at reading or writing of data, the number of reading/writing retries and occurrence of errors per each storage area. By recording the number of read/write retries associated with each storage area of the storage device, storage areas deemed to be likely to fail or storage areas in which defects have occurred during use can be replaced by substitute storage areas automatically.

However, with the conventional storage device of this kind, substitution processing for dealing with defects that have occurred anew during use of the device is executed in response to an instruction from the user.

Further, as described in Japanese Patent Application Laid-Open No. 4-266117, the detection and prediction of the occurrence of defects is limited to storage areas actually accessed. More specifically, the detection and prediction of defects in storage areas is not carried out with regard to storage areas currently vacant and unused but to which data are likely to be written in the future or with regard to storage areas in which data exist but which will not be read or written for an extended period of time.

Another problem is that satisfactory detection and prediction of the occurrence of defects cannot be carried out because such detection and prediction is performed only when a read instruction or write instruction is implemented as an actual accessing operation.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a storage device, a method of controlling the same and a storage system in which the detection and prediction of the occurrence of defects in all storage areas of the storage device can be performed accurately and automatically, and in which a storage area that has become defective can be replaced by another storage area automatically.

A further object of the present invention is to provide a storage device, a method of controlling the same and a storage system in which accessing as by an ordinary read instruction or write instruction can be executed while detection and prediction of the occurrence of defects in storage areas is carried out.

According to the present invention, the foregoing objects are attained by providing a storage device equipped with a storage medium, comprising checking means for checking for defects in storage areas by performing reading and writing of data over all storages areas constituting the storage medium, accumulating means which, when an error that has occurred by checking performed by the checking means is an error for which retry is possible, is for accumulating the number of times this has occurred, and detecting means for detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed by the checking means or the number of occurrences accumulated by the accumulating means.

In a preferred embodiment, the device further comprises substitution means for substituting another storage area for a storage area having a defect detected by the detecting means. Providing the substitution means makes it unnecessary for the substitution to be performed by the user.

In a preferred embodiment, the detecting means detects a storage area under examination as being a defective location if the number of occurrences accumulated by the accumulating means exceeds a predetermined number or if the error that has occurred by checking performed by the checking means is an error for which retry is impossible.

In a preferred embodiment, the storage device has a control instruction for checking for defects in storage areas by performing control in such a manner that in-

structions from elsewhere are not accepted during execution of checking by the checking means, wherein the checking means checks for defects in the storage areas using this control instruction. By employing this control instruction, storage areas other than storage areas being checked are capable of accepting instructions from elsewhere.

In a preferred embodiment, the storage device further comprises holding means for holding data read out by the checking means, wherein the checking means checks for defects of the storage areas by re-reading data out of a storage area after it has been checked by the checking means and comparing the read data and the data held by the holding means. Adopting this arrangement makes it possible to improve the accuracy of the check performed by the checking means.

In a preferred embodiment, the check performed by the checking means is executed at predetermined times. According to the present invention, the foregoing objects are attained by providing a storage system equipped with a plurality of storage devices, comprising checking means for checking for defects in storage areas by performing reading and writing of data over all storages areas constituting a storage medium provided in each storage device of the plurality thereof, accumulating means which, when an error that has occurred by checking performed by the checking means is an error for which retry is possible, is for accumulating the number of times this has occurred, detecting means for detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed by the checking means or the number of occurrences accumulated by the accumulating means, monitoring means for monitoring status of detection of each storage device of the plurality thereof by the detecting means, and substitution means for substituting one storage device for another in dependence upon status of detection monitored by the monitoring means.

According to the present invention, the foregoing objects are attained by providing a method of controlling a storage device equipped with a storage medium, comprising a checking step of checking for defects in storage areas by performing reading and writing of data over all storages areas constituting the storage medium, an accumulating step which, when an error that has occurred by checking performed at the checking step is an error for which retry is possible, is a step of accumulating the number of times this has occurred, and a detecting step of detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed at the checking step or the number of occurrences accumulated at the accumulating step.

According to the present invention, the foregoing objects are attained by providing a method of controlling a storage system equipped with a plurality of storage devices, comprising a checking step of checking for defects in storage areas by performing reading and writing of data over all storages areas constituting a storage medium provided in each storage device of the plurality thereof, an accumulating step which, when an error that has occurred by checking performed at the checking step is an error for which retry is possible, is a step of accumulating the number of times this has occurred, a detecting step of detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed at the checking step or the number of occurrences accumulated at the accumulating step, a monitoring step of monitoring status of detection of each storage device of the plurality thereof at the detecting step, and a substitution step of substituting one storage device for another in dependence upon status of detection monitored at the monitoring step.

According to the present invention, the foregoing objects are attained by providing a computer readable memory storing program codes of control processing for controlling a storage device equipped with a storage medium, the memory comprising a program code of a checking step of checking for defects in storage areas by performing reading and writing of data over all storages areas constituting the storage medium, a program code of an accumulating step which, when an error that has occurred by checking performed at the checking step is an error for which retry is possible, is a step of accumulating the number of times this has occurred, and a program code of a detecting step of detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed at the checking step or the number of occurrences accumulated at the accumulating step.

Thus, in accordance with the present invention, as described above, it is possible to provide a storage device, a method of controlling the same and a storage system in which the detection and prediction of the occurrence of defects in all storage areas of the storage device can be performed accurately and automatically, and in which a storage area that has become defective can be substituted by another storage area automatically.

Further, it is possible to provide a storage device, a method of controlling the same and a storage system in which accessing as by an ordinary read instruction or write instruction can be executed while detection and prediction of the occurrence of defects in storage areas is carried out.

Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

Fig. 1 is a block diagram illustrating a preferred system for implementing a storage device according to a first embodiment of the present invention;

Fig. 2 is a flowchart illustrating the flow of processing executed according to the first embodiment;

Fig. 3 is a flowchart illustrating the flow of processing executed according to a second embodiment of the invention;

Fig. 4 is a flowchart illustrating the flow of processing executed according to a third embodiment of the invention;

Fig. 5 is a flowchart illustrating the flow of processing executed in order to perform the processing described in connection with the second and third embodiments of the invention;

Fig. 6 is a diagram for describing processing executed according to a third embodiment of the invention;

Fig. 7 is a diagram showing the structure of the memory map of a floppy disk storing a program for processing according to the present invention; and

Fig. 8 is a diagram showing the structure of the memory map of a floppy disk storing a program for processing according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described in detail with reference to the drawings.

Fig. 1 is a block diagram illustrating a preferred system for implementing a storage device according to a first embodiment of the present invention.

Shown in Fig. 1 are a storage device 1 comprising a storage medium such as a hard disk, a CPU (central processing unit) 2 for subjecting the elements of the system to various control, and a memory 3. The memory 3 includes a defect checking program 3a for executing processing described in the first embodiment, and a retry-count storage area 3b. It is assumed that the detailed construction of the storage device 1 is similar to that of the storage device 71 shown in Fig. 7.

The processing executed in accordance with the first embodiment will now be described with reference to the flowchart of Fig. 2.

Fig. 2 is a flowchart illustrating the flow of processing executed according to the first embodiment. First, in outline, data stored in each of the plurality of storage areas of storage device 1 are read out of each area successively in response to a read instruction and occurrence of a defect in a storage area owing to the read instruction is detected or predicted. If a defect is detected, substitution processing is executed. Further, data read out of each area in response to the read instruction are written to each corresponding storage area successively in response to a write instruction, and occurrence of a defect in a storage area owing to the write instruction is detected or predicted. If a defect is detected, substitution processing is executed.

Further, the number of retries for reading storage areas of the storage device 1 in response to the read instruction is stored and, if the number of retries in regard to a storage area exceeds a predetermined threshold value, this storage area is subjected to substitution processing. A similar operation is performed with regard to the write instruction as well.

It should be noted that each of the plurality of storage areas is assigned a number for distinguishing the storage area. Detection and prediction of the occurrence of a defect in each area is performed in the order of these numbers.

The details of the above-mentioned processing will now be described.

Step S201 in Fig. 2 calls for initialization, to "1", of a counter "block", which counts the numbers of the storage areas that undergo defect detection and prediction. This is followed by step S202, at which it is determined whether all storage areas have undergone defect detection and prediction processing. If defect detection and prediction is finished for all storage areas ("YES" at step S202), then processing is terminated. If defect detection and prediction is not finished for all storage areas ("NO" at step S202), then the program proceeds to step S203.

Data stored in a storage area corresponding to content indicated by the counter "block" are read out by a read instruction (read block) at step S203. If data cannot be read out at the first operation, retry is carried out by the system. This is followed by step S204, at which it is determined whether the storage area for which the data read operation was performed in response to the read instruction has developed an unrecoverable error (referred to as an "unrecoverable readout error") even when readout is retried. If such an error has occurred ("YES" at step S204), then the program proceeds to step S205, where substitution processing is executed. This is followed by step S206, at which error processing such as issuance of an error warning is executed. The program then returns to step S203, at which next storage area undergoes defect detection and prediction processing. It should be noted that the unrecoverable readout error is a fatal error in which data that have been stored in the storage area are lost.

If it is found at step S204 that an error has not occurred ("NO" at step S204), then the program proceeds to step S207. Here it is determined whether reading of this storage area in response to the read instruction is retried or not. If retry is carried out ("YES" at step S207), the program proceeds to step S208. If retry is not carried out ("NO" at step S207), then the program proceeds to step S211.

With regard to a storage area from which reading is retried in response to the read instruction, step S208 calls for incrementing of the content of an adding counter R[block] (block = n, where n is the nth storage area) which counts up the number of retries (retry count) in response to the read instruction. Next, at step S209, it

is determined whether the content of the adding counter R[block] is greater than a maximum retry count Rmax that has been set in advance. If the content of the adding counter R[block] is greater than the maximum retry count Rmax ("YES" at step S209), then the program proceeds to step S210, at which this storage area undergoes substitution processing. If the content of the adding counter R[block] is equal to or less than the maximum retry count Rmax ("NO" at step S209), on the other hand, then the program proceeds to step S211.

The data that have been read out by the read instruction at step S203 are written to the corresponding storage area at step S211 in response to a write instruction (write block). This is followed by step S212, at which it is determined whether the storage area for which the data write operation was performed in response to the write instruction has developed an unrecoverable error (referred to as an "unrecoverable write error") even when writing is retried. If such an error has occurred ("YES" at step S212), then the program proceeds to step S216, where substitution processing is executed. If an error has not occurred ("NO" at step S212), on the other hand, then the program proceeds to step S213.

It is determined at step S213 whether writing of this storage area in response to the write instruction is to be retried or not. In case of retry ("YES" at step S213), the program proceeds to step S214. If retry is not to be carried out ("NO" at step S213), then the program proceeds to step S217.

With regard to a storage area from which writing is to be retried in response to the write instruction, step S214 calls for incrementing of the content of an adding counter W[block] (block = n, where n is the nth storage area) which counts up the number of retries (retry count) in response to the write instruction. Next, at step S215, it is determined whether the content of the adding counter W[block] is greater than a maximum retry count Wmax that has been set in advance. If the content of the adding counter W[block] is greater than the maximum retry count Wmax ("YES" at step S215), then the program proceeds to step S216, at which this storage area undergoes substitution processing. If the content of the adding counter W[block] is equal to or less than the maximum retry count Wmax ("NO" at step S215), on the other than, then the program proceeds to step S217.

The content of the counter "block" is incremented at step S217, whence the program returns to step S202. The processing described in connection with steps S202 ~ S217 is repeated until detection and prediction of occurrence of defects is finished for storage areas. When all storage areas have been subjected to detection and prediction of defect occurrence, processing is terminated.

The content of the adding counter R[block] and W [block] may be stored in the retry-count storage area of the memory 3 shown in Fig. 1 or in a prescribed storage area of the storage device 1.

In accordance with the first embodiment, as described above, each of the plurality of storage areas constituting the storage device 1 undergo reading and writing of data in response to read/write instructions successively and all storage areas can be automatically subjected to processing for detecting and predicting the occurrence of defective areas in response to the read/write instructions. If a defect is detected, substitution processing can be executed automatically.

Further, the number of retries of the read/write instructions is stored in regard to the storage areas of the storage device 1 and, if the number of retry count regarding a storage area has exceeded a predetermined threshold value, this storage area can be subjected to substitution processing automatically.

As a result of the operation described above, partial defects present in the plurality of storage areas constituting the storage device 1 can be detected and predicted automatically.

<Second Embodiment>

In the first embodiment, storage areas can be automatically subjected to processing for detecting and predicting the occurrence of defects in response to read/write instructions by writing data, which have been read out of a storage area, to the same storage area. However, if, during execution of an initial read instruction and the ensuing write instruction with regard to a certain storage area the same storage area is subjected to a write operation by the user, the data that have been written by the user will be destroyed by the ensuing write instruction in the arrangement described in the first embodiment. Accordingly, in the first embodiment, it is required that the defect detection and prediction applied to storage areas of the storage device be executed under conditions in which the user is not present or under conditions in which other write instructions initiated by the user are forbidden. In other words, a problem with the first embodiment is that ordinary accessing cannot be carried out while detection and prediction of the occurrence of defects is being implemented.

Accordingly, in a second embodiment of the invention, an "inseparable read/write instruction" (ARDWR: Atomic ReaD/WRite) is introduced with respect to disk read/write. The ARDWR instruction allows read/write instructions to be executed successively without interruption. In other words, until execution of a read/write instruction implemented by the ARDWR instruction is finished, an interrupt by another instruction is forbidden. The other instruction is executed only after execution of the ARDWR instruction is completed. More specifically, with regard to a storage area for which defect detection and prediction has not been executed by the ARDWR instruction, another instruction such as an ordinary read instruction or write instruction can be executed. As a result, it is possible to subject storage areas to defect detection and prediction processing even if the user is present or even if another write instruction entered by

the user is not forbidden.

This may readily be implemented by extending the command system of an SCSI (Small Computer System Interface), which is a standard for connecting computer peripherals. It is also possible to implement the foregoing on the software level.

Further, a buffer (memory) area equivalent to one block of a storage area is prepared in order to implement the ARDWR instruction. When the ARDWR instruction is applied to a certain storage area, the data that have been stored in this area are read out, the read data are held in the above-mentioned buffer temporarily and the held data are written again to the same storage area to which the ARDWR instruction was applied. Since the data read out of a certain storage area are written to this storage area after first being placed in the buffer, the stored data will not undergo any change after issuance of the ARDWR instruction.

The processing executed in the second embodiment will now be described with reference to the flowchart of Fig. 3.

Fig. 3 is a flowchart illustrating the flow of processing executed according to the second embodiment.

In response to the ARDWR instruction, a counter "block", which counts the numbers of the storage areas that undergo defect detection and prediction, is initialized to "1" at step S301. This is followed by step S302, at which it is determined whether all storage areas have undergone defect detection and prediction processing. If defect detection and prediction is finished up to the final storage area ("YES" at step S302), then processing is terminated. If defect detection and prediction is not finished for all storage areas ("NO" at step S302), then the program proceeds to step S303.

At step S303, data stored in a storage area corresponding to content indicated by the counter "block" are read out by the ARDWR instruction (ARDWR block), the data are placed in a buffer temporarily and then written back to the same storage area. This is followed by step S304, at which it is determined whether the storage area for which the data read/write operation was performed in response to the ARDWR instruction has developed a recoverable error (referred to as a "recoverable ARDWR error") owing to retry of the storage area. If such an error has occurred ("YES" at step S304), then the program proceeds to step S305. If it is found at step S304 that an error has not occurred ("NO" at step S304), then the program proceeds to step S306.

With regard to a storage area for which an error has occurred owing to the ARDWR instruction, step S305 calls for incrementing of the content (block = n, where n is the nth storage area) of an adding counter E[block] which counts up the number of times the error has occurred owing to the ARDWR instruction. Next, at step S306, it is determined whether the content of the adding counter E[block] is greater than a cumulative error count Emax that has been set in advance. If the content of the adding counter E[block] is greater than the cumulative error count Emax ("YES" at step S306), then the program proceeds to step S307, at which this storage area undergoes substitution processing. If the content of the adding counter E[block] is equal to or less than the cumulative error count Emax ("NO" at step S306), on the other hand, then the program proceeds to step S308.

The content of the counter "block" is incremented at step S308, whence the program returns to step S302. The processing described in connection with steps S302 ~ S308 is repeated until detection and prediction of occurrence of defects is finished for storage areas. When all storage areas have been subjected to detection and prediction of defect occurrence, processing is terminated.

It should be noted that the content of the adding counter E[block] may be stored in the retry-count storage area of the memory 3 shown in Fig. 1 or in a prescribed storage area of the storage device 1.

In accordance with the first embodiment, as described above, each of the plurality of storage areas constituting the storage device 1 can undergo reading and writing of data in response to the ARDWR instruction successively without an interruption caused by another write instruction, and storage areas can be automatically subjected to processing for detecting and predicting the occurrence of defective areas in response to the ARDWR instruction. If a defect is detected, substitution processing can be executed automatically.

Further, it is possible to subject storage areas to defect detection and prediction processing even if the user is absent or even if another write instruction entered by the user is not forbidden.

Further, the number of times errors occur with regard to storage areas of the storage device in response to the ARDWR instruction can be stored and, if the error count exceeds a predetermined threshold value with regard to a particular storage area, this storage area can be subjected to substitution processing automatically.

As a result of the operation described above, partial defects present in the plurality of storage areas constituting the storage device 1 can be detected and predicted automatically.

<Third Embodiment>

In a third embodiment of the invention, the arrangement of the second embodiment is so adapted that after the ARDWR instruction is executed, data are again read out of the storage area, to which the ARDWR instruction was applied, in response to a read instruction and these data are compared with the data that were read out by the ARDWR instruction. This makes it possible to detect and predict even more accurately the occurrence of defects in the storage areas of the storage device.

The processing executed in the third embodiment will now be described with reference to the flowchart of Fig. 4.

Fig. 4 is a flowchart illustrating the flow of process-

ing executed according to the third embodiment.

In response to the ARDWR instruction and a read instruction that follows the ARDWR instruction, a counter "block", which counts the numbers of the storage areas that undergo defect detection and prediction, is initialized to "1" at step S401. This is followed by step S402, at which it is determined whether all storage areas have undergone defect detection and prediction processing. If defect detection and prediction is finished up to the final storage area ("YES" at step S402), then processing is terminated. If defect detection and prediction is not finished up to the final storage area ("NO" at step S402), then the program proceeds to step S403.

At step S403, data stored in a storage area corresponding to content indicated by the counter "block" are read out by the ARDWR instruction (ARDWR block), the data are placed in a buffer temporarily and then written back to the same storage area. This is followed by step S404, at which the data stored in this storage area are read out by the read instruction (read block). Next, at step S405, with regard to data stored in a certain storage area, it is determined whether the data read out by the ARDWR instruction and the data read out by the read instruction that followed the ARDWR instruction are different. If the data are identical ("NO" at step S405), the program proceeds to step S406. If the data are different ("YES" at step S405), however, then the program proceeds to step S409.

It is determined at step S406 whether the storage area for which the data read/write operation was performed in response to the ARDWR instruction has developed a recoverable error (referred to as a "recoverable ARDWR error") owing to retry of the storage area. If such an error has occurred ("YES" at step S406), then the program proceeds to step S407. If it is found at step S406 that an error has not occurred ("NO" at step S406), then the program proceeds to step S408.

With regard to a storage area for which an error has occurred owing to the ARDWR instruction, step S407 calls for incrementing of the content (block = n, where n is the nth storage area) of an adding counter E[block] which counts up the number of times the error has occurred owing to the ARDWR instruction. Next, at step S408, it is determined whether the content of the adding counter E[block] is greater than a cumulative error count Emax that has been set in advance. If the content of the adding counter E[block] is greater than the cumulative error count Emax ("YES" at step S408), then the program proceeds to step S409, at which this storage area undergoes substitution processing. If the content of the adding counter E[block] is equal to or less than the cumulative error count Emax ("NO" at step S408), on the other hand, then the program proceeds to step S410.

The content of the counter "block" is incremented at step S410, whence the program returns to step S402. The processing described in connection with step S402 ~ S408 is repeated until detection and prediction of occurrence of defects is finished for storage areas. When all storage areas have been subjected to detection and prediction of defect occurrence, processing is terminated.

It should be noted that the content of the adding counter E[block] may be stored in the retry-count storage area of the memory 3 shown in Fig. 1 or in a prescribed storage area of the storage device 1.

Further, the third embodiment is obtained by adding the processing of step S404 in Fig. 4 to the second embodiment. However, it is also possible to apply the processing of step S404 to the first embodiment or to other embodiments.

In accordance with the third embodiment, as described above, data stored in a storage area after execution of the ARDWR instruction can be read out again by a read instruction and these data can be compared with the data that were read out by the ARDWR instruction, thereby making possible more accurate automatic detection and prediction of occurrence of defective storage areas. If a defect is detected, substitution processing can be executed automatically.

Further, the number of times errors occur with regard to storage areas of the storage device in response to the ARDWR instruction can be stored and, if the error count exceeds a predetermined threshold value with regard to a particular storage area, this storage area can be subjected to substitution processing automatically.

As a result of the operation described above, partial defects present in the plurality of storage areas constituting the storage device 1 can be detected and predicted automatically.

The processing described in the first through third embodiments can be started up periodically at fixed intervals, such as once a day or once a week, or at start-up or shut-down of the system, by the system software or built-in firmware, or manually at the volition of the administrator.

Further, in order to avoid a decline in overall system performance owing to the processing for detecting and predicting the occurrence of defects in storage areas in accordance with the second and third embodiments, it is possible to adopt an arrangement in which the processing for detecting and predicting the occurrence of defects in storage areas is executed at a selected time, namely when the load on the system is low.

Processing executed by such an arrangement will now be described with reference to Fig. 5.

Fig. 5 is a flowchart illustrating the flow of processing executed to perform the processing described in connection with the second and third embodiments of the invention.

Step S501 in Fig. 5 calls for measurement of the load Lsys, which indicates the load on the system at a certain point in time. This is followed by step S502, at which it is determined whether Lsys is less than a predetermined constant L. If the load equal to or greater than the predetermined constant L ("NO" at step S502), the program proceeds to step S501. On the other hand,

if the load is less than the predetermined constant L ("YES" at step S502), then the program proceeds to step S503. Here the occurrence of defects in the storage areas of the storage device 1 is detected and predicted using any of the arrangements of the first through third embodiments.

Thus, when the system load is high, the invention is not started up and is prevented from influencing other operations.

It is also possible to adopt an arrangement in which the occurrence of defects in the storage areas of the storage device 1 is detected and predicted depending upon overall conditions inclusive of the number of users and the present time (i.e., whether it is late at night, a holiday, etc.).

<Fourth Embodiment>

In the first through third embodiments, the occurrence of defects in the storage areas of a single storage device is detected and predicted. A fourth embodiment of the invention is adapted to detect and predict the occurrence of defects in the storage areas of a plurality of storage devices such as a disk array.

The processing executed in the fourth embodiment will now be described with reference to the flowchart of Fig. 6.

Fig. 6 is a diagram for describing the processing executed according to the fourth embodiment.

Shown in Fig. 6 is a storage device array 10 comprising a plurality of storage devices 11 ~ 14, a CPU (central processing unit) 30 for subjecting the elements of the system to various control, and a memory 30. The memory 30 has a defect checking program (not shown) for executing processing described in the fourth embodiment, as well retry-count storage areas, the number of which correspond to the number of storage devices 11 ~ 14, for performing a function identical with that of the retry-count storage area 3b described above in connection with Fig. 1. It is assumed that the detailed construction of the storage devices 11 ~ 14 is similar to that of the conventional storage device 71 shown in Fig. 7. Further, the retry-count storage areas may be provided in individual storage areas.

If a total number of errors obtained by summing the number of errors that have occurred in each of the storage areas of any of the storages devices 11 ~ 14, or if the number of errors that have occurred in each storage area of the storage areas of any of the storages devices 11 ~ 14, exceeds a predetermined threshold value, substitution processing is executed on a perdevice basis. This can be implemented by sending a message to the user or system administrator and having the user or administrator intervene, or, as shown in Fig. 6, by setting aside the storage device 14 as a spare storage device that usually is not used and executing substitution processing automatically.

In accordance with the first through fourth embodiments, as described above, the occurrence of defects in the storage areas of a storage device can be predicted and substitution processing can be executed to automatically substitute another storage area for one that has failed. This furnishes the storage device with a high reliability and makes it easy to use. Further, storage areas can be subjected to substitution processing and the save effects can be obtained even when a failure has actually occurred.

The present invention can be applied to a system constituted by a plurality of devices (e.g., a host computer, interface, reader, printer, etc.) or to an apparatus comprising a single device (e.g., a copier or facsimile machine, etc.).

Further, it goes without saying that the object of the present invention can also be achieved by providing a storage medium storing program codes for performing the aforesaid functions of the foregoing embodiments to a system or an apparatus, reading the program codes with a computer (e.g., a CPU or MPU) of the system or apparatus from the storage medium, and then executing the program.

In this case, the program codes read from the storage medium implement the functions according to the embodiments, and the storage medium storing the program codes constitutes the invention.

Further, the storage medium, such as a floppy disk, hard disk, optical disk, magneto-optical disk, CD-ROM, CD-R, magnetic tape, non-volatile type memory card or ROM can be used to provide the program codes.

Furthermore, besides the case where the aforesaid functions according to the embodiments are implemented by executing the program codes read by a computer, the present invention covers a case where an operating system (OS) or the like working on the computer performs a part of or the entire process in accordance with the designation of program codes and implements the functions according to the embodiments.

Furthermore, the present invention further covers a case where, after the program codes read from the storage medium are written to a function extension board inserted into the computer or to a memory provided in a function extension unit connected to the computer, a CPU or the like contained in the function extension board or function extension unit performs a part of or the entire process in accordance with the designation of program codes and implements the function of the above embodiments.

In a case where the present invention is applied to the above-mentioned storage medium, program codes corresponding to the flowcharts described earlier are stored on this storage medium. More specifically, modules illustrated in the example of the memory map of Fig. 8 are stored on the storage medium.

Specifically, it will suffice to store program codes of at least a "checking module", an "accumulating module" and a "detecting module" on the storage medium.

The "checking module" checks for defects in stor-

age areas by performing reading and writing of data over all storages areas constituting a storage medium. The "accumulating module" is a module which, when an error that has occurred by checking, is an error for which retry is possible, accumulates the number of times this has occurred. The "detecting module" detects fault locations in the storage areas based upon the type of error that has occurred by checking or the number of occurrences accumulated by the accumulating module.

As many apparently widely different embodiments of the present invention can be made without departing from the spirit and scope thereof, it is to be understood that the invention is not limited to the specific embodiments thereof except as defined in the appended claims.

Claims

1. A storage device equipped with a storage medium, characterized by comprising:

   checking means (2, 3a) for checking for defects in storage areas by performing reading and writing of data over all storages areas constituting the storage medium;
   accumulating means (2, 3a, 3b) which, when an error that has occurred by checking performed by said checking means is an error for which retry is possible, is for accumulating the number of times this has occurred; and
   detecting means (2, 3a, 3b) for detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed by said checking means or the number of occurrences accumulated by said accumulating means.

2. The device according to claim 1, further comprising substitution means for substituting another storage area for a storage area having a defect detected by said detecting means.

3. The device according to any-preceding claim, wherein said detecting means detects a storage area under examination as being a defective location if the number of occurrences accumulated by said accumulating means exceeds a predetermined number or if the error that has occurred by checking performed by said checking means is an error for which retry is possible.

4. The device according to any preceding claim, wherein the storage device has a control instruction for inhibiting instructions from elsewhere during execution of checking by said checking means, thereby allowing checking for defects in the storage areas;

   said checking means checking for defects in the storage areas using said control instruction.

5. The device according to claim 4, further comprising memory means for holding data read out by said checking means;

   said checking means checking for defects of the storage areas by re-reading data out of a storage area after it has been checked by said checking means and comparing the read data and the data held by said memory means.

6. The device according to any preceding claim, wherein the check performed by said checking means is executed at predetermined times.

7. A storage system equipped with a plurality of storage devices, characterized by comprising:

   checking means (20, 30) for checking for defects in storage areas by performing reading and writing of data over all storage areas constituting a storage medium provided in each storage device of the plurality thereof;
   accumulating means (20, 30) which, when an error that has occurred by checking performed by said checking means is an error for which retry is possible, is for accumulating the number of times this has occurred;
   detecting means (20, 30) for detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed by said checking means or the number of occurrences accumulated by said accumulating means;
   monitoring means (20, 30) for monitoring status of detection of each storage device of the plurality thereof by said detecting means; and
   substitution means (20, 30) for substituting one storage device for another in dependence upon status of detection monitored by said monitoring means.

8. A method of controlling a storage device equipped with a storage medium, characterized by comprising:

   a checking step (S201, S202, S203, S207, S211, S213, S217, S301, S302, S303, S308, S401, S402, S403, S404, S410) of checking for defects in storage areas by performing reading and writing of data over all storages areas constituting the storage medium;
   an accumulating step (S208, S214, S305, S407) which, when an error that has occurred by checking performed at said checking step is an error for which retry is possible, is a step of accumulating the number of times this has oc-

curred; and
a detecting step (S204, S209, S212, S215, S304, S306, S405, S406, S408) of detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed at said checking step or the number of occurrences accumulated at said accumulating step.

9. The method according to claim 8, further comprising a substitution step of substituting another storage area for a storage area having a defect detected at said detecting step.

10. The method according to any of claims 8 and 9, wherein said detecting step detects a storage area under examination as being a defective location if the number of occurrences accumulated at said accumulating step exceeds a predetermined number or if the error that has occurred by checking performed at said checking step is an error for which retry is impossible.

11. The method according to any of claims 8 to 10, wherein the method has a control instruction for inhibiting instructions from elsewhere during execution of checking at said checking means, thereby allowing checking for defects in the storage areas;
said checking step checking for defects in the storage areas using said control instruction.

12. The method according to claim 11, further comprising a data holding step of holding data read out at said checking step;
said checking step checking for defects of the storage areas by re-reading data out of a storage area after it has been checked at said checking step and comparing the read data and the data held at said data holding step.

13. The method according to any of claims 8 to 12, wherein the check performed at said checking step is executed at predetermined times.

14. A method of controlling a storage system equipped with a plurality of storage devices; characterized by comprising:

a checking step (S201, S202, S203, S207, S211, S213, S217, S301, S302, S303, S308, S401, S402, S403, S404, S410) of checking for defects in storage areas by performing reading and writing of data over all storages areas constituting a storage medium provided in each storage device of the plurality thereof;
an accumulating step (S208, S214, S305, S407) which, when an error that has occurred by checking performed at said checking step is an error for which retry is possible, is a step of accumulating the number of times this has occurred;
a detecting step (S204, S209, S212, S215, S304, S306, S405, S406, S408) of detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed at said checking step or the number of occurrences accumulated at said accumulating step;
a monitoring step (S205, S210, S216, S307, S409) of monitoring status of detection of each storage device of the plurality thereof at said detecting step; and
a substitution step (S205, S210, S216, S307, S409) of substituting one storage device for another in dependence upon status of detection monitored at said monitoring step.

15. A computer readable memory storing program codes of control processing for controlling a storage device equipped with a storage medium, the memory characterized by comprising:

a program code of a checking step (S201, S202, S203, S207, S211, S213, S217, S301, S302, S303, S308, S401, S402, S403, S404, S410) of checking for defects in storage areas by performing reading and writing of data over all storages areas constituting the storage medium;
a program code of an accumulating step (S208, S214, S305, S407) which, when an error that has occurred by checking performed at said checking step is an error for which retry is possible, is a step of accumulating the number of times this has occurred; and
a program code of a detecting step (S204, S209, S212, S215, S304, S306, S405, S406, S408) of detecting fault locations in the storage areas based upon the type of error that has occurred by checking performed at said checking step or the number of occurrences accumulated at said accumulating step.

16. A method of substituting substitute storage areas for defective storage areas in a storage medium in a storage device comprising the steps of;

controlling the storage device to automatically check all storage areas for defects; and
substituting another storage area for a storage area having a defect.

17. A method of detecting defective storage areas in a storage medium in a storage device, comprising the steps of;

writing data to all storage areas of the storage medium;
reading the data from the storage areas; and
comparing the read and written data.

18. A method as claimed in any of claims 16 and 17 in combination with any one or more of the method steps defined in claims 8 to 14.

19. A storage medium processed according to any one of claims 8 to 14 and 16 to 18.

FIG. 1

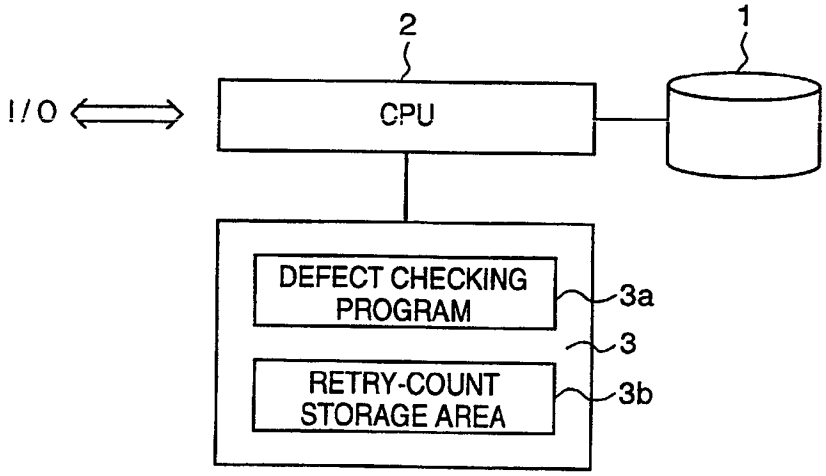


FIG. 2

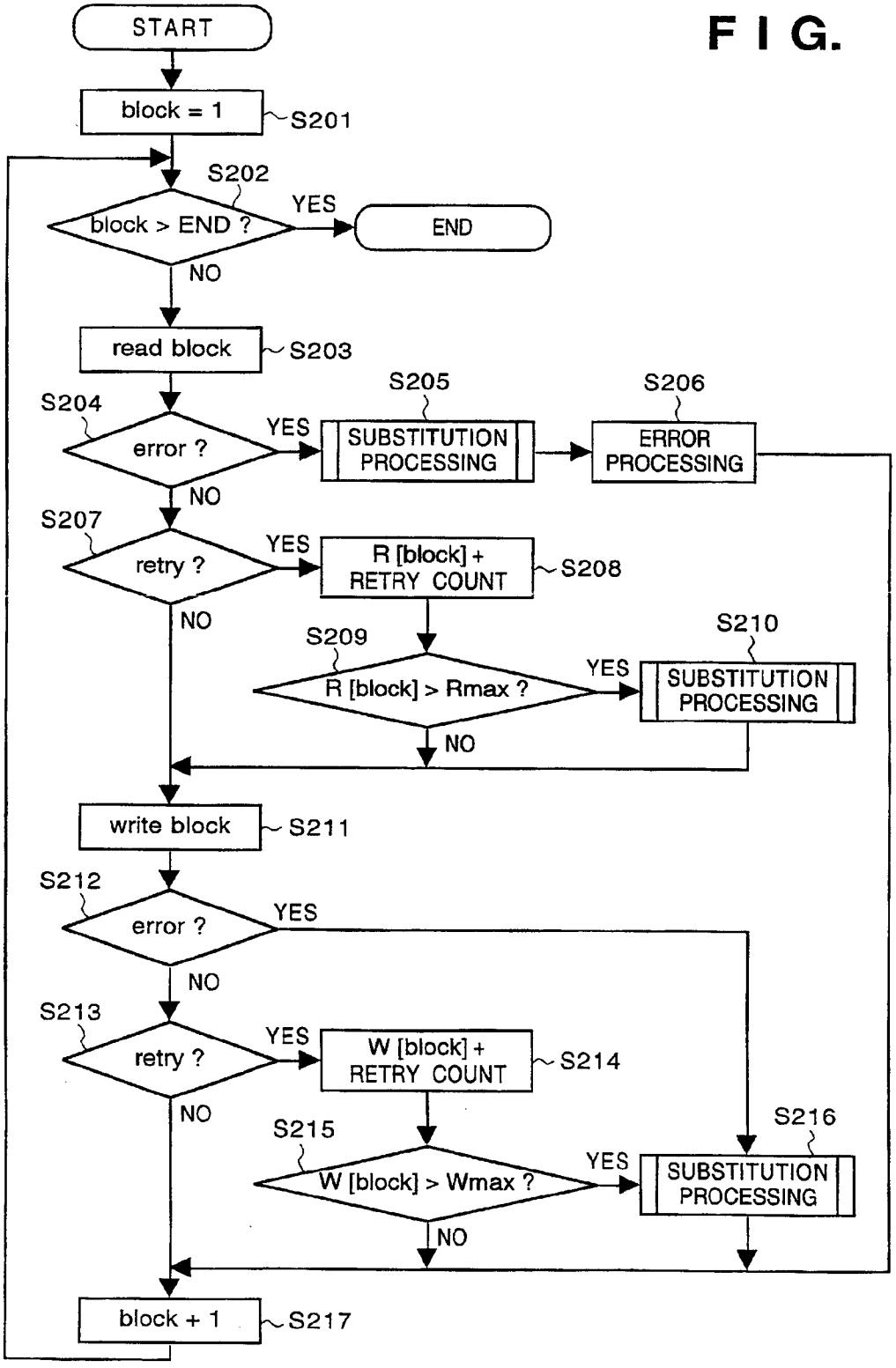


FIG. 3

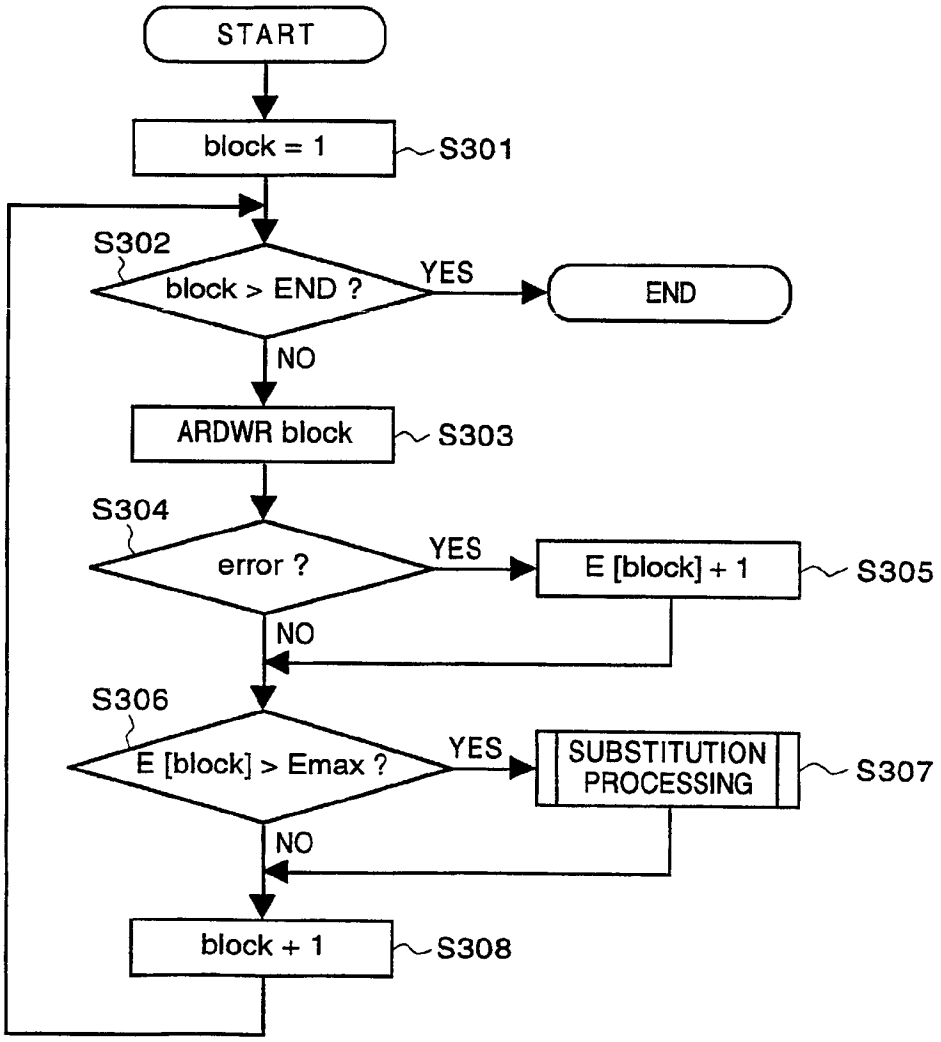


FIG. 4

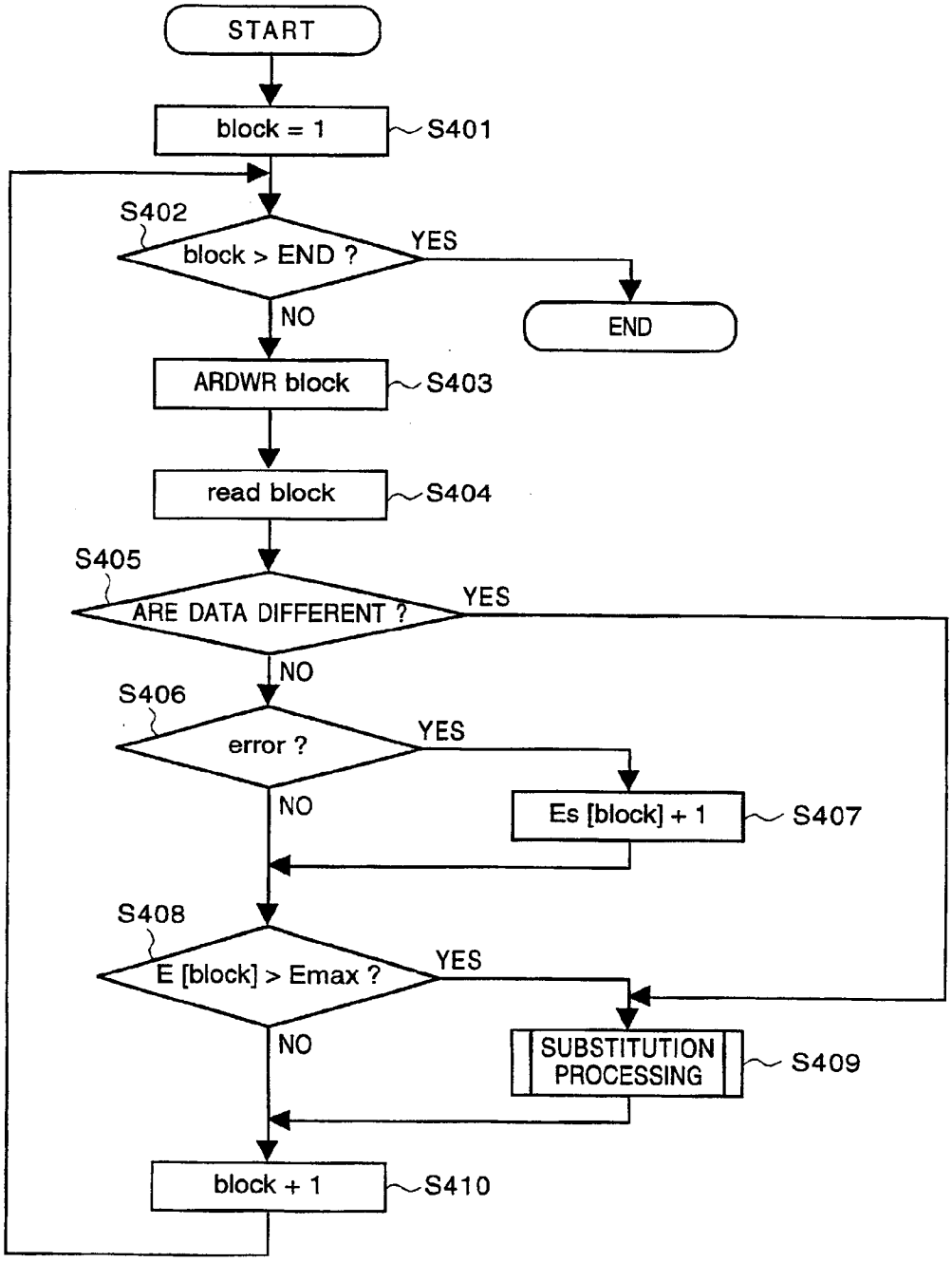


FIG. 5

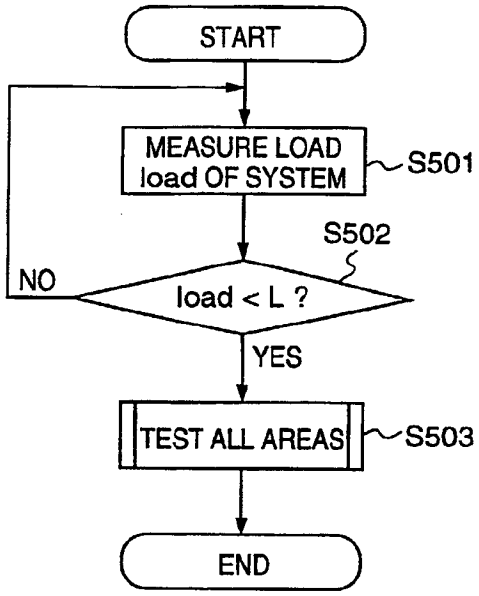


FIG. 6

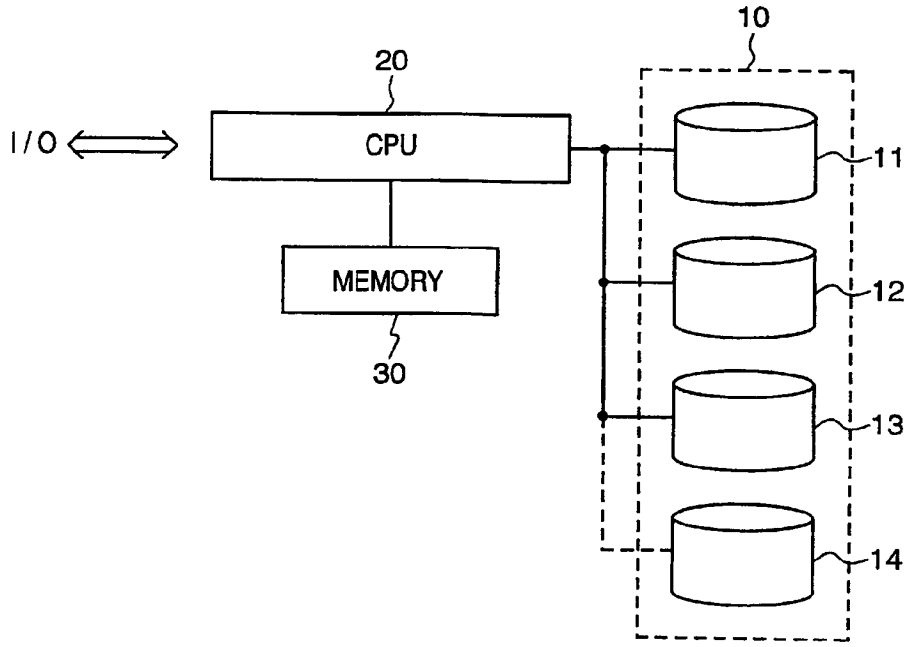


FIG. 7

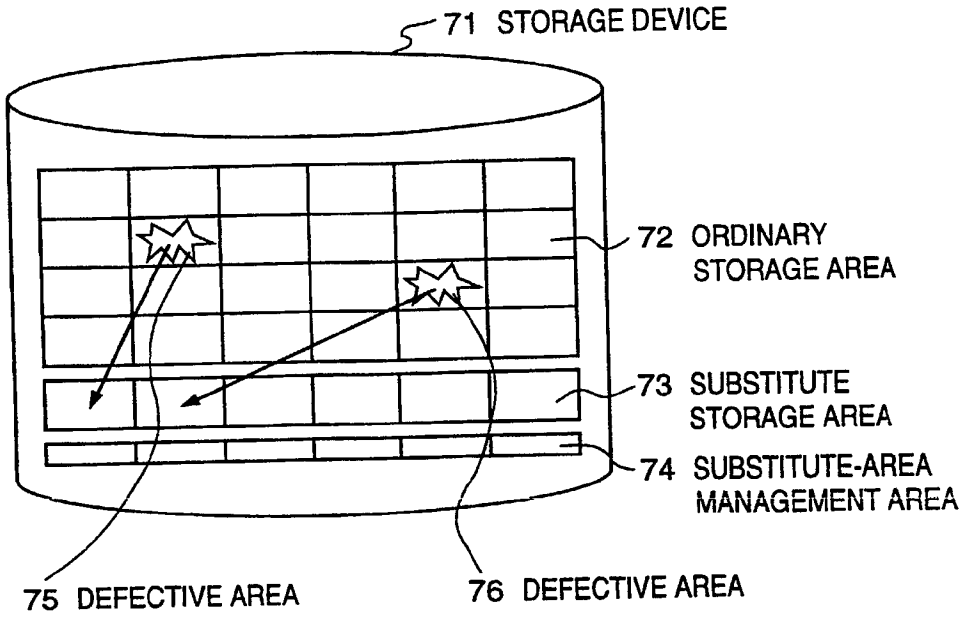
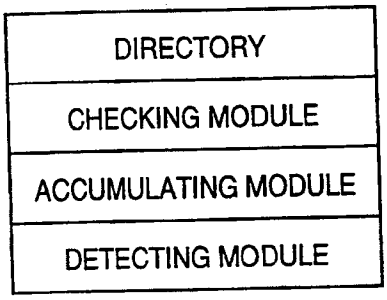


FIG. 8



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(71) Applicant: **CANON KABUSHIKI KAISHA**
Tokyo (JP)

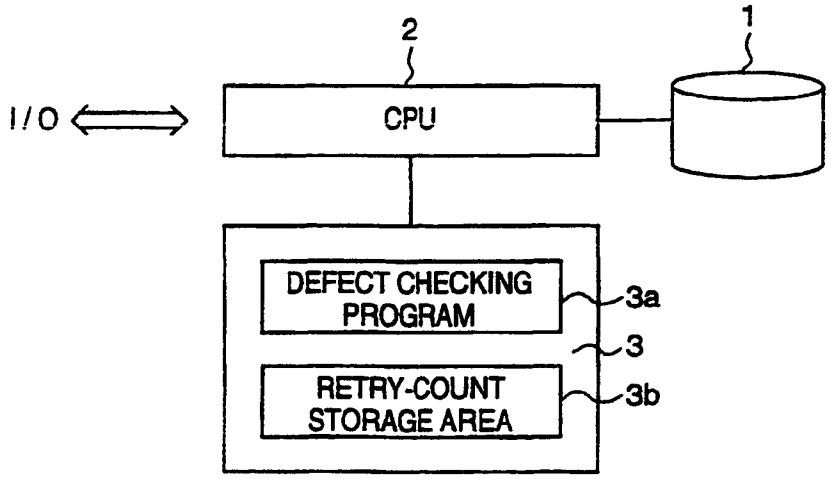
(72) Inventor: **Inoue, Sunao**
Ohta-ku, Tokyo (JP)

(74) Representative:
Beresford, Keith Denis Lewis et al
BERESFORD & Co.
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

(54) Storage device, method of controlling same, storage system and method of controlling same

(57) All storage areas constituting a storage medium 1 are checked for defects by successively reading and writing data. If an error that has occurred owing to the checking operation is an error for which retry is possible, the number of times this occurs is accumulated in a retrial-count storage area 36 of a memory. A faulty storage area is detected based upon the type of error that has occurred by checking or the number of occurrences that have been accumulated.

FIG. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 97 30 2369

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	NN: "Detection and Reallocation of Defective Clusters in Removable DASD Media" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 37, no. 6B, June 1994, US, pages 571-572, XP000456101	8-10, 16-19	G11B20/18
Y	* page 571, line 1 - page 572, last line *	1-7, 11-15	

Y	NN: "Method for Recovering from Runaway Sector Reassignments on Hard Disk Drive" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 34, no. 7B, December 1991, US, pages 178-179, XP002062695 * page 179, paragraph 2 *	1-7, 11-15	

A	NN: "High-Speed Formatting Operation for a Disk File" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 36, no. 8, August 1993, US, pages 673-674, XP002062696 * page 673, line 1 - page 674, last line *	1-19	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
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A	NN: "Effective Management Method of Spare Area Allocation for Sector and Cylinder Effects" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 38, no. 5, May 1995, US, pages 141-142, XP002062697 * page 141, line 1 - page 141, last line *	1-19	

A	NN: "Method for Allocating Spare Sectors after SAT" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 29, no. 1, June 1986, US, pages 210-214, XP002062698 * page 210, line 1 - page 211, last line *	1-19	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 April 1998	Van Staveren, M

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OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
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Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	11/205,121	HAISHIMA, JUN	
	Examiner	Art Unit	
	Bradford A. Rodgers-Farmer	4141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/17/2005;1/25/2008* .
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3 are pending.

2. The examiner has acknowledged the applicant's priority to Japanese Patent Application No. 2004-245377 filed on August, 25, 2004.

Specification

3. The applicant's specification appears to be in proper order. However, it has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of that the applicant may become aware of in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Owada et al (Odwada) (United States Patent NO.5860122).

As Per claim 1 Odwada teaches:

- ***An information process device comprising:***
  a first memory device for storing a boot program executed when the information process device is started to operate; a mother board on which the first memory device is provided;(Odwada, Col 2 lines 35-42, "According to a first aspect of the present invention, a backup unit comprises a first storage means containing at least one program and a setup file in which the operating

environment of this program is written) Wherein the first storage means is the first memory device as claimed and the setup file is the program which is executed. Furthermore a motherboard is an inherent feature of all computers;

- ***a second memory device for storing an application program, the second memory device being connected to the mother board;*** (Odwada, Col 1 lines 5-7, The present invention relates to a backup unit having a countermeasure against a fault in an external storage unit, such as a hard disk drive …) Wherein the harddrive is the second memory device as claimed;

- ***a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device; wherein the fault inspection program is stored in the first memory device;*** (Odwada, Col 3 lines 5-8, According to a fourth aspect of the present invention, the above-mentioned backup unit further comprises a fault detecting means for detecting a fault in the first storage means.);

- ***and wherein the control device executes the fault inspection program when the information process device is started to operate.*** (Odwada, Col 3 lines 9-11,When a fault is detected in the first storage means by the fault detecting means, the switch means selects the second storage means as a storage means for booting) Wherein the fact that it detected the problem during booting must mean that it is running when the device is started.

As Per claim 2 claim 1 is incorporated and further Odwada teaches:

- ***wherein the first memory device is a ROM provided on the mother board, wherein the second memory device is a hard disk which is independent from the mother board, and wherein the control device executes the fault***

inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk. (Odwada, Col 8 lines 29-41 In the first and second embodiments of the invention, the duplication and conversion unit 31, the system loading switch unit 32, the setup file correction detector 33, and the HDD fault detector 34 are implemented by software, i.e., programs loaded to the central control unit 30. However, these constituents may be implemented by hardware. Further, when these constituents are implemented by software, their programs may be stored in the HDD 10. In addition, a program for generating the system loading switch unit 32 may be stored in a ROM in the information processor.)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owada et al (Odwada) (United States Patent NO.5860122) in view of Pascal et al (Pascal) (United States Patent NO. 5971851).

As Per claim 3 claim 1 is incorporated and Odwada does not specifically teach that the information process device is utilized as a gaming machine for business use.

However the analogous art of Pascal teaches the above limitation. (Pascal Col 1 lines 11-15, Game machines … However, these machines occasionally malfunction and enter into a lock up state, ceasing all functions and leaving the player stranded.).

Therefore it would have been obivious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Pascal into the invention of

Owada to create a fault tolerant gaming machine, because one of ordinary skill would have recognized the benefit of preventing players from having to " either abandon the machine after a few attempts at "fixing" the machine, or wait for an attendant's assistance." (Pascal Col 1 lines 15-18).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradford A. Rodgers-Farmer whose telephone number is (571) 270-3888. The examiner can normally be reached on Monday to Thursday 7:30am to 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cameli Das can be reached on 571-272-3696. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bradford A Rodgers-Farmer/
Examiner, Art Unit 4141
March 25, 2008

/CHAMELI C. DAS/
Supervisory Patent Examiner, Art Unit 4141

Notice of References Cited	Application/Control No. 11/205,121	Applicant(s)/Patent Under Reexamination HAISHIMA, JUN	
	Examiner Bradford A. Rodgers-Farmer	Art Unit 4141	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,860,122 A	01-1999	Owada et al.	711/162
*	B	US-5,971,851 A	10-1999	Pascal et al.	463/24
*	C	US-6,449,735 B1	09-2002	Edwards et al.	714/25
*	D	US-2004/0078697 A1	04-2004	Duncan, William L.	714/042
*	E	US-2007/0168738 A1	07-2007	Wang, Chien-Chih	714/036
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11205121	HAISHIMA, JUN
	Examiner	Art Unit
	Bradford A Rodgers-Farmer	4141

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/25/2008								
	1	✓								
	2	✓								
	3	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11205121	HAISHIMA, JUN
	Examiner	**Art Unit**
	Bradford A Rodgers-Farmer	4141

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
714	36	3/25/2008	BARF
710	104	3/25/2008	BARF

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Classes 711/170 and 713/1-100 searched using text	3/25/2008	BARF
Plus searche requested and concidered	3/25/2008	BARF
Google scholar searched	3/25/2008	BARF
IEEE searched	3/25/2008	BARF
East searched using EPO: JPO: Dewert; USPAT; USPgpub	3/25/2008	BARF

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

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BIB DATA SHEET

CONFIRMATION NO. 2910

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/205,121	08/17/2005	714	4141	276900US90

APPLICANTS
Jun Haishima, Tokyo, JAPAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************
JAPAN 2004-245337 08/25/2004

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
09/02/2005

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged: /BRADFORD A RODGERS FARMER/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	3	3	1

ADDRESS
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314
UNITED STATES

TITLE
Information process device

FILING FEE RECEIVED		
1000	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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game machine fault detection Search

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Scholar **All articles - Recent articles** Results **1** - **10** of about **13,300** for **game machine fault detection**. (**0.18** seconds)

All Results

M Yannakakis
D PELED
R Finkel
R Alur
U Manber

Progressive gaming control and communication system - all 3 versions »
DN Hilgendorf, PE Pajak - US Patent 5,249,800, 1993 - Google Patents
... said **fault detection**. 30. ... unit indicating that said current unit over said connect line indicating that the **game** ... **machine** is connected to said communication unit ...
Cited by 21 - Related Articles - Web Search

Distinguishing tests for nondeterministic and probabilistic machines - all 5 versions »
R Alur, C Courcoubetis, M Yannakakis - Proceedings of the twenty-seventh annual ACM symposium on ..., 1995 - portal.acm.org
... two-player **games** wit h incomplete information. A two-player Yv-**game** G consists of a nondetermin- istic **machine** with **game**-positions S, inputs I, out- ...
Cited by 39 - Related Articles - Web Search

Testing, Optimizaton, and Games - all 10 versions »
M Yannakakis - Automata, Languages And Programming: 31st International ..., 2004 - books.google.com
... A deterministic FSM (or Mealy **machine**) M consists of ... Each state diagram defines an instance of the **game**. ... for the extent of the **fault detection** capabifities of ...
Cited by 9 - Related Articles - Web Search

Shooting **game machine** - all 3 versions »
K Suzuki - US Patent 5,366,229, 1994 - Google Patents
... output an on-target **detection** signal to the **game** arith- ... meanS; it is possible to make the whole **game machine** ... would occur no **fault** resu lting from any mis ...
Cited by 32 - Related Articles - Web Search

The Silicon Gaming Odyssey slot **machine** - all 4 versions »
A Levinthal, M Barnett - Compcon'97. Proceedings, IEEE, 1997 - ieeexplore.ieee.org
... Page 3 Navigator, **Games**, Stoppage, MMS Application ... requirements of casino gaming **machines**, including high reliability and security, **fault detection** and recovery ...
Cited by 7 - Related Articles - Web Search

BLACK BOX CHECKING - all 10 versions »
D PELED, M YANNAKAKIS - Formal Methods for Protocol Engineering and Distributed ..., 1999 - books.google.com
... He also posed the **fault detection** or conformance testing ... we want to check whether this **machine** deadlocks, namely ... modeling the problem as a **game** with incomplete ...
Cited by 57 - Related Articles - Web Search

An expert system approach to **fault** diagnosis in hydraulic systems
C Angeli, A Chatzinikolaou - Expert System, 1995 - Blackwell Synergy
... produce a useful tool for **fault** diag- nosis ... based systems, International Journal ofMan-**Machine** Studies, 26,3 ... BWsE, JH and BR **GAMES** (1988) Knowledge Acquisition ...
Cited by 16 - Related Articles - Web Search

On the application of a **machine** learning technique to faultdiagnosis of power distribution lines -

all 4 versions »

M Togami, N Abe, T Kitahashi, H Ogawa, N Mfg - Power Delivery, IEEE Transactions on, 1995 - ieeexplore.ieee.org

... An area of particular interest is **fault detection** and diagnosis. **...** One aim of **machine** learning is to make an algorithm which automatically and efficiently shows **...**

Cited by 12 - Related Articles - Web Search

Can **machine** learning be secure? - all 8 versions »

M Barreno, B Nelson, R Sears, AD Joseph, JD Tygar - Proceedings of the 2006 ACM Symposium on Information, ..., 2006 - portal.acm.org

... within the context of deception **games** [14, 32 **...** 5.2 Scale of Training Some **machine** learning systems are **...** a widely used paradigm in **fault detection** [40], intrusion **...**

Cited by 10 - Related Articles - Web Search

Traction Monitoring for Collision **Detection** with Legged Robots - all 7 versions »

MJ Quinlan, CL Murch, RH Middleton, SK Chalup - Robocup 2003: Robot Soccer World Cup VII, 2004 - books.google.com

... the legs slip on ice the **machine** would not **...** soccer, but the objective of the **game** is identical **...** Note however that the **fault detection** methods presented below are **...**

Cited by 14 - Related Articles - Web Search

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Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 276900US8	SERIAL NO. 11/205,121
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Jun HAISHIMA	
		FILING DATE August 17, 2005	GROUP 2113

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
/B.A.R.F./	AA	US 6,449,735 B1	9/10/2002	David A. EDWARDS, et al.			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
/B.A.R.F./	AO	JP 9-319445	12/12/1997	Japan (with English Abstract)		x
/B.A.R.F./	AP	JP 2000-35888	2/2/2000	Japan (with English Abstract)		x
/B.A.R.F./	AQ	EP 0 774 716 A1	5/21/1997	Europe		
/B.A.R.F./	AR	EP 0 801 387 A2	10/15/1997	Europe		
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	
	AX	
	AY	
	AZ	

☐ Additional References sheet(s) attached

Examiner	/Bradford Rodgers-Farmer/	Date Considered	03/25/2008

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Docket No. 276900US90

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jun HAISHIMA

SERIAL NO: New Application GAU:

FILED: Herewith EXAMINER:

FOR: INFORMATION PROCESS DEVICE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:
Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

☐ Attached is a list of applicant's pending application(s), published application(s) or issued patent(s) which may be related to the present application. In accordance with the waiver of 37 CFR 1.98 dated September 21, 2004, copies of the cited pending applications are not provided. Cited published and/or issued patents, if any, are listed on the attached PTO form 1449.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Masayasu Mori
Registration No. 47,301
C. Irvin McClelland
Registration Number 21,124

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 05/03)

Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO.	SERIAL NO.
LIST OF REFERENCES CITED BY APPLICANT		276900US90	New Application
		APPLICANT: Jun HAISHIMA	
		FILING DATE: Herewith	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
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	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
/B.A.R.F./	AO	2003-330793	11/21/2003	Japan (with English Abstract)		X
/B.A.R.F./	AP	2003-331236	11/21/2003	Japan (with English Abstract)		X
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

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	AX	
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	AZ	

☐ Additional References sheet(s) attached

Examiner /Bradford Rodgers-Farmer/ Date Considered 03/25/2008

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Results for "(((gaming machine)<in>metadata) <and> ((fault)<in>metadata))<and> ((det..."

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Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

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(((gaming machine)<in>metadata) <and> ((fault)<in>metadata))<and> ((detection)<in>m

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1. **The Silicon Gaming Odyssey slot machine**
   Levinthal, A.; Barnett, M.;
   Compcon '97. Proceedings, IEEE
   23-26 Feb. 1997 Page(s):296 - 301
   Digital Object Identifier 10.1109/CMPCON.1997.584736
   AbstractPlus | Full Text: PDF(436 KB) IEEE CNF
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	339	(714/36).CCLS.	US-PGPUB; USPAT	OR	OFF	2008/03/25 14:24
L2	1144	(710/104).CCLS.	US-PGPUB; USPAT	OR	OFF	2008/03/25 15:02
L3	1	("6,449,735").PN.	US-PGPUB; USPAT	OR	OFF	2008/03/25 15:06
L4	1	("5860122").PN.	US-PGPUB; USPAT	OR	OFF	2008/03/25 15:08
L5	7927	711/170.ccls. 713/1-100.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2008/03/25 16:05
L6	5056597	memory storage area ROM	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2008/03/25 16:05
L7	176959	(fault error problem crash) near (program detect$4 inspect$6 software device locat$4)	US-PGPUB; USPAT	OR	ON	2008/03/25 16:08
L8	820841	boot start$1up "start-up" POST	US-PGPUB; USPAT	OR	ON	2008/03/25 16:09
L9	38264	(fault problem crash error) near l6	US-PGPUB; USPAT	OR	ON	2008/03/25 16:09
L10	3576	l8 and l7 and l9 and l6	US-PGPUB; USPAT	OR	ON	2008/03/25 16:10
L11	88	l8 and l7 and l9 and l6 and l5	US-PGPUB; USPAT	OR	ON	2008/03/25 16:10
L12	903	l8 and l7 and l9 and l6 and "714".clas.	US-PGPUB; USPAT	OR	ON	2008/03/25 16:10
L13	2612	l7 same ROM	US-PGPUB; USPAT	OR	ON	2008/03/25 16:12
L14	921	(fault problem crash error) near ("Hard disk" "hard drive" HDD HD)	US-PGPUB; USPAT	OR	ON	2008/03/25 16:13
L15	67	l13 and l12	US-PGPUB; USPAT	OR	ON	2008/03/25 16:13
L16	1	l4 and l15	US-PGPUB; USPAT	OR	ON	2008/03/25 16:13

L17	26147	((arcade gam$4) near (machine portable)) psp gameboy playstation nintendo xbox	US-PGPUB; USPAT	OR	ON	2008/03/25 16:40
L18	223	l17 and "714".clas.	US-PGPUB; USPAT	OR	ON	2008/03/25 16:40
L19	55	l18 l8	US-PGPUB; USPAT	AND	ON	2008/03/25 16:41
L20	3575356	memory storage area ROM	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:40
L21	84621	(fault error problem crash) near (program detect$4 inspect$6 software device locat$4)	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:40
L22	259085	boot start$1up "start-up" POST	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:40
L23	3	(fault problem crash error) l20	FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/03/25 17:41
L24	0	l23 and l22 and l21	FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/03/25 17:41
L25	0	l23 and l22	FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/03/25 17:41
L26	0	l22 and l23	FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/03/25 17:42
L27	679	l22 and l21	FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/03/25 17:42
L28	267	l22 and l21 and l20	FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/03/25 17:42
L29	166	(fault problem crash error) near ("Hard disk" "hard drive" HDD HD)	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:42

L30	117891	((arcade gam$4) near (machine portable)) psp gameboy playstation nintendo xbox	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:42
L31	0	l29 and l28	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:42
L32	0	l30 and l29	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:43
L33	1587	l30 and l22	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:43
L34	242	l30 and l21	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:43
L35	3	l33 and l21	FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/03/25 17:43

3/ 25/ 2008 6:07:22 PM

DOCKET NO: 276900US8

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
JUN HAISHIMA	: EXAMINER: RODGERS FARMER, B.A.
SERIAL NO: 11/205,121	:
FILED: AUGUST 17, 2005	: GROUP ART UNIT: 4141
FOR: INFORMATION PROCESS DEVICE	:

AMENDMENT

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action dated April 3, 2008, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 6 of this paper.

IN THE SPECIFICATION

Please replace the Abstract on page 8, lines 1-6 in its entirety, as follows:

ABSTRACT

An information processing device and associated methodology are provided for inspecting a program fault. A first memory stores a boot program executed when the information processing device is initiated for operation. A second memory device is provided for storing an application program. A control device executes a fault inspection program to inspect whether or not a fault has occurred in the second memory device. The fault inspection program is stored in the first memory device and is initiated upon initialization of the information processing device.

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): An information process device comprising:

a first memory device for storing a boot program executed when the information process device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing an application program, the second memory device being connected to the mother board;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device;

wherein the fault inspection program is stored in the first memory device; and

wherein the control device executes the fault inspection program when the information process device is started to operate.

Claim 2 (Original): The information process device according to claim 1, wherein the first memory device is a ROM provided on the mother board,

wherein the second memory device is a hard disk which is independent from the mother board, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk.

Claim 3 (Original): The information process device according to claim 1, wherein the information process device is utilized as a gaming machine for business use.

Claim 4 (New): A gaming machine utilizing an information process device, the

information process device comprising:

a first memory device configured to store a boot program executed when the information process device is started to operate;

a mother board on which the first memory device is provided;

a second memory device configured to store a game application program, the second memory device being connected to the mother board and electrically rewritable;

a control device configured to execute a fault inspection program to inspect whether or not a fault occurs in the second memory device;

wherein the fault inspection program is stored in the first memory device;

wherein the control device executes the fault inspection program every time the information process device is started to operate, and

wherein when the fault does not occur in the second memory device the game application program is started to execute and when the fault occurs in the second memory device an error display is conducted on a display device.

Claim 5 (New): The gaming machine according to Claim 4,

wherein the first memory device is a ROM provided on the mother board,

wherein the second memory device is a hard disk which is independent from the mother board, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk.

Claim 6 (New): The gaming machine according to Claim 5, further comprising:

a RAM provided on the mother board;

wherein the game application program is loaded from the hard disk to the RAM and executed by the control device when the fault does not occur in the hard disk.

REMARKS

Favorable reconsideration of this application as presently amended, and in light of the following discussion, is respectfully requested.

After entry of the foregoing amendment, Claims 1-6 remain pending in the present application. New Claims 4-6 are added and find support in the original specification and claims. A new Abstract has been submitted which is in a better format for U.S. practice. No new matter has been added.

By way of summary, the Official Action presents the following issues: Claims 1-2 stand rejected under 35 U.S.C. § 102 as being unpatentable over Owada et al. (U.S. Patent No. 5,860,122, hereinafter "Owada"); and Claim 3 stands rejected under 35 U.S.C. § 103 as being unpatentable over Owada in view of Pascal et al. (U.S. Patent No. 5,971,851, hereinafter "Pascal").

REJECTION UNDER 35 U.S.C. § 102

The Official Action has rejected Claims 1 and 2 under 35 U.S.C. § 102 as being unpatentable over Owada. The Official Action contends that Owada describes all of the Applicant's claimed features. Applicant respectfully traverses the rejection.

Applicant's Claim 1 recites, *inter alia*, an information processing device, including:

> a first memory device for storing a boot program executed when the information process device is started to operate; ...
>
> a second memory device for storing an application program, the second memory device being connected to the mother board;
>
> a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device;
>
> wherein the fault inspection program is stored in the first memory device. ...

As can be appreciated from the above claim language, the first memory device as claimed must store a boot program and a fault inspection program. The fault inspection program of the first memory device is executed to inspect whether or not a fault occurs in the second memory device.

At pages 2-3 of the Official Action, the first memory device is identified as corresponding to column 2, lines 35-42 of Owada. Additionally, the control device is identified as corresponding to column 3, lines 5-8 of Owada. In other words, the Official Action is taking the position that the central control unit (30) and HDT fault detector (34) as shown in Figure 5 of Owada, corresponds to the claimed fault inspection program. However, the Official Action has also taken the position that the first memory device is a first storage means which contains at least one program and a set up file.

As the Official Action has not identified a first memory in accordance with Applicant's claims, namely, a memory that includes both **A Boot Program and a Fault Inspection Program,** the rejection is clearly improper under 35 U.S.C. § 102.

Accordingly, Applicant respectfully request that the rejection of Claims 1 and 2 under 35 U.S.C. § 102 be withdrawn.

REJECTION UNDER 35 U.S.C. § 103

The Official Action has rejected Claim 3 under 35 U.S.C. § 103 as being unpatentable over Owada in view of Pascal. The Official Action contends that the combination of these references describe all of the Applicant's claimed features. Applicant respectfully traverses the rejection.

As noted above, Owada does not provide all of the features of the Applicant's claims for which it has been asserted. Likewise, as Pascal does not remedy the deficiencies

discussed above, either alone or in combination with Owada, Applicant respectfully submit that a *prima facie* case of obviousness has not been presented.

Accordingly, Applicant respectfully request that the rejection of Claim 3 under 35 U.S.C. § 103 be withdrawn.

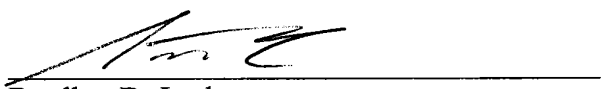
NEW CLAIMS

New Claims 4-6 present more detailed aspects of the Applicants specification. For example, as recited in Claim 4, before execution of an application program a fault inspection program inspects a fault in electrically-rewritable second memory device. If there is no fault detected, a game application program is executed. New Claim 6 recites that a RAM is provided on a mother board and loaded with an application program of a hard disk when a fault is not detected. Applicants respectfully submit that these more detailed aspects of the Applicants claimed advancements are neither disclosed nor suggested by the art of record.

CONCLUSION

Consequently, in view of the foregoing amendment and remarks, it is respectfully submitted that the present application, including Claims 1-6, is patentably distinguished over the prior art, in condition for allowance, and such action is respectfully requested at an early date.

Respectfully submitted,
OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Bradley D. Lytle
Attorney of Record
Registration No. 40,073

Scott A. McKeown
Registration No. 42,866

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/07)

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Electronic Acknowledgement Receipt

EFS ID:	3551268
Application Number:	11205121
International Application Number:	
Confirmation Number:	2910
Title of Invention:	Information process device
First Named Inventor/Applicant Name:	Jun Haishima
Customer Number:	22850
Filer:	Marvin Jay Spivak/Corrine Cunningham
Filer Authorized By:	Marvin Jay Spivak
Attorney Docket Number:	276900US90
Receipt Date:	01-JUL-2008
Filing Date:	17-AUG-2005
Time Stamp:	16:59:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		276900USamendment.pdf	263094 151efe5b823f3631d1e6a86f16740c0d59ac3d04	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment - After Non-Final Rejection	2	2
	Specification	3	3
	Abstract	4	4
	Claims	5	7
	Applicant Arguments/Remarks Made in an Amendment	8	10
Warnings:			
Information:			
	Total Files Size (in bytes):	263094	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No. 276900US8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Jun HAISHIMA

SERIAL NO: 11/205,121 ART UNIT: 4141

FILING DATE: August 17, 2005 EXAMINER: RODGERS, FARMER, B.A.

FOR: INFORMATION PROCESS DEVICE

FEE TRANSMITTAL

■ No additional fee is required

☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.

The Fee has been calculated as shown below:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	6 - 20 =	0	x $50 =	$0.00
INDEPENDENT CLAIMS	2 - 3 =	0	x $210 =	$0.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ $370 =	$0.00
☐ LATE FILING OF DECLARATION			+ $130 =	$0.00
			BASIC FEES	$0.00
			TOTAL OF ABOVE CALCULATIONS	$0.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				$0.00
☐ FILING IN NON-ENGLISH LANGUAGE			+ $130 =	$0.00
			TOTAL	$0.00

☐ Please charge Deposit Account No. 15-0030 in the amount of **$0.00**

☐ A check in the amount of **$0.00** to cover the filing fee is enclosed.

☐ Online credit card payment is being made to cover the filing fee in the amount of **$0.00**

■ The Director is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to Deposit Account No. 15-0030.

■ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030.

Submitted by:

Bradley D. Lytle
Registration No. 40,073

Scott A. McKeown
Registration No. 42,866

Customer Number
22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 07/07)

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/205,121	08/17/2005	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	07/01/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 6	Minus	** 20	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/ADRIENE D. SELLMAN/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	08/17/2005	Jun Haishima	276900US90	2910

22850 7590 11/04/2008

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
CONTINO, PAUL F	
ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
11/04/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	11/205,121	HAISHIMA, JUN	
	Examiner	Art Unit	
	PAUL F. CONTINO	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION: Non-final Rejection

Response to Arguments

1. Applicant's arguments, filed July 1, 2008, with respect to the rejection of claims 1-3 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made as follows.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. PGPub 2005/0246586) in view of Official Notice.

As in claim 1, Chang teaches an information process device comprising:

a first memory device for storing a boot program executed when the information process device is started to operate *(Fig. 3 #10; paragraph [0002], BIOS)*;

a mother board on which the first memory device is provided *(Fig. 3; paragraph [0005], [0007], and [0037], ROM containing BIOS and a motherboard)*;

a second memory device for storing an application program, the second memory device being connected to the mother board *(paragraph [0002], hard disk)*;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device *(paragraph [0002], BIOS contains a testing program)*;

wherein the fault inspection program is stored in the first memory device *(paragraph [0002])*; and

wherein the control device executes the fault inspection program when the information process device is started to operate *(paragraph [0002])*.

However, Chang fails to expressly teach of a mother board or a second memory device attached to a mother board. The Examiner takes Official Notice that it would have been obvious to one skilled in the art at the time the invention was made to have included these elements in the invention of Chang. This would have been obvious because it is well known in the art to include a memory device (ROM) on a mother board and to connect a second memory device (hard disk) to the motherboard, resulting in a compact, efficient, and properly working computer system.

As in claim 2, Chang teaches the first memory device is a ROM provided on the mother board *(paragraph [0005])*,

wherein the second memory device is a hard disk which is independent from the mother board *(paragraph [0002])*, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk *(paragraph [0002])*.

As in claim 3, Chang teaches of the information processing device as a machine for general use. However, Chang fails to teach of using the device as a gaming machine for business use. The Examiner takes Official Notice that it would have been obvious to a person skilled in the art at the time the invention was made to utilize the invention of Chang as a gaming machine for business use. This would have been obvious because it is well known in the art to use a computer as a business tool with software included which runs gaming applications as a secondary utilization.

* * *

4. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Yamato (U.S. Patent No. 6,115,036), further in view of Official Notice.

As in claim 4, Chang teaches of a machine utilizing an information processing device, the information process device comprising:

a first memory device for storing a boot program executed when the information process device is started to operate *(Fig. 3 #10; paragraph [0002], BIOS)*;

a mother board on which the first memory device is provided *(Fig. 3; paragraph [0005], [0007], and [0037], ROM containing BIOS and a motherboard)*;

a second memory device configured to store an application program, the second memory device being connected to the mother board and electrically rewritable *(paragraph [0002], hard disk)*;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device *(paragraph [0002], BIOS contains a testing program)*;

wherein the fault inspection program is stored in the first memory device *(paragraph [0002])*; and

wherein the control device executes the fault inspection program every time the information process device is started to operate *(paragraph [0002])*; and

wherein when the fault does not occur in the second memory device the application program is started to execute and when the fault occurs in the second memory device an error display is conducted on a display device *(paragraph [0002])*.

However, Chang fails to expressly teach of a gaming machine, a game application program, a mother board or a second memory device attached to a mother board. Yamato teaches of a gaming machine and a game application program *(Fig. 1A; column 26 lines 1-14 [game application program] and 54-57)*. It would have been obvious to a person skilled in the art at the time the invention was made to have included the gaming components as taught by

Yamato in the invention of Chang because Chang offers a further level of fault tolerance while booting a computer system using a BIOS in the invention of Yamato.

The Examiner takes Official Notice that it would have been obvious to one skilled in the art at the time the invention was made to have included a mother board and a second memory device in the combined invention of Chang and Yamato. This would have been obvious because it is well known in the art to include a memory device (ROM) on a mother board and to connect a second memory device (hard disk) to the motherboard, resulting in a compact, efficient, and properly working computer system.

As in claim 5, Chang teaches the first memory device is a ROM provided on the mother board *(paragraph [0005])*,

wherein the second memory device is a hard disk which is independent from the mother board *(paragraph [0002])*, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk *(paragraph [0002])*.

As in claim 6, Yamato teaches of a RAM provided on the mother board *(Fig. 2A)*;

wherein the game application program is loaded from the hard disk to the RAM and executed by the control device when the fault does not occur in the hard disk *(Chang: paragraph [0002] hard disk; Yamoto: column 5 lines 36-37, program from disk 8 to RAM 4)*.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL F. CONTINO whose telephone number is (571)272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul F. Contino/
28 October 2008
Patent Examiner
AU 2114

Notice of References Cited	Application/Control No. 11/205,121	Applicant(s)/Patent Under Reexamination HAISHIMA, JUN	
	Examiner PAUL F. CONTINO	Art Unit 2114	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0246586	11-2005	Chang, Yen Sheng	714/036
*	B	US-6,115,036	09-2000	Yamato et al.	715/723
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11205121	HAISHIMA, JUN
	Examiner	Art Unit
	PAUL F. CONTINO	2114

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/25/2008	10/28/2008							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4		✓							
	5		✓							
	6		✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11205121	HAISHIMA, JUN
	Examiner	Art Unit
	PAUL F. CONTINO	2114

SEARCHED

Class	Subclass	Date	Examiner
714	36	10/28/2008	PFC
710	104	10/28/2008	PFC

SEARCH NOTES

Search Notes	Date	Examiner
Previous Examiner's prosecution history	10/28/2008	PFC
714/2,3,5 - text search - see included search history	10/28/2008	PFC
Inventor search	10/28/2008	PFC

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1592	714/36.ccls. 710/104.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 17:25
S1	2	"5860122".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 10:32
S2	2	"5971851".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 10:34
S4	1662	714/3,5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 14:38
S5	2664	713/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 14:38
S6	4296	S4 S5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 14:38
S7	309	S6 and (boot$3 with (rom eprom eeprom)) and ((fault$3 corrupt $3 error erroneous fail $3) with (memory hdd harddrive hard adj (drive disc disk)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 14:39

S8	68	S6 and (boot$3 with (rom eprom eeprom)) same ((fault$3 corrupt $3 error erroneous fail $3) with (memory hdd harddrive hard adj (drive disc disk)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 14:40
S9	18	S6 and (boot$3 with (rom eprom eeprom)) same ((fault$3 corrupt $3 error erroneous fail $3) with (hdd harddrive hard adj (drive disc disk)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 14:41
S10	2	(boot$3 with post with (rom eprom eeprom)) same ((fault$3 corrupt $3 error erroneous fail $3) with (hdd harddrive hard adj (drive disc disk)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 14:45
S11	1	(boot$3 with (test$3 diagnos $5) with (rom eprom eeprom)) same ((fault$3 corrupt $3 error erroneous fail $3) with (hdd harddrive hard adj (drive disc disk)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 14:45

S12	43	(boot$3 with (post test$3 diagnos$5)) same ((fault$3 corrupt$3 error erroneous fail $3) with (hdd harddrive hard adj (drive disc disk)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 14:46
S13	1991	boot$3 with (gam$3 videogam$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 15:40
S14	39	S13 with bios	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/10/28 15:40

10/28/08 5:32:38 PM
C:\Documents and Settings\pcontino\My Documents\EAST\Workspaces\11_205121.wsp

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BIB DATA SHEET

CONFIRMATION NO. 2910

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/205,121	08/17/2005	714	2114	276900US90

APPLICANTS
Jun Haishima, Tokyo, JAPAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************
JAPAN 2004-245337 08/25/2004

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
09/02/2005

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /PAUL F CONTINO/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	3	3	1

ADDRESS

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314
UNITED STATES

TITLE

Information process device

FILING FEE RECEIVED		
1000	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

DOCKET NO: 276900US8

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
JUN HAISHIMA	: EXAMINER: P. F. CONTINO
SERIAL NO: 11/205,121	:
FILED: AUGUST 17, 2005	: GROUP ART UNIT: 2114
FOR: GAMING APPARATUS HAVING MEMORY FAULT DETECTION	:

AMENDMENT

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action dated November 4, 2008, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks begin on page 6 of this paper.

IN THE SPECIFICATION

Please delete the title on page 1 and insert therefor the following replacement title as follows:

GAMING APPARATUS HAVING MEMORY FAULT DETECTION

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): An information process device comprising:

a first memory device for storing a boot program executed when the information process device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing an application program, the second memory device being connected to the mother board;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device and the application program stored therein;

wherein the fault inspection program is stored in the first memory device; and

wherein the control device executes the fault inspection program when the information process device is started to operate.

Claim 2 (Original): The information process device according to claim 1, wherein the first memory device is a ROM provided on the mother board,

wherein the second memory device is a hard disk which is independent from the mother board, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk.

Claim 3 (Original): The information process device according to claim 1, wherein the information process device is utilized as a gaming machine for business use.

Claim 4 (Currently Amended): A gaming machine utilizing an information process device, the information process device comprising:

a first memory device configured to store a boot program executed when the information process device is started to operate;

a mother board on which the first memory device is provided;

a second memory device configured to store a game application program, the second memory device being connected to the mother board and electrically rewritable;

a control device configured to execute a fault inspection program to inspect whether or not a fault occurs in the second memory device and the application program stored therein;

wherein the fault inspection program is stored in the first memory device;

wherein the control device executes the fault inspection program every time the information process device is started to operate, and

wherein when the fault does not occur in the second memory device the game application program is started to execute and when the fault occurs in the second memory device an error display is conducted on a display device.

Claim 5 (Previously Presented): The gaming machine according to Claim 4,

wherein the first memory device is a ROM provided on the mother board,

wherein the second memory device is a hard disk which is independent from the mother board, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk.

Claim 6 (Previously Presented): The gaming machine according to Claim 5, further comprising:

a RAM provided on the mother board;

wherein the game application program is loaded from the hard disk to the RAM and executed by the control device when the fault does not occur in the hard disk.

Claim 7 (New): An information process device comprising:

a first memory device for storing a boot program executed when the information process device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing an application program and a BIOS, the second memory device being connected to the mother board;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device and the application program stored therein;

wherein the fault inspection program is stored in the first memory device; and

wherein the control device executes the boot program to initialize the BIOS stored in the second memory device before executing the fault inspection program when the information process device is started to operate.

REMARKS

Favorable reconsideration of this application as presently amended, and in light of the following discussion, is respectfully requested.

After entry of the foregoing amendment, Claims 1-7 remain pending in the present application. Claims 1 and 4 have been amended to include features described at least at page 5 of the specification. New Claim 7 has been added. Support for which is found at least at page 4 of the specification. A new title has been submitted. No new matter has been added.

By way of summary, the Official Action presents the following issues: the title of the invention is objected to as to matters of form; Claims 1-3 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chang (U.S. Patent Publication 2005/0246586) in view of Official Notice; and Claims 4-6 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chang in view of Yamato (U.S. Patent 6,115,036) in further view of Official Notice.

Objection to the Title

With regard to the objection to the title outlined at paragraph 2 of the Official Action, Applicant submits herewith a new title.

Accordingly, Applicant respectfully requests that the objection to the title be withdrawn.

Rejection under 35 U.S.C. § 103

The Official Action has rejected Claims 1-3 under 35 U.S.C. § 103 as being unpatentable over Chang. The Official Action contends that Chang describes or suggests all of the Applicant's claimed features, in combination with Official Notice. Applicant respectfully traverses the rejection.

Applicant's amended Claim 1 recites, *inter alia*, an information processing device, including:

> a first memory device for storing a boot program executed when the information process device is started to operate;
>
> a mother board on which the first memory device is provided;
>
> a second memory device for storing an application program, the second memory device being connected to the mother board;
>
> a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device and the application program stored therein; ...

Applicant's amended claims require that the control device be configured to execute a fault inspection program which inspects whether or not a fault occurs in a second memory device and an application program stored therein.

As the Official Action has cited the BIOS of Chang as corresponding to the fault detection program, Applicant points out that the BIOS does not perform any analysis of application programs.

Accordingly, Applicant respectfully requests that the rejection of Claims 1-3 under 35 U.S.C. § 103 be withdrawn.

The Official Action has rejected Claims 4-6 under 35 U.S.C. § 103 as being unpatentable over Chang and Yamato, in view of Official Notice. Applicant respectfully traverses the rejection.

As noted above, Chang does not provide all of the features of the Applicant's amended claims for which it has been cited. Likewise, as Yamato nor Official Notice is relied upon for such features, nor do they provide such features, Applicant respectfully submits that a *prima facie* case of obviousness has not been presented.

Accordingly, Applicant respectfully requests that the rejection of Claims 4-6 under 35 U.S.C. § 103 be withdrawn.

NEW CLAIM

New Claim 7 has been added to clarify that a BIOS is included in the claim device and provides functionality which is separate with respect to the fault inspection program. Claim 7 is allowable over the art of record at least for the reasons discussed above.

CONCLUSION

Consequently, in view of the foregoing amendment and remarks, it is respectfully submitted that the present application, including Claims 1-6, is patentably distinguished over the prior art, in condition for allowance, and such action is respectfully requested at an early date.

Respectfully submitted,
OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Bradley D. Lytle
Attorney of Record
Registration No. 40,073

Scott A. McKeown
Registration No. 42,866

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/07)

I:\ATTY\SAM\PROSECUTION WORK\276900\276900US-AM DUE 02-04-09.DOC

Electronic Acknowledgement Receipt

EFS ID:	4711208
Application Number:	11205121
International Application Number:	
Confirmation Number:	2910
Title of Invention:	Information process device
First Named Inventor/Applicant Name:	Jun Haishima
Customer Number:	22850
Filer:	Marvin Jay Spivak/Corrine Cunningham
Filer Authorized By:	Marvin Jay Spivak
Attorney Docket Number:	276900US90
Receipt Date:	30-JAN-2009
Filing Date:	17-AUG-2005
Time Stamp:	17:41:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		276900USamendment.pdf	252977 4f937d582cb159f9ff510c0835f2c8c6c47984a4	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment/Req. Reconsideration-After Non-Final Reject	2	2
	Specification	3	3
	Claims	4	6
	Applicant Arguments/Remarks Made in an Amendment	7	9
Warnings:			
Information:			
	Total Files Size (in bytes):	252977	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No. 276900US8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Jun HAISHIMA

SERIAL NO: 11/205,121 ART UNIT: 2114

FILING DATE: August 17, 2005 EXAMINER: P. F. CONTINO

FOR: GAMING APPARATUS HAVING MEMORY FAULT DETECTION

FEE TRANSMITTAL

■ No additional fee is required

☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.

The Fee has been calculated as shown below:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	7 - 20 =	0	x $52 =	$0.00
INDEPENDENT CLAIMS	3 - 3 =	0	x $220 =	$0.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ $390 =	$0.00
☐ LATE FILING OF DECLARATION			+ $130 =	$0.00
			BASIC FEES	$0.00
			TOTAL OF ABOVE CALCULATIONS	$0.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				$0.00
☐ FILING IN NON-ENGLISH LANGUAGE			+ $130 =	$0.00
			TOTAL	$0.00

☐ Please charge Deposit Account No. **15-0030** in the amount of ____

☐ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of ____.

■ The Director is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to Deposit Account No. **15-0030**.

■ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030.

Submitted by: _____

Bradley D. Lytle
Registration No. 40,073

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/08)

Scott A. McKeown
Registration No. 42,866

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/205,121	08/17/2005	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 01/30/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 7	Minus	** 20	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Fennell A. Pearlie/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	08/17/2005	Jun Haishima	276900US90	2910

22850 7590 04/30/2009

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
CONTINO, PAUL F	

ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
04/30/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	11/205,121	HAISHIMA, JUN	
	Examiner	Art Unit	
	PAUL F. CONTINO	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION: Final Rejection

Response to Arguments

1. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizzarri (U.S. Patent No. 5,732,268) in view of Alexander (U.S. Patent No. 6,393,559).

As in claim 1, Bizzarri teaches of an information process device *(Fig. 1 #11)* comprising:

a first memory device for storing a boot program executed when the information process device is started to operate *(column 5 lines 9-20, E-BIOS 17 boot program inherently stored in a first memory device)*;

a second memory device for storing an application program *(column 5 lines 35-36, application program code on a hard disk)*;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device and the application program stored therein *(column 6 lines 6-11)*;

wherein the fault inspection program is stored in the first memory device *(column 5 lines 9-20 and column 6 lines 6-11, E-BIOS)*; and

wherein the control device executes the fault inspection program when the information process device is started to operate *(column 5 lines 9-20 and column 6 lines 6-11, fault inspection upon booting of information processing device 11)*.

However, Bizzarri fails to expressly teach of a mother board or a second memory device connected to a mother board. Alexander teaches of a motherboard with a connected second memory device *(Fig. 2 #s18,26,28; column 2 lines 58-68, hard drive 26, disk drive 28, and BIOS memory 18)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the motherboard and memory connection as taught by Alexander in the invention of Bizzarri. This would have been obvious because the computer layout as taught by Alexander is well-known to those skilled in the art as a conventional means of laying out a computer system *(column 2 lines 61-63)*.

As in claim 2, the combined invention of Bizzarri and Alexander teaches the first memory device is a ROM provided on the mother board *(Bizzarri: column 3 lines 66-67; Alexander: Fig. 2 #18, column 2 lines 64-68)*,

wherein the second memory device is a hard disk which is independent from the mother board *(Alexander: Fig. 2 #26; column 2 line 58)*, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk *(Bizzarri: column 5 lines 30-42 and column 6 lines 5-13)*.

* * *

3. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizzarri in view of Alexander, further in view of Yamato (U.S. Patent No. 6,115,036).

As in claim 3, the combined invention of Bizzarri and Alexander teaches of an information processing device. However, the combined invention of Bizzarri and Alexander fails to teach of a gaming machine. Yamato teaches of a gaming machine for business use *(abstract, game fabrication system)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the gaming components as taught by Yamato in the combined invention of Bizzarri and Alexander because the combined invention of Bizzarri and Alexander offers a

further level of fault tolerance while booting a computer system using a BIOS in the invention of Yamato.

As in claim 4, Bizzarri teaches of a machine utilizing an information processing device *(Fig. 1 #11)*, the information process device comprising:

a first memory device for storing a boot program executed when the information process device is started to operate *(column 5 lines 9-20, E-BIOS 17 boot program inherently stored in a first memory device)*;

a second memory device configured to store an application program *(column 5 lines 35-36, application program code on a hard disk)*;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device and the application program stored therein *(column 6 lines 6-11)*;

wherein the fault inspection program is stored in the first memory device *(column 5 lines 9-20 and column 6 lines 6-11, E-BIOS)*; and

wherein the control device executes the fault inspection program every time the information process device is started to operate *(column 5 lines 9-20 and column 6 lines 6-11, fault inspection upon booting of information processing device 11)*; and

wherein when the fault does not occur in the second memory device the application program is started to execute and when the fault occurs in the second memory device an error display is conducted on a display device *(column 6 lines 10-14, normal application program loading; column 6 lines 50-53, on-screen message upon failure)*.

However, Bizzarri fails to expressly teach of a gaming machine, a game application program, a mother board or a second memory device connected to a mother board. Alexander teaches of a motherboard with a connected second memory device *(Fig. 2 #s18,26,28; column 2 lines 58-68, hard drive 26, disk drive 28, and BIOS memory 18)*. Yamato teaches of a gaming machine and a game application program *(Fig. 1A; column 26 lines 1-14 [game application program] and 54-57)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the motherboard and memory connection as taught by Alexander in the invention of Bizzarri. This would have been obvious because the computer layout as taught by Alexander is well-known to those skilled in the art as a conventional means of laying out a computer system *(column 2 lines 61-63)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the gaming components as taught by Yamato in the combined invention of Bizzarri and Alexander because the combined invention of Bizzarri and Alexander offers a further level of fault tolerance while booting a computer system using a BIOS in the invention of Yamato.

As in claim 5, the combined invention of Bizzarri and Alexander teaches the first memory device is a ROM provided on the mother board *(Bizzarri: column 3 lines 66-67; Alexander: Fig. 2 #18, column 2 lines 64-68)*,

wherein the second memory device is a hard disk which is independent from the mother board *(Alexander: Fig. 2 #26; column 2 line 58)*, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk *(Bizzarri: column 5 lines 30-42 and column 6 lines 5-13)*.

As in claim 6, Yamato teaches of a RAM provided on the mother board *(Fig. 2A)*;

wherein the game application program is loaded from the hard disk to the RAM and executed by the control device when the fault does not occur in the hard disk *(Chang: paragraph [0002] hard disk; Yamoto: column 5 lines 36-37, program from disk 8 to RAM 4)*.

* * *

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizzarri in view of Alexander, further in view of Krau (U.S. Patent No. 5,864,698).

As in claim 7, Bizzarri teaches of an information process device *(Fig. 1 #11)* comprising:

a first memory device for storing a boot program executed when the information process device is started to operate *(column 5 lines 9-20, E-BIOS 17 boot program inherently stored in a first memory device)*;

a second memory device for storing an application program *(column 5 lines 35-36, application program code on a hard disk)*;

a control device for executing a fault inspection program to inspect whether or not a fault occurs in the second memory device and the application program stored therein *(column 6 lines 6-11)*;

wherein the fault inspection program is stored in the first memory device *(column 5 lines 9-20 and column 6 lines 6-11, E-BIOS)*; and

wherein the control device executes the fault inspection program when the information process device is started to operate *(column 5 lines 9-20 and column 6 lines 6-11, fault inspection upon booting of information processing device 11)*.

However, Bizzarri fails to expressly teach of a mother board or a second memory device connected to a mother board, or execution of a BIOS on a second memory device. Alexander teaches of a motherboard with a connected second memory device *(Fig. 2 #s18,26,28; column 2 lines 58-68, hard drive 26, disk drive 28, and BIOS memory 18)*. Krau teaches of a BIOS initialized on a second memory device upon execution of a boot program *(column 1 lines 55-62, balance of BIOS on second memory hard disk)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the motherboard and memory connection as taught by Alexander in the invention of Bizzarri. This would have been obvious because the computer layout as taught by Alexander is well-known to those skilled in the art as a conventional means of laying out a computer system *(column 2 lines 61-63)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the BIOS layout as taught by Krau in the combined invention of Bizzarri and Alexander. This would have been obvious because Krau teaches of storing portions of a

BIOS in both a ROM and a hard disk in order to reduce the space available for applications *(column 1 lines 55-66)*, which, when coupled with the BIOS execution as taught by Bizzarri, would execute the BIOS before fault inspection.

Conclusion

5. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL F. CONTINO whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit 2114

PFC
20 April 2009

Notice of References Cited	Application/Control No. 11/205,121	Applicant(s)/Patent Under Reexamination HAISHIMA, JUN	
	Examiner PAUL F. CONTINO	Art Unit 2114	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,732,268	03-1998	Bizzarri, Maurice W.	713/2
*	B	US-5,864,698	01-1999	Krau et al.	713/2
*	C	US-6,393,559	05-2002	Alexander, Marc D.	713/2
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11205121	HAISHIMA, JUN
	Examiner	Art Unit
	PAUL F. CONTINO	2114

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/25/2008	10/28/2008	04/20/2009						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4		✓	✓						
	5		✓	✓						
	6		✓	✓						
	7			✓						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11205121	HAISHIMA, JUN
	Examiner	Art Unit
	PAUL F. CONTINO	2114

SEARCHED

Class	Subclass	Date	Examiner
714	36	10/28/2008	PFC
710	104	10/28/2008	PFC

SEARCH NOTES

Search Notes	Date	Examiner
Previous Examiner's prosecution history	10/28/2008	PFC
714/2,3,5 - text search - see included search history	10/28/2008	PFC
Inventor search	10/28/2008	PFC
SEARCHED subclasses updated	4/16/2009	PFC

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S20	105	(bios) with (hard adj (disk disc drive) harddisk harddrive harddisc) with (fault$3 corrupt$4 error erroneous fail $3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/16 10:11
S19	259	(bios) with (hard adj (disk disc drive) harddisk harddrive harddisc) same (fault$3 corrupt$4 error erroneous fail $3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/16 10:10
S18	1669	714/36.ccls. 710/104.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/16 10:04
S17	2916	713/2.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/16 10:04
S16	319	714/27.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/16 10:03

4/20/09 10:52:59 AM
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\ 11_205121.wsp

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	08/17/2005	Jun Haishima	276900US90	2910

22850 7590 07/21/2009

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
CONTINO, PAUL F	

ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
07/21/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Interview Summary	Application No.	Applicant(s)	
	11/205,121	HAISHIMA, JUN	
	Examiner	Art Unit	
	PAUL F. CONTINO	2114	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Paul F. Contino (Examiner)*. (3)_____.

(2) *Derek P. Benke (Attorney)*. (4)_____.

Date of Interview: *16 July 2009*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☐ applicant 2)☒ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *All*.

Identification of prior art discussed: *Bizarri (U.S. Patent 5,732,268)*.

Agreement with respect to the claims f)☐ was reached. g)☐ was not reached. h)☒ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *The Examiner and the Applicant discussed the 103 rejection and applied prior art references. No agreement was reached with respect to the claims*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

/Paul F. Contino/ Patent Examiner	16 July 2009

DOCKET NO: 276900US8

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
JUN HAISHIMA	: EXAMINER: CONTINO, P.
SERIAL NO: 11/205,121	:
FILED: AUGUST 17, 2005	: GROUP ART UNIT: 2114
FOR: INFORMATION PROCESS DEVICE	:

AMENDMENT UNDER 37 C.F.R. §1.116

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action dated April 30, 2009, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): [[An]] A gaming device configured to execute a game, the gaming ~~information process~~ device comprising:

a first memory device for storing a boot program executed when the gaming ~~information process~~ device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing [[an]] a game application program for the game, the second memory device being connected to the mother board; and

a control device for executing a fault inspection program for the gaming device to inspect whether or not a fault occurs in the second memory device and the game application program stored therein,

wherein the fault inspection program is stored in the first memory device[[;]], and the control device executes the fault inspection program when the gaming device is started to operate and completes the execution of the fault inspection program before the game is started.

Claim 2 (Currently Amended): The gaming ~~information process~~ device according to claim 1, wherein the first memory device is a ROM provided on the mother board,

wherein the second memory device is a hard disk which is independent from the mother board, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk.

Claim 3 (Currently Amended): The ~~information process~~ gaming device according to claim 1, wherein the ~~information process device is utilized as a~~ gaming machine is configured for business use.

Claim 4 (Currently Amended): A gaming ~~machine utilizing an information process~~ device configured to execute a game, the ~~information process~~ gaming device comprising:

a first memory device configured to store a boot program executed when the information process device of the gaming machine is started to operate;

a mother board on which the first memory device is provided;

a second memory device configured to store a game application program, the second memory device being connected to the mother board and electrically rewritable;

a control device configured to execute a fault inspection program to inspect whether or not a fault occurs in the second memory device and the game application program stored therein;

wherein the fault inspection program is stored in the first memory device[[;]], and ~~wherein~~ the control device executes the fault inspection program every time the information process device is started to operate and completes the execution of the fault inspection program before the game is started, and

wherein when the fault does not occur in the second memory device the game application program is started to execute and when the fault occurs in the second memory device an error is displayed ~~display is conducted~~ on a display device located on the exterior of the gaming machine.

Claim 5 (Currently Amended): The gaming device ~~machine~~ according to Claim 4, wherein the first memory device is a ROM provided on the mother board,

wherein the second memory device is a hard disk which is independent from the mother board, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk.

Claim 6 (Currently Amended): The gaming device ~~machine~~ according to Claim 5, further comprising:

a RAM provided on the mother board;

wherein the game application program is loaded from the hard disk to the RAM and executed by the control device when the fault does not occur in the hard disk.

Claim 7 (Currently Amended): [[An]] A gaming device configured to execute a game, the gaming ~~information process~~ device comprising:

a first memory device for storing a boot program executed when the gaming ~~information process~~ device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing [[an]] a game application program for the game and a BIOS, the second memory device being connected to the mother board; and

a control device for executing a fault inspection program for the gaming device to inspect whether or not a fault occurs in the second memory device and the game application program stored therein;

wherein the fault inspection program is stored in the first memory device,[[;]] and ~~wherein~~ the control device executes the boot program to initialize the BIOS stored in the second memory device before executing the fault inspection program when the ~~information~~

~~process~~ gaming device is started to operate, and completes the execution of the fault inspection program before the game is started.

Claim 8 (New): The gaming device according to claim 1, wherein the first memory device and the mother board are located in the information process device.

Claim 9 (New): The gaming device according to claim 1, wherein the second memory device is a flash memory.

Claim 10 (New): The gaming device according to Claim 4, wherein the display device is a liquid crystal display.

REMARKS

Favorable reconsideration of this application as presently amended, and in light of the following discussion, is respectfully requested.

Claims 1-10 are pending in this application, Claims 8-10 having been added; and Claims 1-7 having been currently amended. Amended Claims 1-7 and new Claims 8-10 find non-limiting support in the disclosure as originally filed, for example at page 6, lines 1-11 and 27-30, and Fig. 1. No new matter has been added.

In the outstanding Office Action, Claims 1 and 2 were rejected under 35 U.S.C. §103(a) as unpatentable over Bizzari (U.S. Patent No. 5,732,268) in view of Alexander (U.S. Patent No. 6,393,559); Claims 3-6 were rejected under 35 U.S.C. §103(a) as unpatentable over Bizzari in view of Alexander and Yamamoto (U.S. Patent No. 6,115,036); and Claim 7 was rejected under 35 U.S.C. §103(a) as unpatentable over Bizzari in view of Alexander and Krau (U.S. Patent No. 5,864,698).

Applicant acknowledges with appreciation the courtesy of Examiner Contino in granting an interview in this case with Applicant's representative on July 16, 2009, during which time the issues in the outstanding Office Action were discussed as substantially summarized hereinafter and also on the Interview Summary Sheet. No agreement was reached during the interview pending a formal response to the outstanding Office Action.

In response to the rejections under 35 U.S.C. §103(a), Applicant respectfully submits that amended independent Claim 1 recites novel features clearly not taught or rendered obvious by the applied references.

Independent Claim 1 is directed to a gaming device including, *inter alia*:

> ... a first memory device for storing a boot program executed when the gaming device is started to operate;
>
> a mother board on which the first memory device is provided;

> a second memory device for storing a game application program for the game, the second memory device being connected to the mother board; and
>
> a control device for executing a fault inspection program for the gaming device to inspect whether or not a fault occurs in the second memory device and the game application program stored therein,
>
> wherein the fault inspection program is stored in the first memory device, and the control device executes the fault inspection program when the gaming device is started to operate and completes the execution of the fault inspection program before the game is started.

Page 3 of the outstanding Office Action asserts that column 5, lines 35-36 of Bizzari describes a "second memory device for storing an application program, the second memory device being connected to the mother board," as recited in Applicant's Claim 1. Column 5, lines 29-42 of Bizzari states:

> There are a number of possible reasons why an E-BIOS PC might fail to boot. Perhaps chief among these, without regard to importance, are (1) a physical failure of the boot drive, (2) code corruption in the boot sector of the boot drive, (3) corruption of the file allocation table (FAT), (4) BIOS setup corrupted (usually in real-time clock, and often called CMOS), and (5) a virus infection affecting code and/or data in CMOS or on a hard disk. In case (1) the necessary correction cannot be made from the remote location, and it is necessary to send a technician to the failed computer to physically repair or change out the offending drive. In the cases of (2), (3), (4), and (5) diagnosis and repair can be made by methods of the present invention.

Thus, the above portion of Bizzari merely describes possible reasons for why an E-BIOS PC might fail to boot, and describes that a virus infection affecting code and/or data on a hard disk could be a possible reason for failure. However, Bizzari does not describe that the hard disk stores a game application program and that the hard disk is connected to a mother board. Bizzari merely describes that the hard disk contains code and/or data, but does not describe that the code or data is an application program for a game.

In addition, pages 2 and 3 of the outstanding Office Action assert that the E-BIOS in Bizzari is equivalent to both of Applicant's claimed fault inspection program and boot program. However, in Applicant's Claim 1, the boot program and the fault inspection program are distinct. Further, Bizzari fails to suggest "a control device for executing a fault inspection program for the gaming device to inspect whether or not a fault occurs in the second memory device and the game application program stored therein," as recited in Claim 1. As described above, Bizzari does not describe a game application program stored in the hard disk of Bizzari. In addition, Bizzari merely describes that there are a number of possible reasons why the E-BIOS might fail to boot, but does not describe a device which executes a fault inspection program to inspect whether or not a fault occurs in the hard disk and a game application program stored in the hard disk.

Turning now to Yamamoto, Yamamoto is directed to a videographics/video game fabricating system including a multiprocessor based game processor console. Column 26, lines 6-14 of Yamamoto states:

> The main CPU 228 executes various utility programs, operating system, peripheral driver programs, and BIOS and IPL software. The utility software operated by the main CPU 228 includes game editing tools, network software, word processing software, disk management software, etc.

However, Yamamoto also fails to teach or suggest "a second memory device for storing a ***game application program*** for the game, the second memory device being connected to the mother board; and a control device for executing ***a fault inspection program for the gaming device to inspect whether or not a fault occurs in the second memory device and the game application program*** stored therein." Lastly, Applicant respectfully submits that Yamamoto does not describe that a "control device executes the fault inspection program when the gaming device is started to operate and completes the execution of the fault inspection program ***before the game is started***," as recited in Claim 1.

Accordingly, Applicant respectfully submits that independent Claim 1 (and all claims depending thereon) patentably distinguishes over Bizzari in view of Yamamoto. Further, Applicant submits that Alexander and Krau fail to cure any of the above-noted deficiencies of Bizzari and Yamamoto.

Independent Claim 4 recites that "the control device executes the fault inspection program every time the information process device is started to operate and completes the execution of the fault inspection program before the game is started," and is believed to be patentable for at least the reasons discussed above. Accordingly, Applicant respectfully submits that independent Claim 4 (and all claims depending thereon) patentably distinguishes over the above cited references.

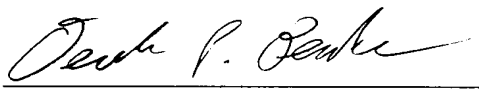
Independent Claim 7 recites that "the control device executes the boot program to initialize the BIOS stored in the second memory device before executing the fault inspection program when the gaming device is started to operate, and completes the execution of the fault inspection program before the game is started," and is also believed to be patentable for at least the reasons discussed above.

Accordingly, Applicant respectfully requests that the rejections under 35 U.S.C. §103 be withdrawn.

Consequently, in view of the present amendment, and in light of the above discussion, the pending claims as presented herewith are believed to be in condition for formal allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Bradley D. Lytle
Attorney of Record
Registration No. 40,073

Derek P. Benke
Registration No. 56,944

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/07)

1265081_2.DOC

Electronic Acknowledgement Receipt

EFS ID:	5802077
Application Number:	11205121
International Application Number:	
Confirmation Number:	2910
Title of Invention:	Information process device
First Named Inventor/Applicant Name:	Jun Haishima
Customer Number:	22850
Filer:	Marvin Jay Spivak/Kim Rouse
Filer Authorized By:	Marvin Jay Spivak
Attorney Docket Number:	276900US90
Receipt Date:	30-JUL-2009
Filing Date:	17-AUG-2005
Time Stamp:	16:22:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		276900USAMENDMENT.PDF	402873 1f09494611b47064c6ac274e8fa246b69b620902	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment After Final	2	2
	Claims	3	6
	Applicant Arguments/Remarks Made in an Amendment	7	11
Warnings:			
Information:			
	Total Files Size (in bytes):	402873	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No. 276900US8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Jun HAISHIMA

SERIAL NO: 11/205,121 ART UNIT: 2114

FILING DATE: August 17, 2005 EXAMINER: CONTINO, P.

FOR: INFORMATION PROCESS DEVICE

FEE TRANSMITTAL

■ No additional fee is required

☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.

The Fee has been calculated as shown below:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	10 - 20 =	0	x $52 =	$0.00
INDEPENDENT CLAIMS	3 - 3 =	0	x $220 =	$0.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ $390 =	$0.00
☐ LATE FILING OF DECLARATION			+ $130 =	$0.00
			BASIC FEES	$0.00
			TOTAL OF ABOVE CALCULATIONS	$0.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				$0.00
☐ FILING IN NON-ENGLISH LANGUAGE			+ $130 =	$0.00
			TOTAL	$0.00

☐ Please charge Deposit Account No. **15-0030** in the amount of **$0.00**

☐ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **$0.00**.

■ The Director is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to Deposit Account No. **15-0030**.

■ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030.

Submitted by: Derek P. Benke

Bradley D. Lytle
Registration No. 40,073

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/08)

Derek P. Benke
Registration No. 56,944

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/205,121	08/17/2005	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	300

APPLICATION AS AMENDED – PART II

AMENDMENT 07/30/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/TAMMY MCBETH BROWN/

DOCKET NO: 276900US8

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
JUN HAISHIMA	: EXAMINER: CONTINO, P.
SERIAL NO: 11/205,121	:
FILED: AUGUST 17, 2005	: GROUP ART UNIT: 2114
FOR: INFORMATION PROCESS DEVICE	:

Please DO NOT ENTER
/dml/
8/15/09

AMENDMENT UNDER 37 C.F.R. §1.116

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action dated April 30, 2009, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	08/17/2005	Jun Haishima	276900US90	2910

22850 7590 08/19/2009

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
LE, DIEU MINH T

ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
08/19/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 11/205,121	**Applicant(s)** HAISHIMA, JUN	
	Examiner Dieu-Minh Le	**Art Unit** 2114	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 30 July 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *The newly proposed limitations that "completes the execution of the fault inspection program before the game is started" [added in claims 1,4 & 7] have not been previously claimed. These limitations would require further consideration/search*. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: *none*.
   Claim(s) objected to: *none*.
   Claim(s) rejected: *1-7*.
   Claim(s) withdrawn from consideration: *none*.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Dieu-Minh Le/
Primary Examiner, Art Unit 2114

Docket No.: 276900US8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jun HAISHIMA

SERIAL NO:	11/205,121	GAU:	2114
FILED:	August 17, 2005	EXAMINER:	LE, D.M.
FOR:	INFORMATION PROCESS DEVICE		

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is a Request for Continued Examination (RCE) under 37 C.F.R. §1.114 of the above-identified application.

Submission required under 37 C.F.R. §1.114

Previously Submitted:

- ■ Consider the amendment(s)/reply under 37 C.F.R. §1.116 previously filed on July 30, 2009
- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on

Enclosed:

- ☐ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ■ Other: Request for Extension of Time (1 month)

FEES	RATE	CALCULATIONS
☐ Suspension of action on the above-identified application is requested under 37 C.F.R. §1.103(c) for a period of months.	$130.00	$0.00
■ RCE Fee required under 37 C.F.R. §1.17(e)	$810.00	$810.00
■ **A ONE MONTH EXTENSION OF TIME IS REQUESTED**		$130.00
☐		$0.00
TOTAL OF ABOVE CALCULATIONS:		$940.00
☐ REDUCTION BY 50% FOR FILING AS SMALL ENTITY		$0.00
TOTAL:		$940.00

■ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of **$940.00.**

■ Please charge any additional Fees for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to Deposit Account No. **15-0030**.

■ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 CFR 1.136, and any additional fees required under 37 CFR 1.136 for any necessary extension of time may be charged to Deposit Account No. **15-0030**.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

Bradley D. Lytle
Registration No. 40,073

Derek P. Benke
Registration No. 56,944

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 07/09)

Docket No. 276900US8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jun HAISHIMA

SERIAL NO:	11/205,121	GAU:	2114
FILED:	August 17, 2005	EXAMINER:	LE, D.M.
FOR:	INFORMATION PROCESS DEVICE		

REQUEST FOR EXTENSION OF TIME UNDER 37 C.F.R. 1.136

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

It is hereby requested that a **one** month extension of time be granted to August 30, 2009 for

☐ filing a response to the Official Action dated:

☐ responding to the requirements in the Notice of Allowability dated:

☐ filing the Formal Drawings. The Issue Fee due has been timely filed.

☐ responding to the Notice to File Missing Parts of Application dated:

■ filing a Request for Continued Examination (RCE). A response to the final rejection was filed on July 30, 2009.

☐ filing an Appeal Brief. A Notice of Appeal was filed on:

☐ Applicant claims small entity status. See 37 CFR 1.27.

The required fee of $130.00 is being made by credit card payment online (if electronically filed), or is attached hereto (if paper filed), and any further charges may be made against the Attorney of Record's Deposit Account No. **15-0030**.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

Bradley D. Lytle
Registration No. 40,073

Derek P. Benke
Registration No. 56,944

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 07/09)

Electronic Patent Application Fee Transmittal

Application Number:	11205121
Filing Date:	17-Aug-2005
Title of Invention:	Information process device
First Named Inventor/Applicant Name:	Jun Haishima
Filer:	Marvin Jay Spivak/Kim Rouse
Attorney Docket Number:	276900US90

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	130	130

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**940**

Electronic Acknowledgement Receipt

EFS ID:	5959566
Application Number:	11205121
International Application Number:	
Confirmation Number:	2910
Title of Invention:	Information process device
First Named Inventor/Applicant Name:	Jun Haishima
Customer Number:	22850
Filer:	Marvin Jay Spivak/Kim Rouse
Filer Authorized By:	Marvin Jay Spivak
Attorney Docket Number:	276900US90
Receipt Date:	26-AUG-2009
Filing Date:	17-AUG-2005
Time Stamp:	17:08:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$940
RAM confirmation Number	3476
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		276900USRCE.PDF	82403 f38be8b90a9fccb6a722cad20ace24c8530ba229	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Request for Continued Examination (RCE)	1	1
	Extension of Time	2	2

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	31862 979737fb1c38774e7816bc9620f6389a057b9171	no	2

Warnings:

Information:

Total Files Size (in bytes):	114265

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/205,121	08/17/2005	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	08/26/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Debra R. Wyatt/

Entered/WRCE
8-26-09
Bwyatt
8-28-09

DOCKET NO: 276900US8

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
JUN HAISHIMA	: EXAMINER: CONTINO, P.
SERIAL NO: 11/205,121	:
FILED: AUGUST 17, 2005	: GROUP ART UNIT: 2114
FOR: INFORMATION PROCESS DEVICE	:

~~Please DO NOT ENTER~~
/dm1/
8/15/09

AMENDMENT UNDER 37 C.F.R. §1.116

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action dated April 30, 2009, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22850 7590 09/25/2009

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
LE, DIEU MINH T	
ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/25/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	08/17/2005	Jun Haishima	276900US90	2910

TITLE OF INVENTION: INFORMATION PROCESS DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/28/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22850 7590 09/25/2009

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	08/17/2005	Jun Haishima	276900US90	2910

TITLE OF INVENTION: INFORMATION PROCESS DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/28/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DIEU MINH T	2114	714-036000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	08/17/2005	Jun Haishima	276900US90	2910

22850 7590 09/25/2009

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
LE, DIEU MINH T	
ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/25/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 510 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 510 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/205,121	HAISHIMA, JUN	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the communication filed 8/26/09*.

2. ☒ The allowed claim(s) is/are *1-10*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Dieu-Minh Le/
Primary Examiner, Art Unit 2114

Notice of References Cited	Application/Control No. 11/205,121	Applicant(s)/Patent Under Reexamination HAISHIMA, JUN	
	Examiner Dieu-Minh Le	Art Unit 2114	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,011,564	01-2000	Furuhashi et al.	345/501
*	B	US-5,701,478	12-1997	Chen, Yi-Rong	713/2
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L20	837	(boot$3 bios initializ$5) with (program$5 software application) with game	USPAT; UPAD	OR	ON	2009/09/22 11:56
L21	3168	(fault$3 error$3 fail$3 corrupt$3 problem malfunction defect $3 bug) with inspect$3 with (program application)	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 11:56
L22	349466	(inspect$3 check $3 monitor$3 track$3) with (program application)	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:01
L23	68574	(rom eprom eeprom harddisk harddrive harddisc hard-disk hard-drive hard-disc "hard disc" "hard drive" "hard disk" "mother board") same (fault$3 error$5 fail$3 corrupt$3 problem malfunction defect $3 bug$4)	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:01
L24	432	(714/36).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:02

L25	372	(714/27).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:02
L26	382	(714/3).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:02
L27	1517	(714/5).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:02
L28	432	(714/36).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:03
L29	1702	(714/47).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:03
L30	1566	(714/48).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:03
L31	3413	(713/2).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:03
L32	1363	(710/104).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:03
L33	0	20 and 21	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:04
L34	322	21 and 22 and 23	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:05
L35	0	34 and 20 and (24 25 26 27 28)	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:05

L36	0	34 and 20 and (29 30 31 32)	US-PGPUB; USPAT; UPAD	OR	ON	2009/09/22 12:06
L37	0	((boot$3 bios initializ$5) same (program$5 software application) same (gam$3 vediogam $3)) and 34 and ("714"/$.ccls.)	USPAT; UPAD	OR	ON	2009/09/22 12:07
L38	0	((boot$3 bios initializ$5) same (program$5 software application) same (gam$3 vediogam $3)) and 34 and ("710"/$.ccls.)	USPAT; UPAD	OR	ON	2009/09/22 12:08
L39	0	((boot$3 bios initializ$5) same (program$5 software application) same (gam$3 vediogam $3)) and 34 and ("713"/$.ccls.)	USPAT; UPAD	OR	ON	2009/09/22 12:08

9/22/09 12:08:31 PM
C:\Documents and Settings\MLe\My Documents\EAST\Workspaces\11205121.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11205121	HAISHIMA, JUN
	Examiner	Art Unit
	PAUL F. CONTINO	2114

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/25/2008	10/28/2008	04/20/2009	09/22/2009					
1	1	✓	✓	✓	=					
2	2	✓	✓	✓	=					
3	3	✓	✓	✓	=					
6	4		✓	✓	=					
7	5		✓	✓	=					
8	6		✓	✓	=					
10	7			✓	=					
4	8				=					
5	9				=					
9	10				=					

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11205121	HAISHIMA, JUN
	Examiner	**Art Unit**
	PAUL F. CONTINO	2114

SEARCHED

Class	Subclass	Date	Examiner
714	36,27,3,5,47	9/22/09	dml
710	104	9/22/09	dml
713	2	9/22/09	dml

SEARCH NOTES

Search Notes	Date	Examiner
EAST search all files USPAT, USPGPUBM USOCR, FPRS, EPO, JPO, DERWENT, IBM-TDB updated	9/22/09	dml
NPL search [IEEE, Google Advanced Search]	9/22/09	dml
Inventor search	9/22/09	dml
SEARCHED subclasses updated	9/22/09	dml

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
714	36,27,3,5,47	9/22/09	dml
710	104	9/22/09	dml
713	2	9/22/09	dml

	/Dieu-Minh Le/ Primary Examiner.Art Unit 2114

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	41083	(inspect$3 check$3 monitor $3 track$3) adj (program application)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:37
L8	1893	(boot$3 bios initializ$5) with (program$5 software application) with game	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:41
L9	102850	(rom eprom eeprom harddisk harddrive harddisc hard-disk hard-drive hard-disc "hard disc" "hard drive" "hard disk" "mother board") same (fault$3 error$5 fail$3 corrupt$3 problem malfunction defect$3 bug $4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:41
L10	25	L9 same L8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:41
L11	2	7 and L10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:41
L12	12060	(before ahead prior previous) with (gam$3 vediogam$3) with (start$3 begin$4 operat$3 execut$3 run$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:46
L14	7	(haishima-jun$).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:50

L15	3149	(713/2).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:51
L16	1336	(710/104).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:52
L17	1242	(710/36).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:52
L18	169	(710/27).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:52
L19	3718	(714/27,36,47,48).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 11:53
S1	20	("20040078697" | "20050246586" | "20070168738" | "5732268" | "5860122" | "5864698" | "5971851" | "6115036" | "6393559" | "6449735").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 14:32
S2	180	(fault$3 error$3 fail$3 problem malfunction defect $3 bug) near2 inspect$3 near (program application)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 14:34
S3	20235	(complet$3 finish$3 done) same game same (start$3 operat$3 execut$3 operat $3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 14:35

S4	0	S2 same S3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 14:35
S5	0	S2 and S3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 14:36
S6	419	(714/36).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 14:36
S7	358	(714/27).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 14:36
S8	7130	(714/3,5,38,47,48).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 14:38
S9	1893	(boot$3 bios initializ$5) with (program$5 software application) with game	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:28
S10	102850	(rom eprom eeprom harddisk harddrive harddisc hard-disk hard-drive hard-disc "hard disc" "hard drive" "hard disk" "mother board") same (fault$3 error$5 fail$3 corrupt$3 problem malfunction defect$3 bug $4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:41
S11	25	S10 same S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:44

S12	180	(fault$3 error$3 fail$3 problem malfunction defect $3 bug) near2 inspect$3 near (program application)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:45
S13	0	S11 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:45
S14	4385	(fault$3 error$3 fail$3 corrupt$3 problem malfunction defect$3 bug) with inspect$3 with (program application)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:46
S15	0	S11 and S14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:46
S16	48801	inspect$3 with (program application)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:47
S17	0	S11 and S16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:47
S18	409730	(inspect$3 check$3 monitor $3 track$3) with (program application)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:47
S19	22	S11 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:55
S20	22	S19 and (gam$3 videogam $3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:56

9/22/09 11:55:27 AM
C:\Documents and Settings\MLe\My Documents\EAST\Workspaces\11205121.wsp

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BIB DATA SHEET

CONFIRMATION NO. 2910

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/205,121	08/17/2005	714	2114	276900US90

APPLICANTS
Jun Haishima, Tokyo, JAPAN;

**** CONTINUING DATA **************************** na dml

**** FOREIGN APPLICATIONS ****************************
JAPAN 2004-245337 08/25/2004 yes dml

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
09/02/2005

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /DIEU-MINH T LE/ Examiner's Signature	☐ Met after Allowance dml Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	3	13 10	1 3

ADDRESS

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314
UNITED STATES

TITLE

Information process device

FILING FEE RECEIVED		
1000	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11205121	HAISHIMA, JUN
	Examiner	**Art Unit**
	Dieu-Minh Le	2114

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
714	36	G 0 6 F 11 / 00 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
713	2				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
6	4														
7	5														
8	6														
10	7														
4	8														
5	9														
9	10														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	10	
/Dieu-Minh Le/ Primary Examiner.Art Unit 2114	09/22/2009	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Web Results **11** - **20** of about **26,300** for **memory stored boot program control device completed executing fault inspection program before game started**. (**0.38** seconds)

Show options...

1. [PDF] Malicious Code Detection for Open Firmware

File Format: PDF/Adobe Acrobat - View

started. **Boot** firmware is the **program** that controls this pro- **...** eral **devices**. The **boot program** runs **before** the operating **....** that represents this **device**. That fcode **program** is **stored** in **.....** ensure the basic properties of **memory**, **control** flow, and **.....** Towards **fault**-tolerant and secure agen- try. In Proc. **...**
www.cs.cornell.edu/~kozen/papers/acsac.pdf - Similar
by F Adelstein - 2002 - Cited by 13 - Related articles

2. Embedded **Control** Systems Design/Operating systems - Wikibooks **...**

Apr 11, 2009 **...** An operating system is a computer **program** that manages the hard and **...** as we first **start** with a more general approach of operating systems. **....** appear are perhaps a divide by zero, a **memory** segmentation **fault**, etc. **....** Namespace: **before** writing any code it is important to name your **device**. **Memory ...**
en.wikibooks.org/wiki/...**Control**.../Operating_systems - Cached - Similar

3. [PDF] **Fault**-Tolerant Systems in A Space Environment: The CRC ARGOS **...**

File Format: PDF/Adobe Acrobat - View as HTML

(**executing** pieces of code two or more times), assigned signature **control** flow **...** that stores the **boot program** and the operating system in a compressed format. **....** This **complete** information will be given to the Collector to be **stored** and **.....** modern operating systems take advantage of that for **memory** protection. **...**
ftp://reports.stanford.edu/pub/cstr/reports/csl/.../CSL-TR-98-774.pdf - Similar
by PP Shirvani - Related articles - All 11 versions

4. Backup Encyclopedia:: V

Program code and data are **stored** in random access **memory** (RAM) chips - also known **...** copy the least recently used pages of **memory** to the hard disk drive, even **before** an **...** to reflect the virtual address space of the currently **executing** processes, **...** The Volume **Boot** Record (also known as the Volume **Boot** Sector or **...**
www.backupencyclopedia.com/glossary/v/v.html - Cached - Similar

5. [PDF] BodySnatcher: Towards reliable volatile **memory** acquisition by software

File Format: PDF/Adobe Acrobat - View as HTML

liably acquiring host **memory** by snatching **complete control ...** configured to be used as a **memory** acquisition **device. ...** contents of **memory** are **stored** in a file. Such **memory ....** tion OS executor into **memory**, then **executing** the acquisition **...** Switching **program** flow from the host OS kernel to the acqui- **...**

www.dfrws.org/2007/proceedings/p126-schatz.pdf - Similar

by B Schatz - Cited by 10 - Related articles - All 5 versions

6. [PDF] TransmetaTM CrusoeTM Hardware, Software, and Development Abstract ...

File Format: PDF/Adobe Acrobat - View

der software **control**, allowing an individual operation to **..... memory** is **stored** in a target-only part of host RAM. Sec- **...** dled by **executing** instructions one-at-a-time until the **fault .....** grade requires **boot** in a minute or less. Crusoe is tuned to **...** was during **program start** when exceptions were frequent. **...**

arnas-bt.cs.virginia.edu/2009proceedings/3-keppel-paper.pdf - Similar

7. [PDF] /tardir/tiffs/a416770.tiff

File Format: PDF/Adobe Acrobat - View as HTML

safe **memory** management options. **Before**, we had to restrict programmers **...** to **execute**, and this decision is beyond the programmers **control**. Nonde- **...** is called **boot** firmware and is typically **stored** in ROM or other non-volatile **memory**. **...** typically **device** drivers, will be loaded into the **boot program** and must **...**

handle.dtic.mil/100.2/ADA416770 - Similar

by FB Schneider - 2003 - Cited by 2 - Related articles - All 7 versions

8. [PDF] INSTALLATION GUIDE System Console Software 2.0

File Format: PDF/Adobe Acrobat - View

The unit of the **program** in which the system is composed is called the package. **...** information for system **fault** analysis to a backup tape **device**. **....** 0.7 Using the **memory** error **inspection** function. (Solaris 7/Solaris 8 **.... Execute** the following command to **start** the daemon. **...** All uninstallation **completed**. **...**

sysdoc.doors.ch/FUJITSUSIEMENS/scs_2_0_inst.pdf - Similar

9. [PDF] The Parallel Board Tester Combining Parallel Boundary-Scan and ...

File Format: PDF/Adobe Acrobat - View as HTML

and test software **executing** on the test objects. The test setup **... boot program** via boundary- scan. This **boot** is an in- **...** The EBoot is **stored** in flash **memory** and the DEST in RAM. **.....** advanced quality **control**, it would be possible to skip the ICT test. **...** ports to a presentation and storing system saves **fault- ...**

www.molesystems.com/.../Parallel%20Board%20Tester%20(3.2).pdf - Similar

10. Computer Programming Software Terms, Glossary and Dictionary - D ...

The Daemon **program**, often **started** at the time the system boots and runs

continuously without **...** as bits and bytes **stored** in electronic **memory**, or as facts **stored** in a person's mind. **...** Data elements usage can be discovered by **inspection** of software **....** create and remove breakpoints, and **execute** your **program**. **...**
www.networkdictionary.com/software/d.php - Cached - Similar

Tip: These results **do not include** the word "game". Show results that include "game".

Gooooooooooogle
Previous 1 2 3 4 5 6 7 8 9 10 11 Next

memory stored boot program control device completed executing fault inspectio Search

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Edit an existing query or compose a new query in the Search Query Display.

Select a search number (#) to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Tue, 22 Sep 2009, 1:48:46 PM EST

Search Query Display

Run Search | Reset

Recent Search Queries		Results
#1	(((boot program executed)<in>metadata) <and> ((fault occurs second memory)<in>metadata))<and> ((before game started) <in>metadata)	0
#2	(((boot program executed)<in>metadata) <and> ((fault occurs second memory)<in>metadata))<and> ((before game started) <in>metadata)	0
#3	(((fault inspection program)<in>metadata) <and> ((error display)<in>metadata))<and> ((exterior gaming machine) <in>metadata)	0
#4	(((fault inspection program)<in>metadata) <and> ((stored mother board)<in>metadata))<and> ((executed before game started)<in>metadata)	0
#5	(((boot program)<in>metadata) <and> ((control device) <in>metadata))<and> ((fault inspection program) <in>metadata)	0
#6	(((bios harddisk)<in>metadata) <and> ((fault inspection program)<in>metadata))<and> ((before game started) <in>metadata)	0

Clear Session History

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Bib Data Sheet

CONFIRMATION NO. 2910

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/205,121	08/17/2005 RULE	714	2114	276900US90

APPLICANTS
Jun Haishima, Tokyo, JAPAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS *********************
JAPAN 2004-245337 08/25/2004

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 09/02/2005

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☒ yes ☐ no	JAPAN	3	3	1
35 USC 119 (a-d) conditions met ☒ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials				

ADDRESS
22850

TITLE
Gaming apparatus having memory fault detection

FILING FEE RECEIVED		
1000	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

10/13/09

Docket No.: 276900US8/jkl

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jun HAISHIMA

SERIAL NUMBER: 11/205,121 GROUP: 2114

FILED: August 17, 2005 EXAMINER: LE, DIEU MINH T.

FOR: **GAMING APPARATUS HAVING MEMORY FAULT DETECTION**

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. § 1.312

MAIL STOP ISSUE FEE
COMMISSIONER FOR PATENTS
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SIR:

In response to the Notice of Allowability dated September 25, 2009, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Previously Presented): A gaming device configured to execute a game, the gaming device comprising:

a first memory device for storing a boot program executed when the gaming device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing a game application program for the game, the second memory device being connected to the mother board; and

a control device for executing a fault inspection program for the gaming device to inspect whether or not a fault occurs in the second memory device and the game application program stored therein,

wherein the fault inspection program is stored in the first memory device, and the control device executes the fault inspection program when the gaming device is started to operate and completes the execution of the fault inspection program before the game is started.

Claim 2 (Previously Presented): The gaming device according to claim 1, wherein the first memory device is a ROM provided on the mother board,

wherein the second memory device is a hard disk which is independent from the mother board, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk.

Claim 3 (Currently Amended): The gaming device according to claim 1, wherein the gaming ~~machine~~ device is configured for business use.

Claim 4 (Currently Amended): A gaming device configured to execute a game, the gaming device comprising:

a first memory device configured to store a boot program executed when ~~the information process device of~~ the gaming ~~machine~~ device is started to operate;

a mother board on which the first memory device is provided;

a second memory device configured to store a game application program, the second memory device being connected to the mother board and electrically rewritable;

a control device configured to execute a fault inspection program to inspect whether or not a fault occurs in the second memory device and the game application program stored therein;

wherein the fault inspection program is stored in the first memory device, and the control device executes the fault inspection program every time the ~~information process~~ gaming device is started to operate and completes the execution of the fault inspection program before the game is started, and

wherein when the fault does not occur in the second memory device the game application program is started to execute and when the fault occurs in the second memory device an error is displayed on a display device located on ~~the~~ an exterior of the gaming ~~machine~~ device.

Claim 5 (Previously Presented): The gaming device according to Claim 4,

wherein the first memory device is a ROM provided on the mother board,

wherein the second memory device is a hard disk which is independent from the mother board, and

wherein the control device executes the fault inspection program stored in the ROM to inspect whether or not the fault occurs in the hard disk.

Claim 6 (Previously Presented): The gaming device according to Claim 5, further comprising:

a RAM provided on the mother board;

wherein the game application program is loaded from the hard disk to the RAM and executed by the control device when the fault does not occur in the hard disk.

Claim 7 (Previously Presented): A gaming device configured to execute a game, the gaming device comprising:

a first memory device for storing a boot program executed when the gaming device is started to operate;

a mother board on which the first memory device is provided;

a second memory device for storing a game application program for the game and a BIOS, the second memory device being connected to the mother board; and

a control device for executing a fault inspection program for the gaming device to inspect whether or not a fault occurs in the second memory device and the game application program stored therein;

wherein the fault inspection program is stored in the first memory device, and the control device executes the boot program to initialize the BIOS stored in the second memory device before executing the fault inspection program when the gaming device is started to

operate, and completes the execution of the fault inspection program before the game is started.

Claim 8 (Currently Amended): The gaming device according to claim 1, wherein the first memory device and the mother board are located in the ~~information process~~ gaming device.

Claim 9 (Previously Presented): The gaming device according to claim 1, wherein the second memory device is a flash memory.

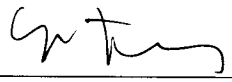
Claim 10 (Previously Presented): The gaming device according to Claim 4, wherein the display device is a liquid crystal display.

REMARKS/ARGUMENTS

Entry of this Amendment After Allowance under 37 C.F.R. § 1.312 is respectfully requested since it does not add any new matter. More specifically, the amendment to claims 3, 4 and 8 corrects antecedent errors. These antecedent errors in the claims were discovered by Applicant's attorney during a post-allowance review of the claims, and the attorney has been diligent in correcting any informalities that he has become aware of.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, L.L.P.



Bradley D. Lytle
Registration No. 40,073

Craig R. Feinberg
Registration No. 62,116

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 07/09)

Electronic Acknowledgement Receipt

EFS ID:	6596434
Application Number:	11205121
International Application Number:	
Confirmation Number:	2910
Title of Invention:	Gaming apparatus having memory fault detection
First Named Inventor/Applicant Name:	Jun Haishima
Customer Number:	22850
Filer:	Marvin Jay Spivak/Jerri Klatecki
Filer Authorized By:	Marvin Jay Spivak
Attorney Docket Number:	276900US90
Receipt Date:	08-DEC-2009
Filing Date:	17-AUG-2005
Time Stamp:	16:58:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		276900USAMN312.pdf	197106 09b624ad6a9dde84eee4812d4be1c85dc75952f4	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment after Notice of Allowance (Rule 312)	2	2
	Claims	3	6
	Applicant Arguments/Remarks Made in an Amendment	7	7
Warnings:			
Information:			
	Total Files Size (in bytes):	197106	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No. 276900US8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Jun HAISHIMA

SERIAL NO: 11/205,121 ART UNIT: 2114

FILING DATE: August 17, 2005 EXAMINER: LE, DIEU MINH T.

FOR: **GAMING APPARATUS HAVING MEMORY FAULT DETECTION**

FEE TRANSMITTAL

■ No additional fee is required

☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.

The Fee has been calculated as shown below:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	10 - 20 =	0	x $52 =	$0.00
INDEPENDENT CLAIMS	3 - 3 =	3	x $220 =	$660.00
☐ MULTIPLE DEPENDENT CLAIMS (If applicable)			+ $390 =	$0.00
☐ LATE FILING OF DECLARATION			+ $130 =	$0.00
			BASIC FEES	$0.00
			TOTAL OF ABOVE CALCULATIONS	$660.00
☐ REDUCTION BY 50% FOR FILING BY SMALL ENTITY				$0.00
☐ FILING IN NON-ENGLISH LANGUAGE			+ $130 =	$0.00
			TOTAL	$660.00

☐ Please charge Deposit Account No. **15-0030** in the amount of _____

☐ Credit card payment is being made online (if electronically filed), or is attached hereto (if paper filed), in the amount of _____.

■ The Director is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no payment is enclosed herewith, or credit any overpayment to Deposit Account No. **15-0030**, with the **EXCEPTION** of deficiencies in fees for multiple dependent claims in new applications.

■ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030.

Submitted by: _____

Bradley D. Lytle
Registration No. 40,073

Craig R. Feinberg
Registration No. 62,116

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 09/09)

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/205,121	08/17/2005	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/08/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DARRYL FORTE/

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22850 7590 09/25/2009

CUSTOMER NUMBER

22850

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	08/17/2005	Jun Haishima	276900US90	2910

TITLE OF INVENTION: GAMING APPARATUS HAVING MEMORY FAULT DETECTION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/28/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, DIEU MINH T	2114	714-036000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Oblon, Spivak,
2 McClelland, Maier
3 & Neustadt, L.L.P.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: UNIVERSAL ENTERTAINMENT CORPORATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Tokyo, JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☒ Payment by credit card. Transmitted via EFS-Web.

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 15-0030 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date DEC 24 2009

Typed or printed name Paul J. Killos Registration No. [illegible]

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DOCKET NO.: 276900US8/ssa

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jun HAISHIMA

SERIAL NUMBER: 11/205,121 GROUP: 2114

FILED: August 17, 2005 EXAMINER: LE, DIEU MINH T

FOR: GAMING APPARATUS HAVING MEMORY FAULT DETECTION

REQUEST TO CORRECT TITLE OF INVENTION

MAIL STOP ISSUE FEE
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

SIR:

In the matter of the above-identified application for patent, we hereby request correction of your records to reflect the correct title of the invention. The title of the invention should read as follows: **GAMING APPARATUS HAVING MEMORY FAULT DETECTION**.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, L.L.P.

Bradley D. Lytle
Registration No. 40,073

Derek P. Benke
Registration No. 56,944

Paul J. Killos
Registration No. 58,014

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 07/09)

Electronic Patent Application Fee Transmittal

Application Number:	11205121
Filing Date:	17-Aug-2005
Title of Invention:	Gaming apparatus having memory fault detection
First Named Inventor/Applicant Name:	Jun Haishima
Filer:	Marvin Jay Spivak/Mimi Chanthaphone
Attorney Docket Number:	276900US90

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1810**

Electronic Acknowledgement Receipt

EFS ID:	6706651
Application Number:	11205121
International Application Number:	
Confirmation Number:	2910
Title of Invention:	Gaming apparatus having memory fault detection
First Named Inventor/Applicant Name:	Jun Haishima
Customer Number:	22850
Filer:	Marvin Jay Spivak/Mimi Chanthaphone
Filer Authorized By:	Marvin Jay Spivak
Attorney Docket Number:	276900US90
Receipt Date:	24-DEC-2009
Filing Date:	17-AUG-2005
Time Stamp:	10:42:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1810
RAM confirmation Number	10031
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		276900USISSUEFEE.pdf	117762 3a873b2a4278c6116944b2093818713d93d3ec8f	yes	2

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Issue Fee Payment (PTO-85B)	1	1
Miscellaneous Incoming Letter	2	2

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	31492 b28549c35a5386003193041266d4a79bc98ce1be	no	2

Warnings:

Information:

Total Files Size (in bytes):	149254

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
11/205,121	08/17/2005	2114	1300	276900US90	3	1

CONFIRMATION NO. 2910

CORRECTED FILING RECEIPT

22850
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

Date Mailed: 12/30/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jun Haishima, Tokyo, JAPAN;

Assignment For Published Patent Application

Aruze Corp., Tokyo, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 022850

Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2004-245337 08/25/2004

If Required, Foreign Filing License Granted: 09/02/2005

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/205,121**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

GAMING APPARATUS HAVING MEMORY FAULT DETECTION

Preliminary Class

714

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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Bib Data Sheet

CONFIRMATION NO. 2910

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/205,121	08/17/2005 RULE	714	2114	276900US90

APPLICANTS
Jun Haishima, Tokyo, JAPAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS *********************
JAPAN 2004-245337 08/25/2004

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 09/02/2005

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no	JAPAN	3	3	1
35 USC 119 (a-d) conditions met: ☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged: Examiner's Signature Initials				

ADDRESS
22850

TITLE
GAMING APPARATUS HAVING MEMORY FAULT DETECTION

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1300	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Docket No.: 276900US8/jkl

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jun HAISHIMA

SERIAL NUMBER: 11/205,121 GROUP: 2114

FILED: August 17, 2005 EXAMINER: LE, DIEU MINH T.

FOR: **GAMING APPARATUS HAVING MEMORY FAULT DETECTION**

O.K. to enter
/dml/
01/04/10

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. § 1.312

MAIL STOP ISSUE FEE
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

SIR:

In response to the Notice of Allowability dated September 25, 2009, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	08/17/2005	Jun Haishima	276900US90	2910

22850 7590 01/12/2010

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
01/12/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Response to Rule 312 Communication	Application No.	Applicant(s)
	11/205,121	HAISHIMA, JUN
	Examiner	Art Unit
	Dieu-Minh Le	2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *08 December 2009* under 37 CFR 1.312 has been considered, and has been:

   a) ☐ entered.

   b) ☒ entered as directed to matters of form not affecting the scope of the invention.

   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

   d) ☐ disapproved. See explanation below.

   e) ☐ entered in part. See explanation below.

The request to correct title of invention filed on 12/24/2009 also has been entered.

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit 2114

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/205,121	02/16/2010	7664988	276900US90	2910

22850 7590 01/27/2010

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 439 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jun Haishima, Tokyo, JAPAN;