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Nelson

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(54) **LOW PIN COUNT (LPC) FIRMWARE HUB RECOVERY**

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(58) **Field of Search** 710/104, 300–304, 710/305–317; 713/1; 365/185.08, 185.11, 185.33

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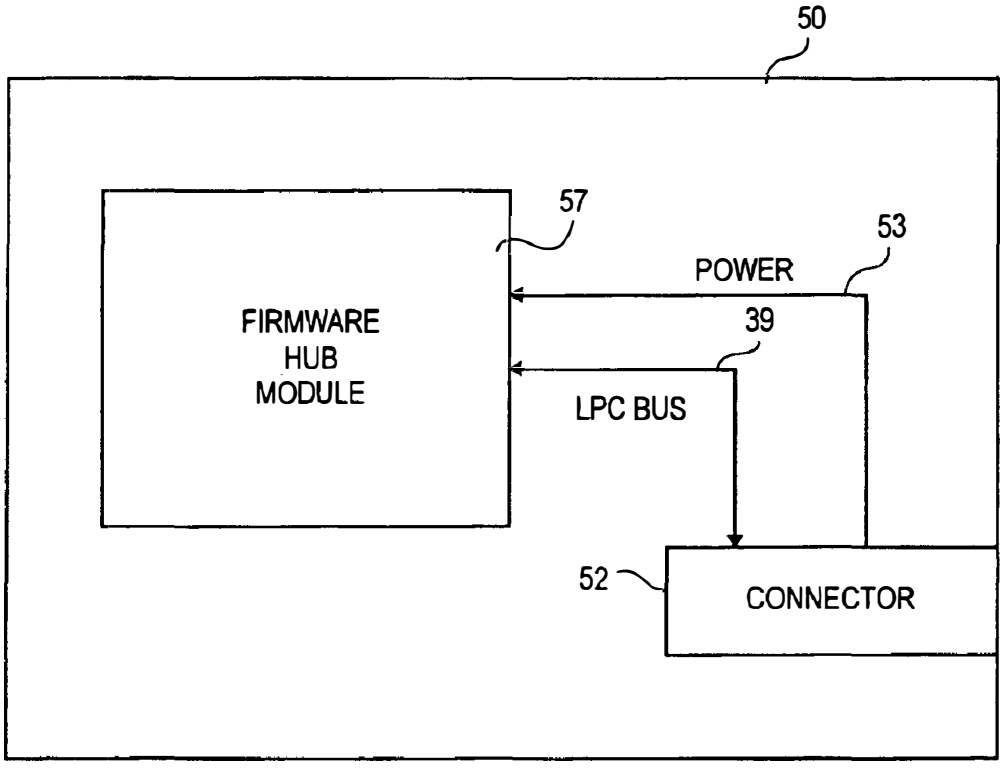
(57) **ABSTRACT**

A method and apparatus for low pin count firmware hub recovery on a circuit board having a firmware hub includes coupling a firmware hub recovery module having a firmware program onto the circuit board, establishing communication between a central processing unit (CPU) and the firmware hub recovery module, and reprogramming the firmware hub by the firmware program.

22 Claims, 3 Drawing Sheets



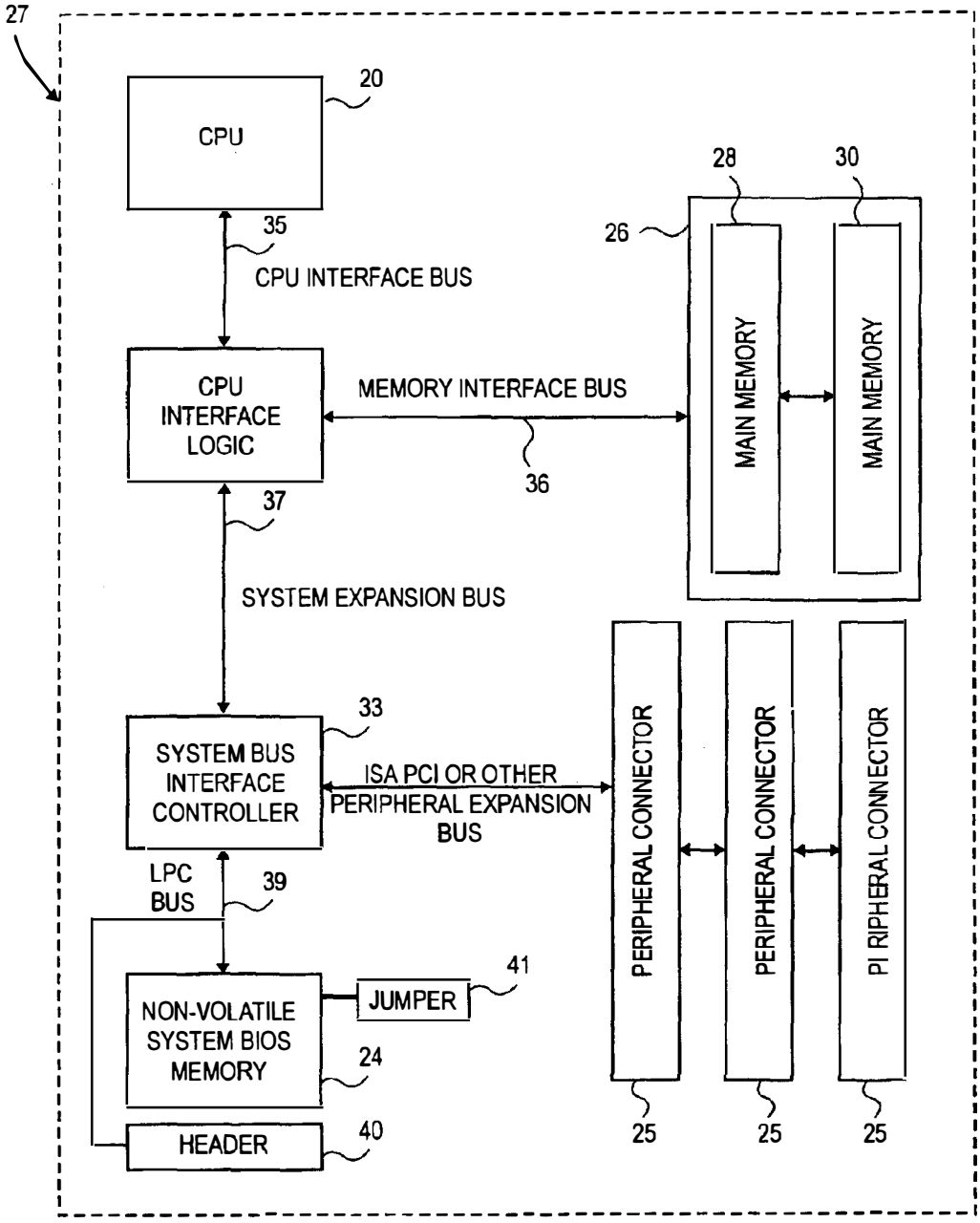


FIG. 1

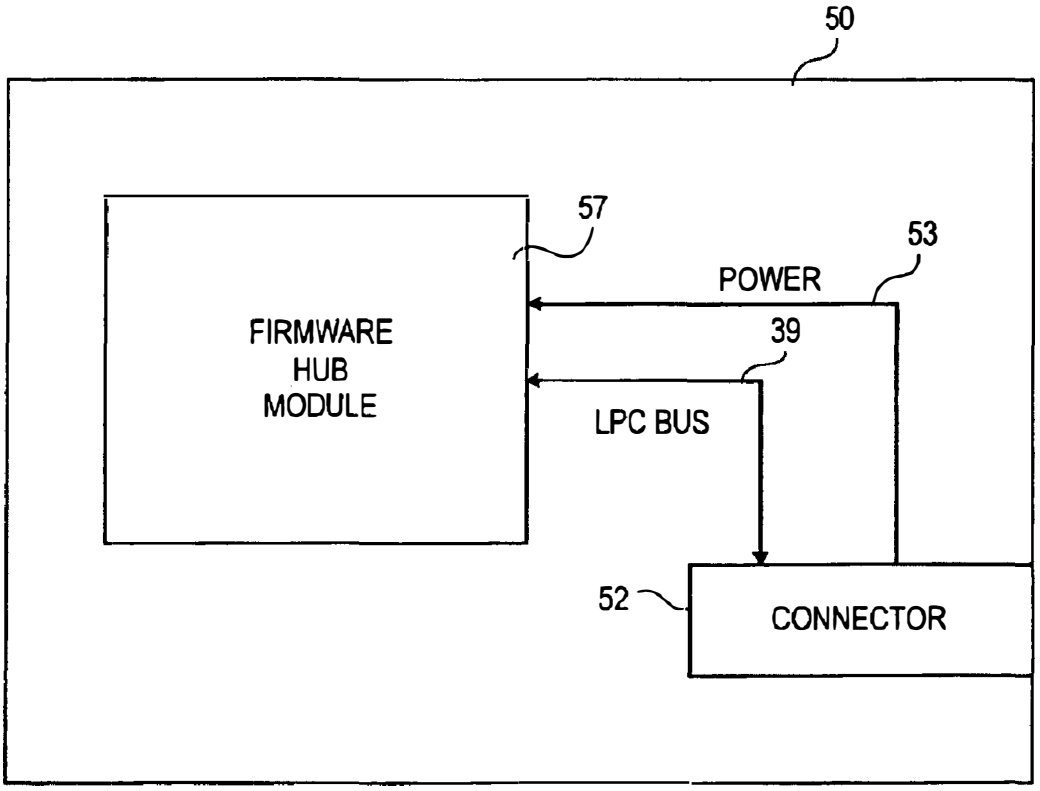


FIG. 2

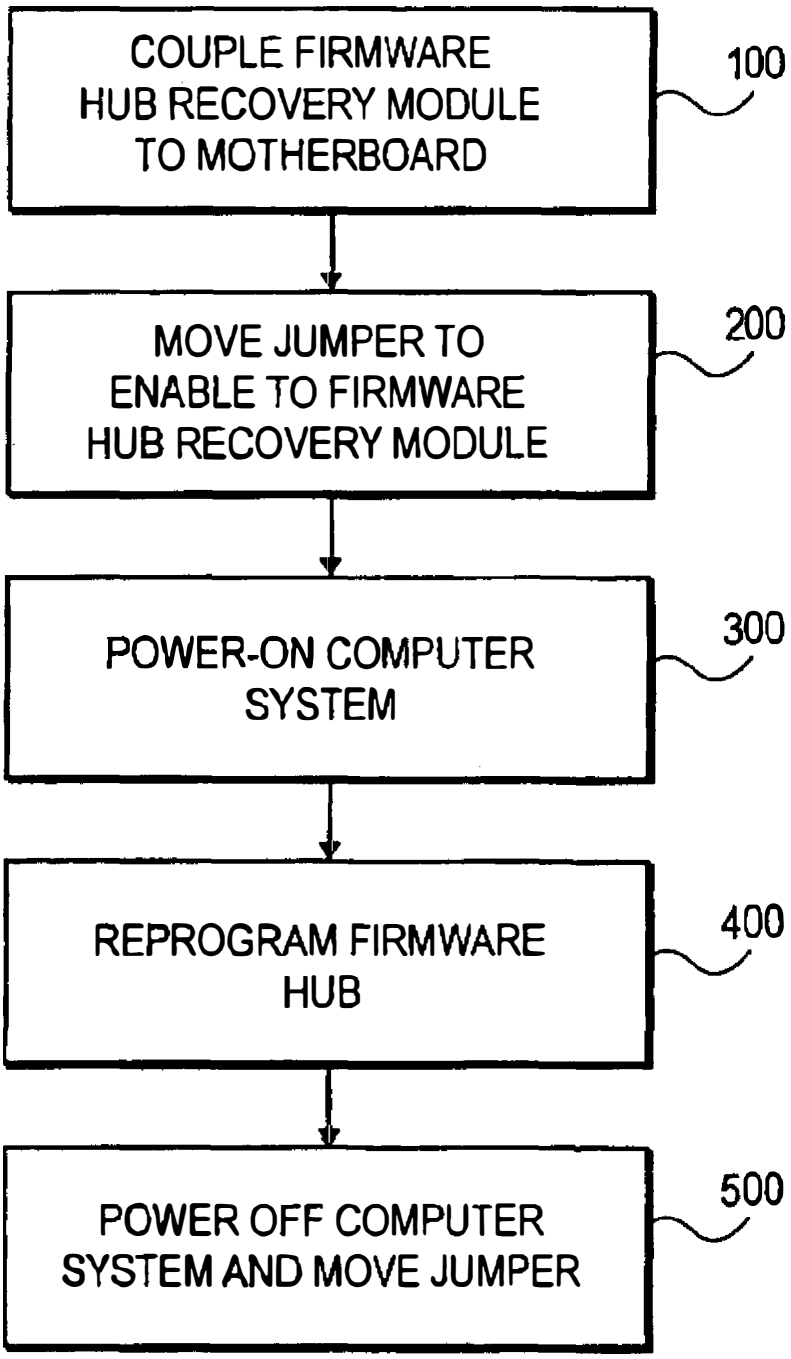


FIG. 3

LOW PIN COUNT (LPC) FIRMWARE HUB RECOVERY

FIELD OF THE INVENTION

Embodiments of the present invention provide a method and apparatus for firmware hub programming on a circuit board. More particularly, embodiments of the present invention provide methods and apparatus for low pin count (LPC) firmware hub recovery on a circuit board via a firmware hub recovery module.

BACKGROUND OF THE INVENTION

Conventional computer systems include a variety of peripheral and memory devices that communicate with the systems's central processing unit (CPU) or chip-set processor via an Industry Standard Architecture (ISA) bus or an Expansion bus (X-bus). The CPU or chip-set processor includes a large amount of pins (e.g., approximately 50–70) and associated circuitry to support the ISA bus or X-bus signals that are used to interface the CPU or chip-set processor with the peripheral devices including input/output (I/O) or I/O controllers, floppy disk controller, keyboard controllers, and memory devices such as non-volatile memory devices that store, for example basis input-output system (BIOS) information.

The large number of pins needed to support the ISA bus and X-bus standards generally increase the overall system cost. For example, larger packages are required for a CPU or chip-set. The development of the low pin count (LPC) bus has obviated to some extent the problem mentioned above. The LPC bus includes general purpose signal lines that carry substantially all time-multiplexed address, data and control information to implement memory, I/O, and bus transactions between the CPU and other system devices.

Presently there are no other peripheral components that are connected to the LPC bus because the LPC bus is designed to be a "local bus" servicing the chip-set. The LPC bus does not provide for expandability for add-on features like that provided for by a Peripheral Component Interconnect (PCI) (e.g., PCI Local Bus Specification, version 2.1, a copy of which may be obtained from the PCI Special Interest Group) bus for example. In general the LPC bus may be limited to being coupled to a system bus interface controller and one or more memory devices. As used herein, the term "firmware hub" refers to the memory devices coupled to a LPC bus.

The firmware in the firmware hub is a computer program including a series of instructions or statements arranged in a specific sequence and written in a language executable by the processor of the computing device to achieve a certain result.

Firmware, as used herein, refers to those computer programs whose instructions and/or data are stored and maintained permanently in the computing device without the need for the continued application of power. One such computer program is the basic input/output system (BIOS). These computer programs, like the BIOS are typically stored in non-volatile read only memory (ROM), programmable read only memory (PROM) or erasable programmable read only memory (EPROM). Use of a non-volatile memory obviates the need to reload the programming into the computing device in the event of a power loss or turn-off.

when programming corrections or upgrades are required. The EEPROM includes a read only memory device whose individual data storage locations (addresses) are erasable and can be reprogrammed by applying certain electrical signals to the chip. New firmware can thus be stored in the chip without removing the chip from the computing device. However, in situations where the computing device's firmware has been corrupted to an extent that the computing device is unable to boot-up, the above mentioned method of supplying new firmware is not available. In these cases, there is no other solution but to replace the firmware chip.

In view of the foregoing, it can be appreciated that a substantial need exists for a method and apparatus for low pin count firmware hub recovery.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will become apparent from the following detailed description in combination with the figures listed below.

FIG. **1** is a block diagram of an circuit board including a low pin count (LPC) bus according to an embodiment of the present invention.

FIG. **2** is a block diagram of a firmware hub updating module according to an embodiment of the present invention.

FIG. **3** is a flow diagram illustrating a method for low pin count (LPC) firmware hub recovery in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

Embodiments of methods and systems for low pin count (LPC) firmware hub recovery using a firmware hub recovery module.

In the following description, for purposes of explanation, numerous specific details are set forth to provide a thorough understanding of the present invention. It will be appreciated, however, by one skilled in the art that the present invention may be practiced without these specific details. In other instances, structures and devices are shown in block diagram form. Furthermore, one skilled in the art can readily appreciated that the specific sequence in which methods are presented and performed are illustrative and it is contemplated that the sequences can be varied and still remain within the spirit and scope of the present invention.

FIG. **1** illustrates a block diagram of a computer system's circuit board **27** including a low pin count (LPC) bus **39** according to an embodiment of the present invention. Circuit board **27** may be a mother board and typically includes a processor such as a central processing unit or CPU **20**. The CPU is the "brains" or "engine" of the computer system responsible for overseeing all execution of operations in the computer. Motherboard **27** also includes CPU interface logic **21**, coupled to CPU **20** and interfacing CPU **20** with other circuit components such as a system bus interface controller **33** and main memory **26**. As shown, system bus interface controller **33** may be any type of expansion bus controller such as a PCI bus or peripheral bus I/O controller. System bus interface controller **33** is coupled to CPU interface logic **21** and is coupled to peripheral connectors **25** via expansion bus **38**. A bus that complies with a Peripheral Component Interconnect (PCT) standard (e.g., PCI Local Bus Specification, version 2.1, a copy of which may be obtained from the PCI Special Interest Group) is a example of such an expansion bus. Main memory **26** may include random

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